DLC Display Co., Limited

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MODEL No:DLC0245AZP05DF-1

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Record of Revision

Date	Revision No.	Summary
2019-11-01	1.0	Rev 1.0 was issued
2023-08-08	2.0	Change driver IC from ST7796S to ST7365P

1. Scope

This data sheet is to introduce the specification of DLC0245AZP05DF-1 active matrix TFT module. It is composed of a color TFT-LCD panel, driver IC, FPC and a backlight unit. The 2.45″ display area contains 272(RGB) x 480 pixels.

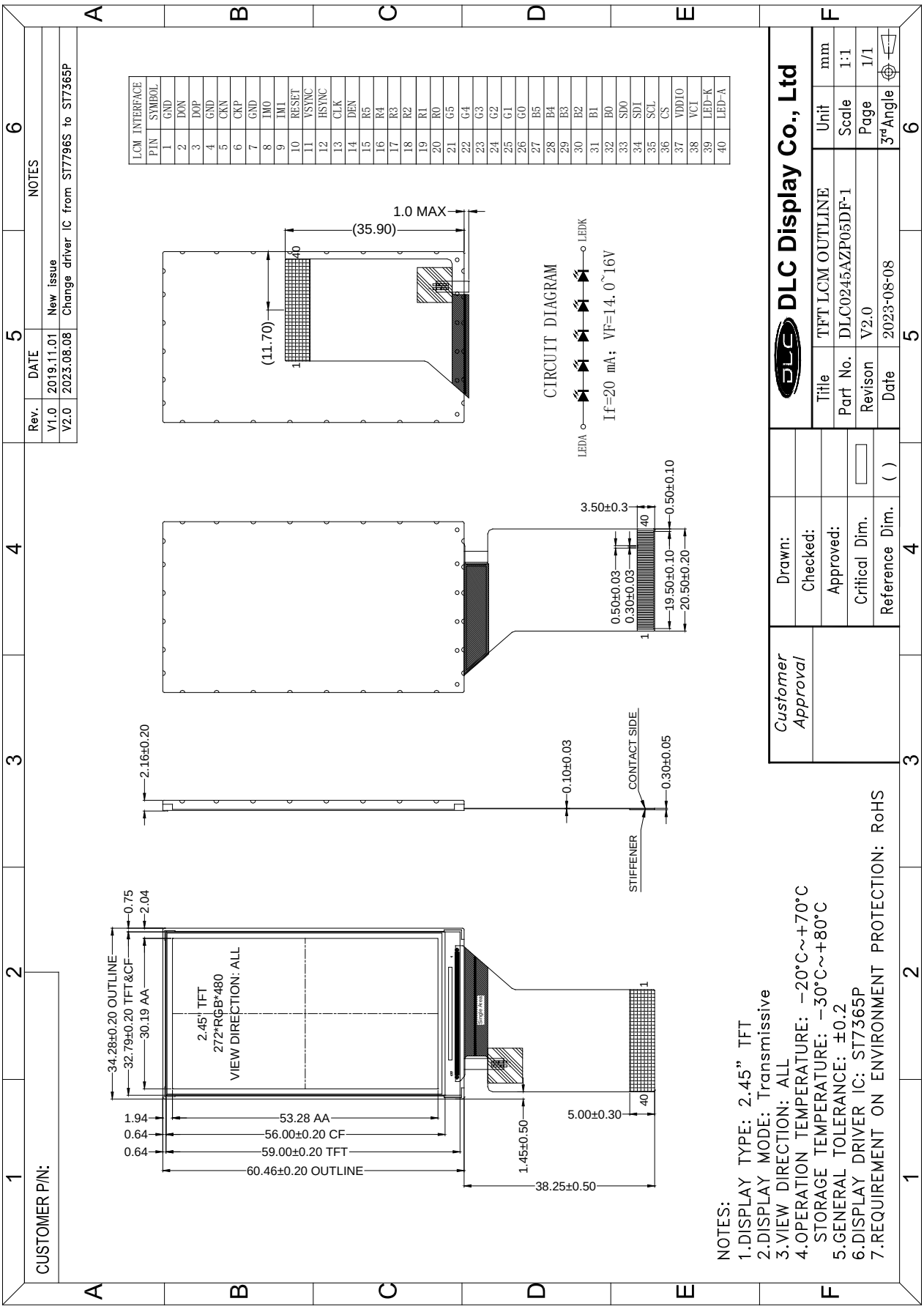
2. Application

Digital equipments which need color display outdoor, mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	2.45	inch
Resolution	272(RGB) x 480	/
Interface	MIPI / RGB / SPI	/
Technology type	a-Si TFT	/
Pixel pitch	0.111 x 0.111	mm
Pixel Configuration	R.G.B. Vertical Stripe	
Outline Dimension (W x H x D)	34.28 x 60.46 x 2.16	mm
Active Area	30.19 x 53.28	mm
Display Mode	Transmissive	/
Viewing Direction	ALL	/
Backlight Type	LED	/
Display Driver IC	ST7365P	/

4. Outline Drawing



5. Interface signals

No	Symbol	Description	Remarks
1	GND	Ground	
2	D0N	Negative polarity of low voltage differential data signal	
3	D0P	Positive polarity of low voltage differential data signal	
4	GND	Ground	
5	CKN	Negative polarity of low voltage differential clock signal	
6	CKP	Positive polarity of low voltage differential clock signal	
7	GND	Ground	
8	IM0	The MCU interface mode select	
9	IM1	The MCU interface mode select	
10	RESET	This signal will reset the device and must be applied to properly initialize the chip.	
11	VSYNC	Frame synchronizing signal for RGB interface operation	
12	HSYNC	Line synchronizing signal for RGB interface operation	
13	CLK	Dot clock signal for RGB interface operation	
14	DEN	Data enable signal for RGB interface operation	
15~20	R5 – R0	Red data bus	
21~26	G5 – G0	Green data bus	
27~32	B5 – B0	Blue data bus	
33	SDO	Serial output signal	
34	SDI	SPI interface input/output pin The data is applied on the rising edge of the SCL signal.	
35	SCL	In SPI mode, this pin is used as SCL	
36	CS	Chip select pin	
37	VDDIO	Power supply for I/O system	
38	VCI	Power supply	
39	LED-K	Cathode pin of Backlight	
40	LED-A	Anode pin of Backlight	

Note:

0	1	3SPI	SDA, SDO
1	0	MIPI	MIPI_DATA MIPI_CLOCK

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Power Supply Voltage (Analog)	VDD	-0.3	4.6	V	
Power Supply Voltage (I/O)	VDDI	-0.3	4.6	V	
Power Supply Voltage (Logic)	VCC	-0.3	2	V	
Driver Supply Voltage	VGH-VGL	-0.3	30	V	
Logic Input Voltage Range	V_{IN}	0.5	VDDI+0.5	V	
Logic Output Voltage Range	V_O	0.5	VDDI+0.5	V	

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

7.Electrical Specifications

7.1 Electrical characteristics

VSSD=0V, Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		VCC	2.5	2.75	3.3	V	
		VDDI	1.65	1.8	3.3		
Gate Driver high Voltage		VGH	12.54	-	15.46		
Gate Driver low Voltage		VGL	-12.5	-	-7.15		
Input Signal Voltage	Low Level	VIL	VSSD	-	0.3*IOVCC	V	
	High Level	VIH	0.7*IOVCC	-	IOVCC	V	

7.2 LED Backlight

Ta=25℃

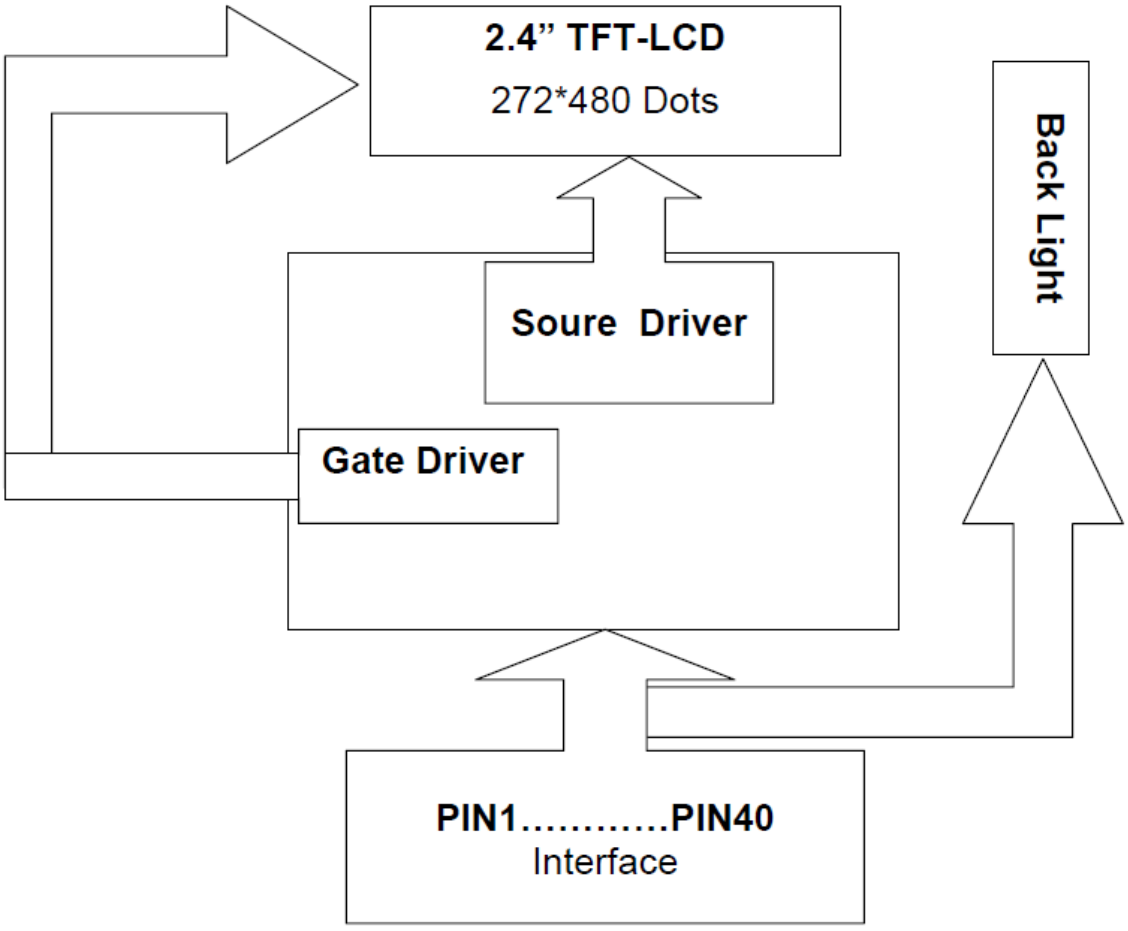
Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF	-	20	-	mA	
Forward Voltage	VF	14	-	16	V	
LED life time	-	-	30,000	-	Hrs	

Note: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The “LED life time” could be decreased if operating IL is larger than 20mA.

CIRCUIT DIAGRAM

If=20 mA; VF=14.0~16V

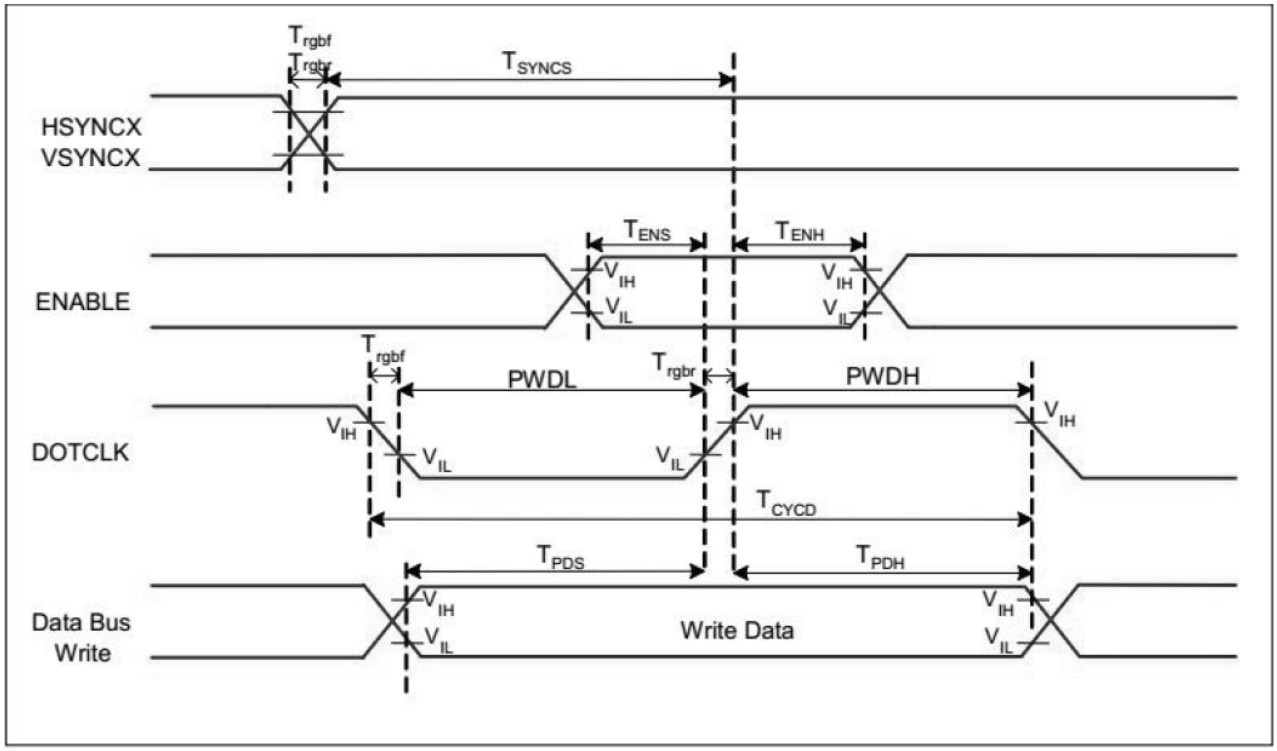
7.3 Block Diagram of LCM



8. Command/AC Timing

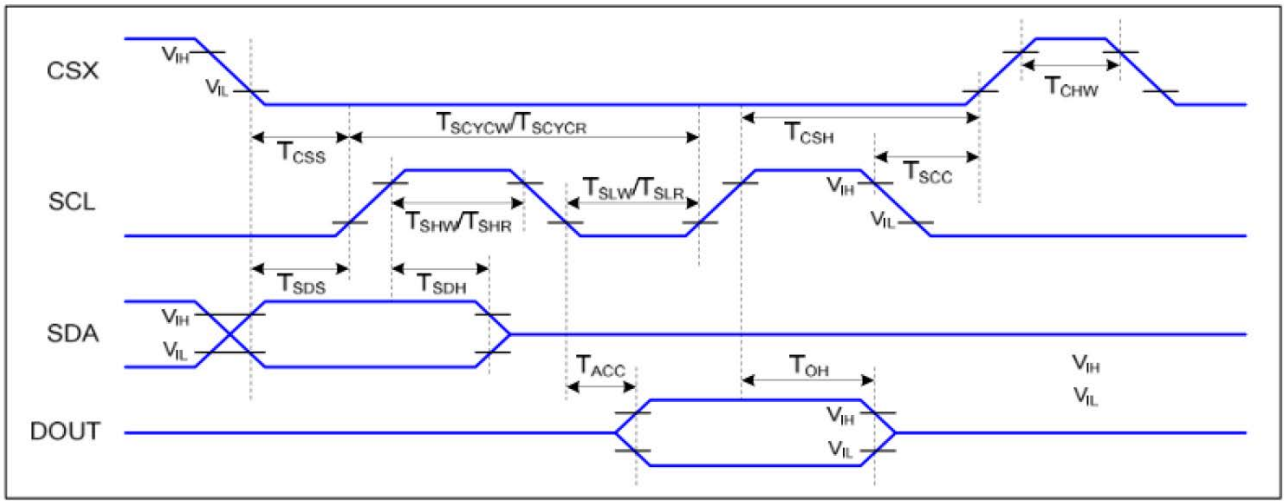
8.1 Timing Characteristics

8.1.1 RGB Interface Characteristics



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC VSYNC	TSYNCS	VSYNC, HSYNC setup time	15	-	ns	
ENABLE	TENS	Enable setup time	15	-	ns	
	TENH	Enable hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse width	30	-	ns	
	PWDL	DOTCLK low-level pulse width	30	-	ns	
	TCYCD	DOTCLK cycle time	66	-	ns	
	Trghr, Trghf	DOTCLK rise/fall time	-	15	ns	
DB	TPDS	PD data setup time	15	-	ns	
	TPDH	PD data hold time	15	-	ns	

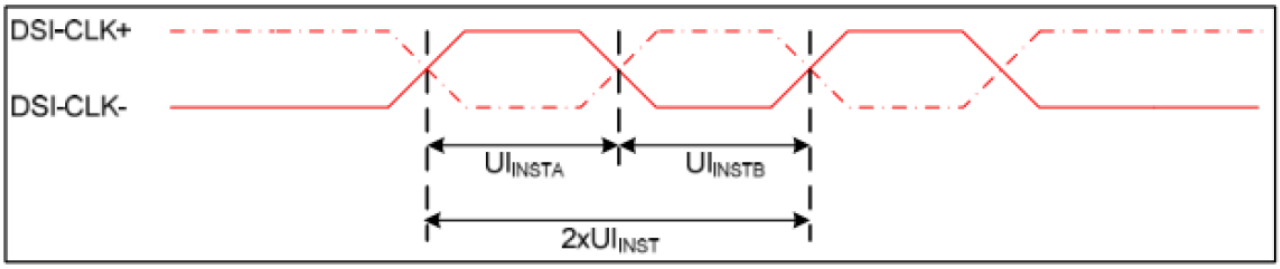
8.2 3-SPI Serial Data Transfer Interface Characteristics



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	tCSS	Chip select setup time (write)	15	-	ns	
	tCSH	Chip select hold time (write)	15	-	ns	
	tCSS	Chip select setup time (read)	60	-	ns	
	tSCC	Chip select hold time (read)	65	-	ns	
	tCHW	Chip select “H” pulse width	40	-	ns	
SCL	tSCYCW	Serial clock cycle (write)	66		ns	
	tSHW	SCL “H” pulse width (write)	15		ns	
	tSLW	SCL “L” pulse width (write)	15		ns	
	tSCYCR	Serial clock cycle (read)	150		ns	
	tSHR	SCL “H” pulse width (read)	60		ns	
	tSLR	SCL “H” pulse width (read)	60		ns	
SDA (DIN)	tSDS	Data setup time	10	-	ns	
	tSDH	Data hold time	10	-	ns	
DOUT	tACC	Access time	10	50	ns	For maximum CL=30Pf For minimum CL=8pF
	tOH	Output disable time	15	50	ns	

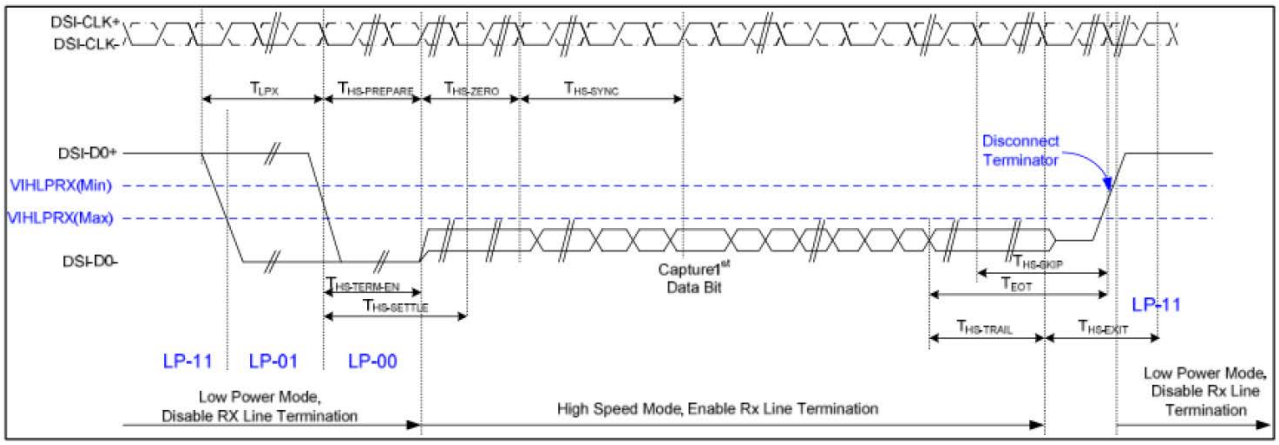
8.3 MIPI Interface Characteristics

8.3.1 High Speed Mode – Clock Channel Timing



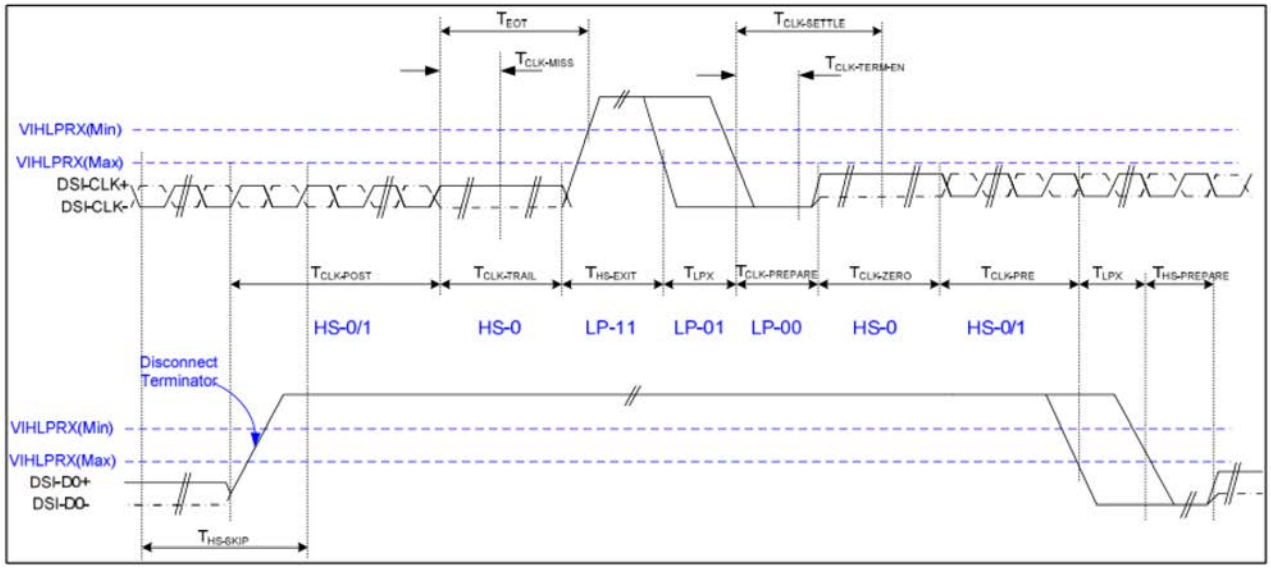
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-DATA_P/N	2xUI INST	Double UI instantaneous	4	25	ns	
DSI-DATA_P/N	UI INSTA ,UI INSTB	UI instantaneous Half	2	12.5	ns	

8.3.2 High-Speed Data Transmission



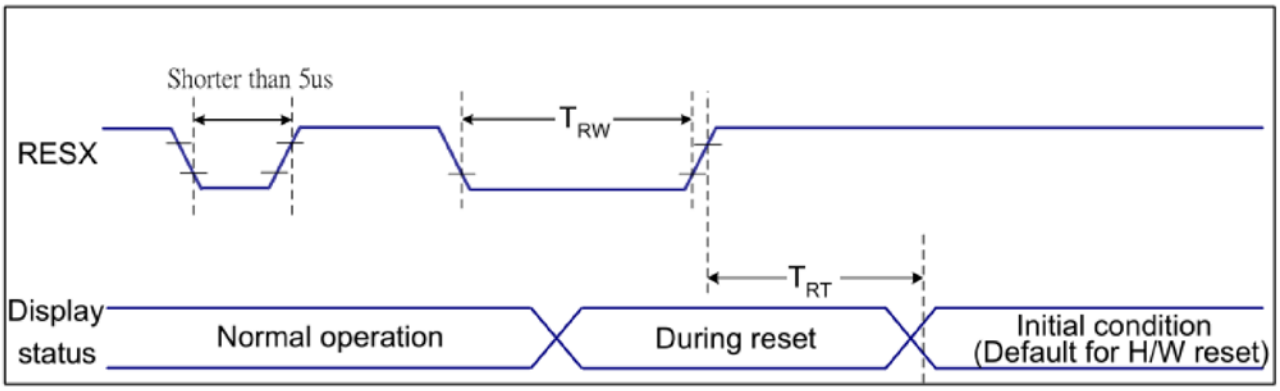
Parameter	Symbol	MIN	TYP	MAX	Unit
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

8.3.3 Switching the Clock Lane Between Clock Transmission and Low-Power Mode



Parameter	Symbol	MIN	TYP	MAX	Unit
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

8.4 Reset Timing



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

9. Optical Specification

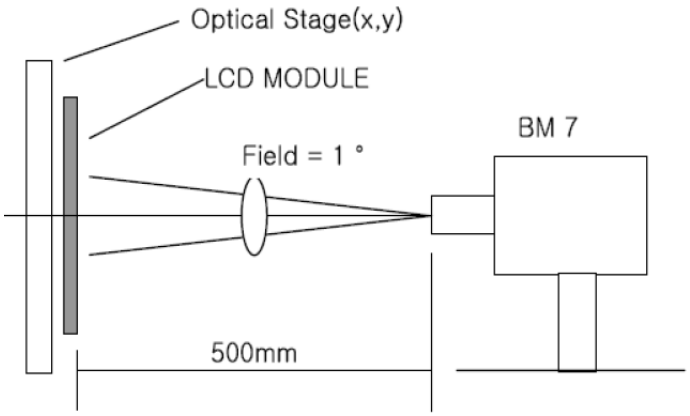
Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	-	1000	-		Note1 Note2
Response Time		Tr+Tf	25℃	-	25	-	ms	Note1 Note3
View Angles		ΘT	CR≧10	-	80	-	Degree	Note 4
		ΘT		-	80	-		
		ΘL		-	80	-		
		ΘR		-	80	-		
Chromaticity	White	x	Brightness is on	Typ-0.05	0.303	Typ+0.05		Note5, Note1
		y			0.331			
	Red	x			0.594			
		y			0.325			
	Green	x			0.292			
		y			0.547			
	Blue	x			0.149			
		y			0.161			
Luminance		L		-	560	-	cd/m^2	Note1 Note6
Uniformity (White)		U		80	-	-	%	Note1 Note7

Test condition: Ta=25ºC, VDD=3.3V

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

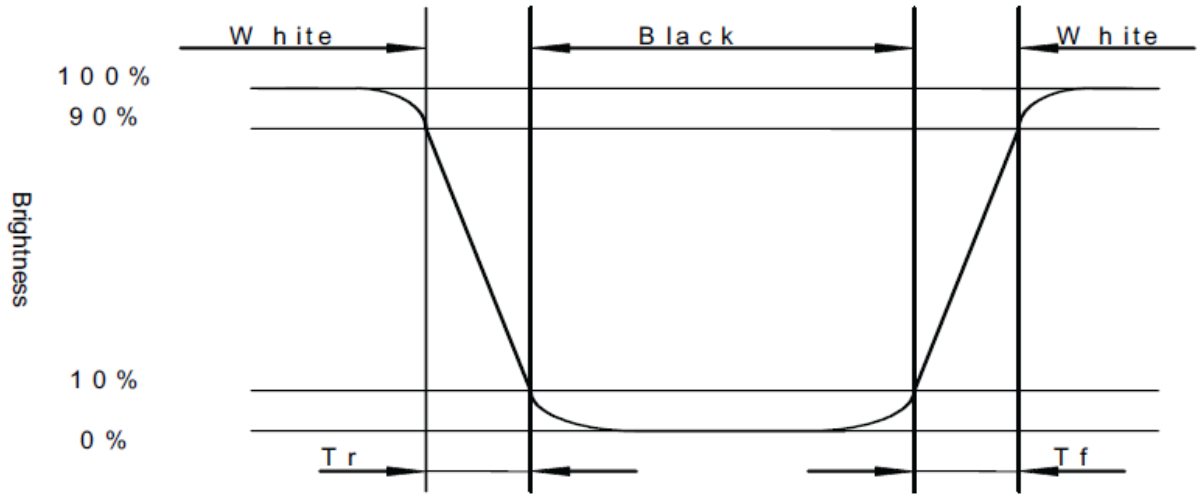


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

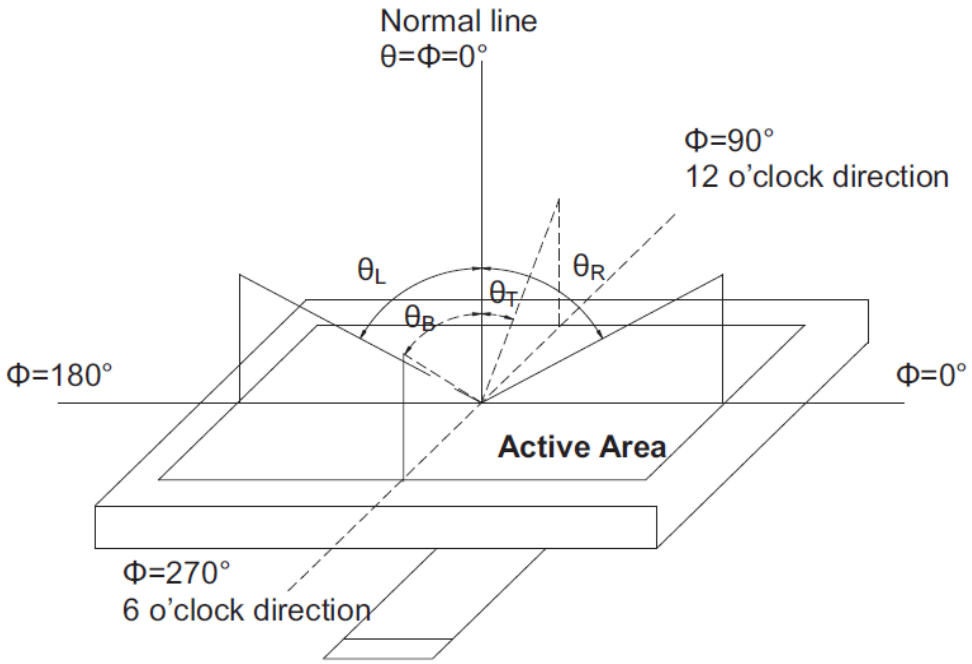
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



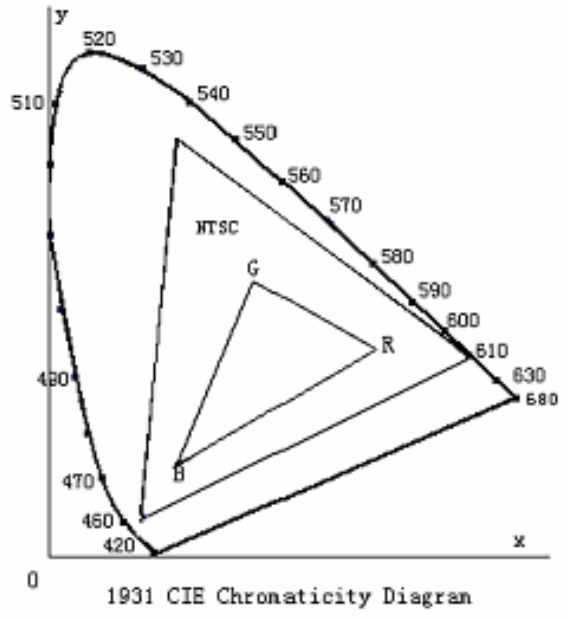
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



1931 CIE Chromaticity Diagran

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity(U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

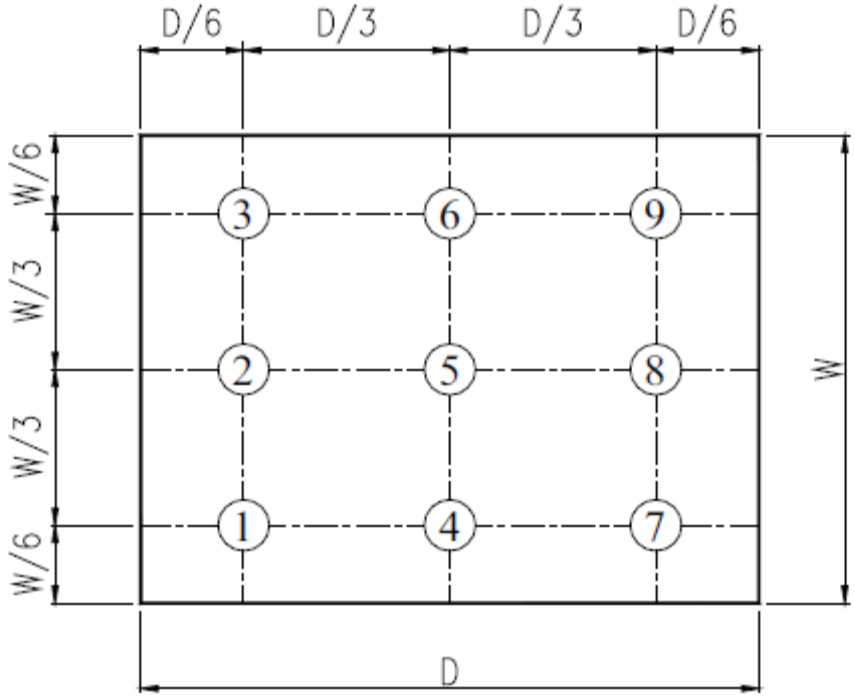


Fig. 2 Definition of uniformity

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ta= +70℃, 96hrs	Per table in below
2	Low Temp Operation	Ta= -20℃, 96hrs	Per table in below
3	High Temp Storage	Ta= +80℃, 96hrs	Per table in below
4	Low Temp Storage	Ta= -30℃, 96hrs	Per table in below
5	High Temp & High Humidity Storage	Ta= +60℃, 90% RH, 96 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30℃ 30 min~+70℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω， 5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

A. Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.
B. In order to make the display assembly stable and firm, DLC recommends to design some supporting at the display backside, especially for the display with tape-attached touch panel, such supporting is important and essential, or else, the display may drop-off from front after some period of time.
C. Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.