

# **Application of High-Power Snubberless Semiconductor Switches in High-Frequency PWM Converters**

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# **Application of High-Power Snubberless Semiconductor Switches in High-Frequency PWM Converters**

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## **Abstract**

For many years, power electronics in the high-power area was performed with extremely slow semiconductor switches. These switches, including the thyristor and the Gate Turn-Off (GTO) thyristor, had the capacity to handle very high voltages and currents but lacked the ability to perform high frequency switching. Low-power converters, such as computer power supplies and low horsepower motor drives, have employed high-frequency switching for years and have benefited from very nice output waveforms, good control dynamic performance, and many other advantages compared to low frequency switching. Recent improvements in high-power semiconductor technology has brought switching performance similar to that of the low-power MOSFETs and IGBTs to the high-power area through the advancement of the IGBT's ratings to create the High Voltage IGBT (HVIGBT) and the development of new GTO-derived devices including the Integrated Gate Commutated Thyristor (IGCT) and the Emitter Turn-Off (ETO) thyristor. These new devices all feature high switching speed and the capability to turn off without the requirement for a turn-off snubber. With these new device technologies the high-power field of power electronics can realize dramatic improvements in the performance of systems for utility applications and motor drives.

However, with these high-speed switches come new issues relating to noise, protection, performance of diodes, and thermal management in high-frequency applications. This thesis addresses the application of these new devices, especially the ETO and the IGCT.

Examples of each device technology (IGBT, IGCT, and ETO) have been characterized in both their switching performance and conduction loss. The tests performed show how these new devices may be applied to various applications. The switching loss, especially related to turn-off, is the dominant factor in the power dissipation of the high-power switches, so knowledge of these characteristics are very important in the system design.

To demonstrate the operation of the ETO, two power converters were constructed. The first was a 100 kW DC/DC converter, which demonstrated the operation of the ETO in a typical building block configuration, the half-bridge. The second system, a 1 MegaVolt-Amp (MVA) three-phase inverter, demonstrated the ETO in an application where the switching frequency and power level were both high. The test results demonstrate the expected characteristics of the high-frequency converters. The development of the ETO's gate driver is described.

During the inverter testing, a new failure mode was found involving a parasitic diode within the ETO. This failure mode was analyzed and solutions were proposed. One of the proposed solutions was implemented and there were no more failures of this type. Another possible failure mode regarding a circulating current in an IGCT-based system is also analyzed.

Soft-switching techniques can help reduce the switching loss in power semiconductor switches. Several topologies were considered for application in the high-power area, and one was selected for further investigation. A prototype Zero Current Transition (ZCT) circuit was developed using an IGCT as the main switch. The turn-off loss was reduced dramatically through the tested ZCT circuit, and the diode recovery was also alleviated.

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# Table of Contents

Abstract .....	I
Acknowledgements .....	III
Table of Contents .....	V
Chapter 1 - Introduction .....	1
1.1 UTILITY APPLICATIONS .....	1
1.2 MOTOR DRIVES .....	2
1.3 OTHER HIGH POWER APPLICATIONS .....	3
1.4 CHALLENGES .....	3
1.5 OPPORTUNITIES .....	4
Chapter 2 - High-Power, High-Speed Devices .....	5
2.1 DEVICE TECHNOLOGY BACKGROUND .....	5
2.2 PULSE TESTER USED FOR CHARACTERIZATION .....	9
2.3 DEVICES USED FOR COMPARISON .....	12
2.4 UNITY GAIN VERIFICATION .....	14
2.5 GATE DRIVE CIRCUITS .....	16
2.6 FORWARD CONDUCTION LOSS CHARACTERIZATION .....	18
2.7 SWITCHING TESTS .....	18
2.8 DISCUSSION .....	23
2.9 COMPARISON CONCLUSIONS .....	25
Chapter 3 - ETO-based DC/DC Converter .....	26
3.1 OBJECTIVE .....	26
3.2 ETO1045HS CHARACTERISTICS .....	26
3.3 ETO PHASE LEG DESIGN .....	27
3.4 DC BUS DESIGN .....	29
3.5 dI/dT SNUBBER DESIGN .....	30
3.6 SYSTEM CONSTRUCTION .....	31

## Table of Contents

3.7	SYSTEM PERFORMANCE .....	31
3.8	THERMAL PERFORMANCE .....	32
3.9	BUCK MODE TESTING .....	33
3.10	DC/DC CONVERTER CONCLUSIONS.....	35
Chapter 4 -	ETO Based Three-Phase Inverter.....	36
4.1	SYSTEM CONFIGURATION .....	36
4.2	ETO1045HS BACKGROUND .....	37
4.3	ETO PHASE LEG .....	38
4.4	dI/dt SNUBBER AND VOLTAGE CLAMP DESIGN .....	40
4.5	INVERTER CAPABILITY DETERMINATION .....	43
4.6	UTILITY INVERTER CAPACITY .....	45
4.7	MOTOR DRIVE POWER CAPABILITY .....	48
4.8	SYSTEM TEST RESULTS .....	49
4.9	PROTECTION.....	51
4.10	THREE-PHASE TEST CONCLUSIONS .....	52
Chapter 5 -	Unconventional Failure Issues .....	54
5.1	ANODE SHORT STRUCTURES .....	54
5.2	ANODE SHORT PARASITIC DIODE.....	55
5.3	PARASITIC DIODE FAILURES .....	56
5.4	PROPOSED SOLUTIONS .....	57
5.5	IGCT ISSUES.....	59
Chapter 6 -	ETO Gate Driver Design.....	63
6.1	REQUIREMENTS .....	63
6.2	MOSFET DRIVER SECTION .....	65
6.3	ACTIVE CLAMP SECTION.....	66
6.4	GTO TURN-ON CURRENT INJECTION SECTION .....	70
6.5	POWER SUPPLY SECTION.....	71
Chapter 7 -	Soft Switching for High-Power Devices.....	76
7.1	INTRODUCTION.....	76

## Table of Contents

7.2	ARCP INVERTERS.....	77
7.3	QUASI-RESONANT DC-LINK THREE-LEVEL INVERTER.....	78
7.4	ZERO CURRENT TRANSITION CIRCUIT.....	79
7.5	ZCT CIRCUIT OPERATION PRINCIPLE.....	79
7.6	ZCT TEST SETUP.....	84
7.7	ZCT TEST RESULTS.....	88
7.8	SOFT-SWITCHING CONCLUSIONS.....	95
	Conclusions.....	97
	References.....	99
	Vita.....	101



## Table of Figures

### Table of Figures

FIGURE 1: GTO STRUCTURE AND EQUIVALENT CIRCUIT .....	6
FIGURE 2: IGBT CELL STRUCTURE AND EQUIVALENT CIRCUIT .....	7
FIGURE 3: GTO AND HARD-DRIVEN GTO GATING .....	8
FIGURE 4: GTO, IGCT, AND ETO GATE LOOPS .....	9
FIGURE 5: PULSE TESTER SCHEMATIC DIAGRAM .....	9
FIGURE 6: DOUBLE-PULSE TESTER WAVEFORMS .....	10
FIGURE 7: SWITCHING TIME DEFINITION WAVEFORM .....	12
FIGURE 8: (CLOCKWISE FROM TOP LEFT) ETO4060, EUPEC HVIGBT, MITSUBISHI HVIGBT, ABB IGCT, MITSUBISHI GCT.....	14
FIGURE 9: GCT UNITY GAIN .....	15
FIGURE 10: MITSUBISHI GCT GATE DRIVER .....	15
FIGURE 11: ETO4060 UNITY GAIN.....	16
FIGURE 12: FORWARD CONDUCTION VOLTAGE .....	18
FIGURE 13: TYPICAL TURN-OFF WAVEFORM .....	19
FIGURE 14: 2 kV SNUBBERLESS SWITCHING LOSS.....	20
FIGURE 15: STORAGE (OR DELAY) TIME COMPARISON .....	21
FIGURE 16: FALL TIME COMPARISON.....	21
FIGURE 17: GCT CURRENT TAIL DETAIL .....	22
FIGURE 18: PICTURE OF ETO1045HS.....	27
FIGURE 19: ETO1045HS HARD TURN-OFF AT 1kA, 3.3 kV .....	27
FIGURE 20: BOOST CONVERTER BASED ON A STANDARD PHASE LEG.....	27
FIGURE 21: ETO PHASE LEG DESIGN.....	28
FIGURE 22: PHOTOGRAPH OF COMPLETED PHASE LEG .....	29
FIGURE 23: DC BUS SHOWN WITH PHASE LEG INSTALLED .....	30
FIGURE 24: AN OVERALL VIEW OF THE CONVERTER.....	31
FIGURE 25: WAVEFORMS OF ETO BOOST CONVERTER RUNNING AT 100kW .....	32
FIGURE 26: VOLTAGE STRESS DURING DEVICE TURN-OFF AT 100kW.....	33
FIGURE 27: DETAIL OF THE TURN-OFF TRANSIENT .....	33
FIGURE 28: BUCK MODE PWM WAVEFORMS .....	34
FIGURE 29: DETAIL OF THE BUCK MODE TURN-OFF TRANSIENT.....	34

## Table of Figures

FIGURE 30: ETO-BASED THREE-PHASE INVERTER.....	36
FIGURE 31: PICTURE OF ETO1045HS.....	37
FIGURE 32: ETO1045HS CONDUCTION LOSS.....	37
FIGURE 34: 1kV SNUBBERLESS TURN-OFF LOSS .....	38
FIGURE 35: 2kV SNUBBERLESS TURN-OFF LOSS .....	38
FIGURE 36: ETO PHASE LEG DESIGN. ....	39
FIGURE 37: PHOTOGRAPH OF COMPLETED PHASE LEG.....	40
FIGURE 38: dI/dt SNUBBER INDUCTOR AND RESISTOR.....	41
FIGURE 39: PICTURE OF THE ETO-BASED INVERTER.....	42
FIGURE 40: MEASURED CONDUCTION LOSS AND LINEAR APPROXIMATION OF CONDUCTION LOSS .	44
FIGURE 41: 2kV SNUBBERLESS TURN OFF LOSS AND LINEAR APPROXIMATION .....	45
FIGURE 42: OUTPUT CURRENT VERSUS FREQUENCY.....	47
FIGURE 43: OUTPUT POWER VERSUS FREQUENCY .....	48
FIGURE 44: OUTPUT CURRENT VERSUS SWITCHING FREQUENCY FOR LOW-FREQUENCY AC OUTPUT .....	49
FIGURE 45: OUTPUT POWER VERSUS SWITCHING FREQUENCY FOR LOW-FREQUENCY AC OUTPUT.	49
FIGURE 46: ETO VOLTAGE (TOP) AND CURRENT (BOTTOM).....	50
FIGURE 47: THREE-PHASE OUTPUT CURRENTS .....	51
FIGURE 48: DSP AND INTERLOCK BOARD .....	52
FIGURE 49: COMPLETE ETO VOLTAGE SOURCE INVERTER SYSTEM.....	53
FIGURE 50: ANODE SHORT GTO STRUCTURE AND EQUIVALENT CIRCUIT.....	54
FIGURE 51: ANODE SHORT GTO EQUIVALENT REPRESENTATION.....	55
FIGURE 52: EQUIVALENT CIRCUIT OF THE ETO GATED 'ON' (LEFT) AND 'OFF' (RIGHT) .....	56
FIGURE 53: DIODE AND GTO REVERSE RECOVERY WAVEFORMS ( $V_{BUS}=200$ ) .....	57
FIGURE 54: DETAIL OF REVERSE RECOVERY OF GTO PARASITIC DIODE.....	57
FIGURE 55: REVERSE RECOVERY WITH SLOW DIODES ( $V_{BUS}=900$ ).....	58
FIGURE 56: ETO USING IGBT FOR GATE SWITCH .....	59
FIGURE 57: GCT CIRCUIT SHOWING PARASITIC DIODE.....	60
FIGURE 58: IGCT TWO-TRANSISTOR EQUIVALENT CIRCUIT .....	61
FIGURE 59: IGCT EQUIVALENT CIRCUIT AFTER RECOVERY OF NPN BEFORE RECOVERY OF PNP..	61
FIGURE 60: CIRCULATING CURRENT IN IGCT DUE TO NEGATIVE ANODE VOLTAGE .....	61

## Table of Figures

FIGURE 61: REVERSE RECOVERY OF THE ANTIPARALLEL DIODE DUE TO CIRCULATING CURRENT ..	62
FIGURE 62: ETO GATE DRIVER BLOCK DIAGRAM.....	63
FIGURE 63: GTO TURN-ON CURRENT REQUIREMENT .....	64
FIGURE 64: ETO DRIVER TIMING DIAGRAM .....	65
FIGURE 65: ETO AT THE UNITY GAIN POINT (LEFT) AND IN THE CURRENT TAIL (RIGHT).....	66
FIGURE 66: CLAMPED VOLTAGE COMPARED TO TURN-OFF CURRENT .....	68
FIGURE 67: DETAIL OF EMITTER SWITCH VOLTAGE DURING TURN-OFF TRANSIENT .....	68
FIGURE 68: NORMAL (ANODE SHORTED) ETO TURN-OFF .....	69
FIGURE 69: TRANSPARENT ANODE ETO TURN-OFF.....	69
FIGURE 70: VOLTAGE CLAMP SCHEMATIC.....	70
FIGURE 71: PULSE CURRENT SOURCE .....	71
FIGURE 72: ETO4060 AND 1 <sup>ST</sup> GENERATION GATE DRIVER .....	71
FIGURE 73: DOUBLE-PRIMARY FLYBACK CONVERTER .....	72
FIGURE 74: NEWER DESIGN ETO GATE DRIVER WITH ONBOARD POWER SUPPLY .....	73
FIGURE 75: DIMENSIONS OF THE NEW GATE DRIVER (IN INCHES) .....	73
FIGURE 76: 300V, 50 kHz INVERTER.....	74
FIGURE 77: GATE DRIVER INVERTER HARDWARE.....	74
FIGURE 78: COMPLETE ETO GATE DRIVER SCHEMATIC .....	75
FIGURE 79: ARCP INVERTER WITH REVERSE-CONDUCTING IGCTs.....	77
FIGURE 80: QUASI-RESONANT DC-LINK 3-LEVEL INVERTER WITH REVERSE-CONDUCTING IGCTs	78
FIGURE 81: ZCT CIRCUIT CONSIDERED WITH ETOS (MAIN) AND IGBTs (AUXILIARY).....	79
FIGURE 82: ZCT CIRCUIT THEORETICAL WAVEFORMS.....	80
FIGURE 83: ZCT TOPOLOGICAL STATES DURING TURN-ON .....	82
FIGURE 84: ZCT TOPOLOGICAL STATES DURING TURN-OFF .....	84
FIGURE 85: ZCT TEST SETUP .....	87
FIGURE 86: PHOTOGRAPH OF ZCT TEST SETUP .....	87
FIGURE 87: RESONANT CAPACITOR AND INDUCTOR.....	88
FIGURE 88: RESONANT TANK WAVEFORMS .....	89
FIGURE 89: MAIN SWITCH TURN-ON WAVEFORMS.....	89
FIGURE 90: MAIN SWITCH TURN-OFF WAVEFORMS .....	90
FIGURE 91: MAIN DIODE TURN-ON WAVEFORMS.....	91

Table of Figures

FIGURE 92: MAIN DIODE TURN-OFF WAVEFORMS..... 92

FIGURE 93: REVERSE RECOVERY PROCESS FOR MAIN DIODE ..... 93

FIGURE 94: DIODE RECOVERY TRENDS AS CONTROL TIMING DECREASES (L TO R)..... 93

FIGURE 95: BOTTOM (TURN-OFF) AUXILIARY SWITCH WAVEFORMS ..... 94

FIGURE 96: TOP (TURN-ON) AUXILIARY SWITCH WAVEFORMS ..... 95

## Chapter 1 - Introduction

The modern world is steadily becoming more and more reliant on high technology electronics and computers, which has led to a dramatic increase in the amount of power that is processed by power electronic converters. Although the majority of the power electronic converters in the world today by volume are in the low or medium power range, a significant amount of power is processed by a smaller number of very high power level converters. This trend will increase with the deregulation of the electric power industry, as the grid becomes full of interconnections between the numerous small suppliers rather than a few large utilities. The main uses of high-power converters can be considered mainly to be either utility applications or motor drives, with only a few specialized applications, which are usually military in nature, falling outside of these two categories.

### **1.1 Utility Applications**

The deregulated power system which is currently beginning to take form will require many high-power, high-performance power electronic systems. Distributed generation, with technologies including but not limited to windmills, photovoltaics, and microturbines, will require many multi-megawatt converters to interface these small localized generation sources to the grid. Many distributed generation technologies generate power in the form of DC such as photovoltaics, or variable voltage and variable frequency AC, since the wind can not be easily regulated to control the speed of a windmill. However, the electric power grid is fixed voltage, fixed frequency AC, so power conversion technology must be used in order for this technology to be effective.

In addition, increased demands on the utilities due to the sensitivity of high technology industries to power quality will require high-power converters to serve as filters and compensators on the grid. Semiconductor fabrication is particularly sensitive to power quality, where any problems with the incoming power can disrupt the process. Obviously this will become worse as finer pitch chips are made and the load on the utility increases, so the power quality is becoming a significant issue.

The summer of 2000 saw many customers in California suffer brownouts and extremely high energy prices due to excessive draw on the grid during the days. Energy storage technology can help alleviate this problem. The concept is essentially to store energy at night when the generators are running with excess capacity available, and to release the energy during the day when the load exceeds the capacity of the generation. This allows for more efficient use of the generation equipment, so it can generate at the same capacity all the time, but requires significant efforts in both the method of storing the energy and the Power Conversion System (PCS) interfacing the storage system to the grid. Examples of energy storage systems include pumped water, conventional batteries, flow batteries, Superconducting Magnetic Energy Storage (SMES), flywheels, capacitors, ultracapacitors, fuel cells, and many more are being developed constantly. The energy storage field is growing quickly and will require good power electronics in order to become practical.

High Voltage DC (HVDC) transmission, used to transmit large amounts of power over long distances with low losses, requires power electronic converters to interface the DC transmission line to the AC grid. Conventional HVDC DC-AC inverters have been line-commutated thyristor inverters, which have very high power ratings (up to several gigawatts) but produce very poor AC waveforms. Therefore bulky and expensive passive filters are used in order to clean the power they provide, but this technique is far from optimal. Ideally a high-frequency inverter would be used which would require almost no filtering in order to produce good quality.

### **1.2 Motor Drives**

Motor drives are being built in always escalating horsepower ratings, and with increased performance requirements. Many pieces of heavy machinery which have been conventionally Diesel based are becoming Diesel-electric, where the engine runs a generator and the motors do the direct work. This allows the use of an engine run at a constant speed where it can be well optimized. Also many ships of the future will rely on electric main drives rather than the conventional steam turbines. The use of electric drives means that there is no need to put a

turbine in the bottom of the ship directly in line with the propeller shaft, which requires enormous space to be consumed by the ductwork and steam lines. If the turbine only provides electric power generation rather than direct propulsion, the turbine and reactor can be placed anywhere in the ship. However, very good reliable power electronics are necessary for the ship's motor drive.

Industrial motor drives are currently the most common high power electronics being used. These motor drives are in the range of 1000 to 20000 horsepower currently, and are facing increasing performance requirements. The output current to the motor must be as clean as possible to ensure smooth operation of the motor without torque ripples, and to minimize heating in the motor. The input to the motor drive also must be clean, in order to not contaminate the power grid. This requires an active front-end for the drive, which will draw currents that are both sinusoidal, and in phase with the input voltage, in order to minimize circulating energy in the grid and to avoid voltage distortion which comes from harmonic currents.

### ***1.3 Other High Power Applications***

Some other applications require very high power converters. One of these that is receiving much attention from the military is electromagnetic launchers. These applications require enormously high pulsed power, with a much lower average value. These electromagnetic launchers are being considered for launching aircraft from carriers to replace the steam catapults in use now. Electromagnetic guns are also being considered, and may be used in the future.

### ***1.4 Challenges***

These are some of the applications which require high power, high performance power electronic converters. Current thyristor technology allows for adequate power ratings, but the performance is only marginally acceptable now and will need to be improved in the future. The solution is the use of high-frequency, Pulse Width Modulated (PWM) converters, identical in principle to the ubiquitous small power supplies found in most electronic equipment, but with much higher power ratings. Unfortunately, this was impossible until a few years ago, due to the

lack of a high-power, high-speed semiconductor switch. The conventional thyristor can be turned on by controls but cannot be forced to turn off by the gate, so it is immediately disqualified from use in PWM converters. The Gate Turn-Off (GTO) thyristor has high power capability as well and can be used for PWM converters, but the switching frequency cannot be made high enough to meet the performance requirements of the future. The power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and the Bipolar Junction Transistor (BJT) have the required controllability and good speed, but they are not even close to having the needed power capacity.

### ***1.5 Opportunities***

The prospects for high-power, high-frequency PWM converters have improved dramatically with the introduction of new power semiconductor devices. These new devices, including the Insulated Gate Bipolar Transistor (IGBT), the Integrated Gate Commutated Thyristor (IGCT), and the Emitter Turn-Off thyristor (ETO) have switching speeds similar to or better than those of a BJT, but with power ratings like the GTO. These devices also feature very good switching capability in that they can control a current level that is much higher than their normal operating current. With this new power semiconductor technology, work can begin on the high-power converters of the future.

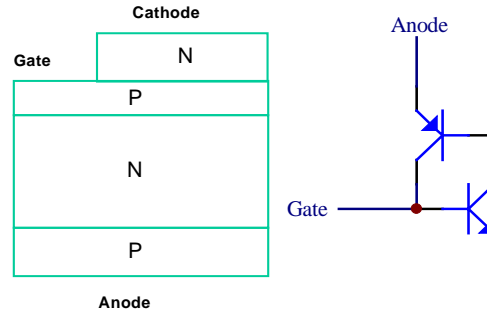


## Chapter 2 - High-Power, High-Speed Devices

### 2.1 *Device Technology Background*

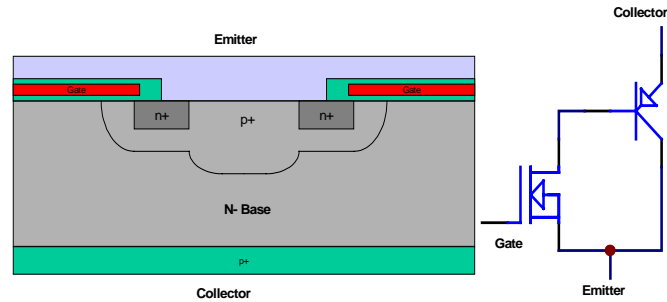
Conventionally for high power systems the Gate Turn-Off (GTO) thyristor has been the dominant fully controllable semiconductor switch due to its huge advantage over any other available device in terms of off-state voltage capability and on-state current capability. The Insulated Gate Bipolar Transistor (IGBT) has become extremely popular in medium power applications and the lower part of high power, especially when the voltage is relatively low (less than 1.5 kV). With the introduction of the High Voltage IGBT (HVIGBT), the IGBT is presenting a challenge to the dominance of the aging GTO even in the very high-power area.

The GTO thyristor is a four-layer semiconductor device of the structure PNPN, usually fabricated on a single die up to six inches in diameter. In the on-state it exhibits a latching behavior which enables it to achieve very low conduction loss at a high current density. Unfortunately, this latched state causes problems when the device turns off. This is because some parts of the die (cells) remain latched even when the anode voltage begins to rise, leading to a poor SOA (safe operating area). A bulky snubber capacitor, typically of a value between 2 and 6  $\mu\text{F}$ , is required to protect the GTO during the turn-off process. The discharge of this snubber requires significant power dissipation on a resistor or the use of complex energy recovery circuits, leading to increased system size and complexity. Additionally, the GTO requires a turn-on snubber to limit the current rise until the entire die has come into the conduction state, as well as to limit the recovery problem of the diode being commutated. Turning the GTO off requires a gate current equal to approximately 1/5 to 1/3 of the anode current which must be supplied for a long time by the gate driver[1].



**Figure 1: GTO structure and equivalent circuit**

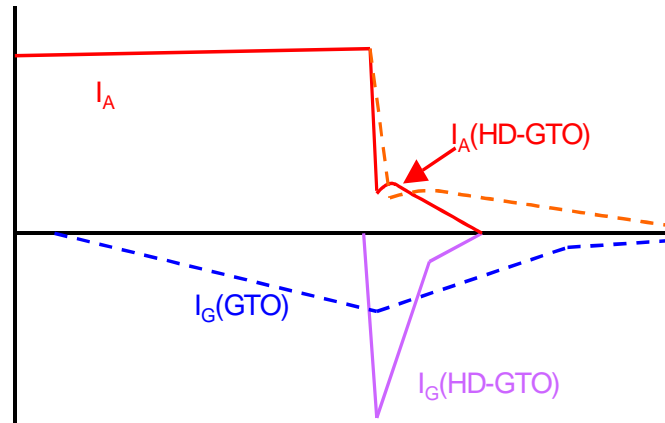
In contrast to the GTO, the IGBT is based on VLSI (very large scale integration) technology, giving much smaller cell sizes as well as smaller dies. The IGBT is essentially a MOSFET with an additional p-layer to improve the conduction loss by injecting minority carriers. The structure and the equivalent circuit of the IGBT are shown in figure 2. Because the IGBT is MOS-based, the gate is very easy to control by applying a voltage signal to charge the input capacitor of the IGBT. The switching performance of the IGBT is very good, and no snubbers are required for the IGBT. The IGBT behaves as an open-base PNP transistor after turn-off, which results in a current tail after the main current fall. The problems with IGBTs have been their relatively low blocking voltage and high conduction drops. New multi-die modules allow acceptable conduction loss by operating the IGBT at a low current density, which has allowed IGBT modules to be commercially built with 3300 V blocking capability. IGBT modules with 6500 V ratings have been developed and are expected to become commercially available soon [11]. However, these new 6.5 kV IGBTs have only 600 Amp ratings, so the power handling capability is almost the same as the existing 1200A/ 3300V devices. Conduction loss for the 6.5kV IGBTs is about twice as high as for 3.3kV at the same current density. Preliminary test results indicate that the overall system efficiency using two 600 A/ 6.5kV HVIGBTs in parallel can result in higher system efficiency than two 1200 A/ 3.3 kV HVIGBTs in series.



**Figure 2: IGBT cell structure and equivalent circuit**

The IGBT technology has much better switching performance than a traditional GTO. However, the switching performance of a GTO can be dramatically improved by driving the gate current to be greater than or equal to the anode current during turn-off. In this condition, referred to as unity-gain or hard-driven, the upper NPN transistor turns off very quickly while the GTO is still in the conduction state. If this transistor is completely off before the PNP portion of the thyristor turns off then there is no positive feedback loop present during the voltage rise phase. The PNP transistor with the base open is very robust, especially compared to the latched turn-off of a GTO. The GTO's latch is the reason it requires a  $dV/dt$  snubber, so the removal of the latching effect during turn-off also eliminates the need for this snubber. When the unity gain condition is satisfied the current distribution is very uniform across the entire die during the turn-off transient. This gives a much larger RBSOA than the GTO has. Typical turn-off waveforms for conventional GTOs and hard-driven GTOs are shown in Figure 3.

In a hard-driven GTO, the need for a high turn-off current capability requires a gate driver with a low impedance connection to the semiconductor device. This same low impedance path can be used to enhance the turn-on performance by injecting a large initial current into the gate, which initiates the latching effect. If the gate current  $dI/dt$  is high enough, then the thyristor can survive a very large anode current  $dI/dt$  at turn-on. However, the existing high voltage diodes cannot survive turning off with such a high  $dI/dt$ , so the speed of turn-on of the switch is limited by the diode's turn-off speed. A  $dI/dt$  snubber is typically used to control the diode's turn-off  $dI/dt$ , which also reduces the switch's turn-on loss to about 10% or less of the turn-off loss.



**Figure 3: GTO and hard-driven GTO gating**

Two methods have been demonstrated for the implementation of a hard-driven GTO. The first way is to hold the gate loop inductance low enough (3 nH) that a DC voltage less than the breakdown voltage of the gate-cathode junction (18-22 V) can generate a slew rate of 6 kA / $\mu$ s. This approach is used in the IGCT/GCT [2,3] (IGCT is ABB's product, GCT is Mitsubishi's, but the concept is the same), where a special low-inductance GTO housing and a carefully designed driver meet this requirement. The power consumption by the GCT driver is greatly reduced compared to that of a conventional GTO driver, since the gate current is present for a much shorter period of time [2]. IGCTs are currently available in 4.5 kV and 6 kV ratings, and a 10 kV IGCT is planned for the future [21].

The method to achieve unity gain used in the ETO thyristor [4] is to insert an additional switch in series with the cathode of the GTO. The cathode of the GTO is the emitter of the internal NPN transistor, so the series switch is referred to as the emitter switch. Turning off this switch applies a high transient voltage long enough to commutate the current even with a higher parasitic inductance present. Due to this higher tolerance for parasitic inductance, conventional GTOs can be used in the ETO. An additional switch is connected to the gate of the GTO, and is complementary to the emitter switch. These switches are implemented with many paralleled low-voltage, high-current MOSFETs, which minimizes the additional conduction loss due to the emitter switch. The typical value for the conduction

loss due to the series switch is 0.2 Volts at the GTO's average current rating. The turn-off driving power for the ETO is negligible, since the turn-off is purely due to the removal of a MOSFET gate signal. Figure 4 shows the current commutation circuits for the conventional GTO, the IGCT, and the ETO.

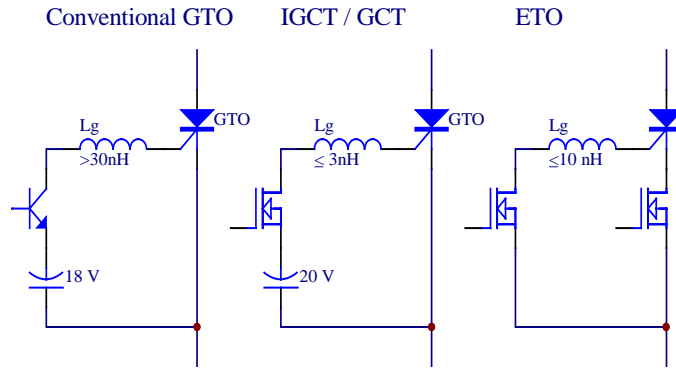


Figure 4: GTO, IGCT, and ETO gate loops

## 2.2 Pulse Tester Used for Characterization

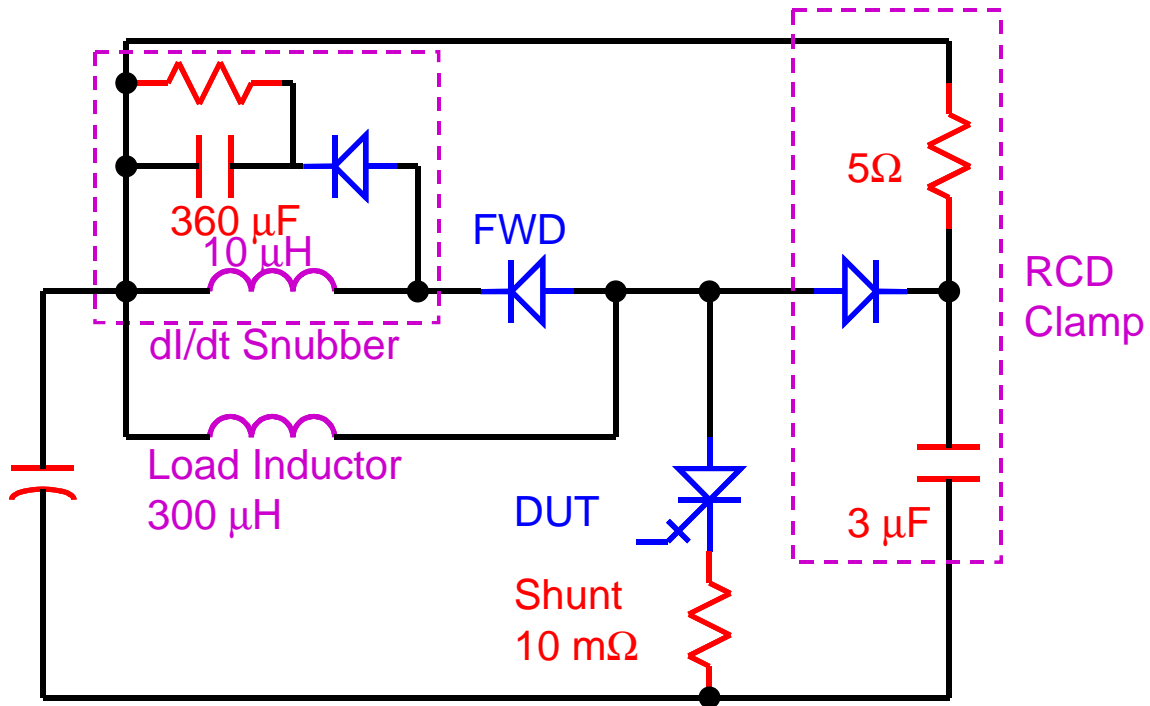
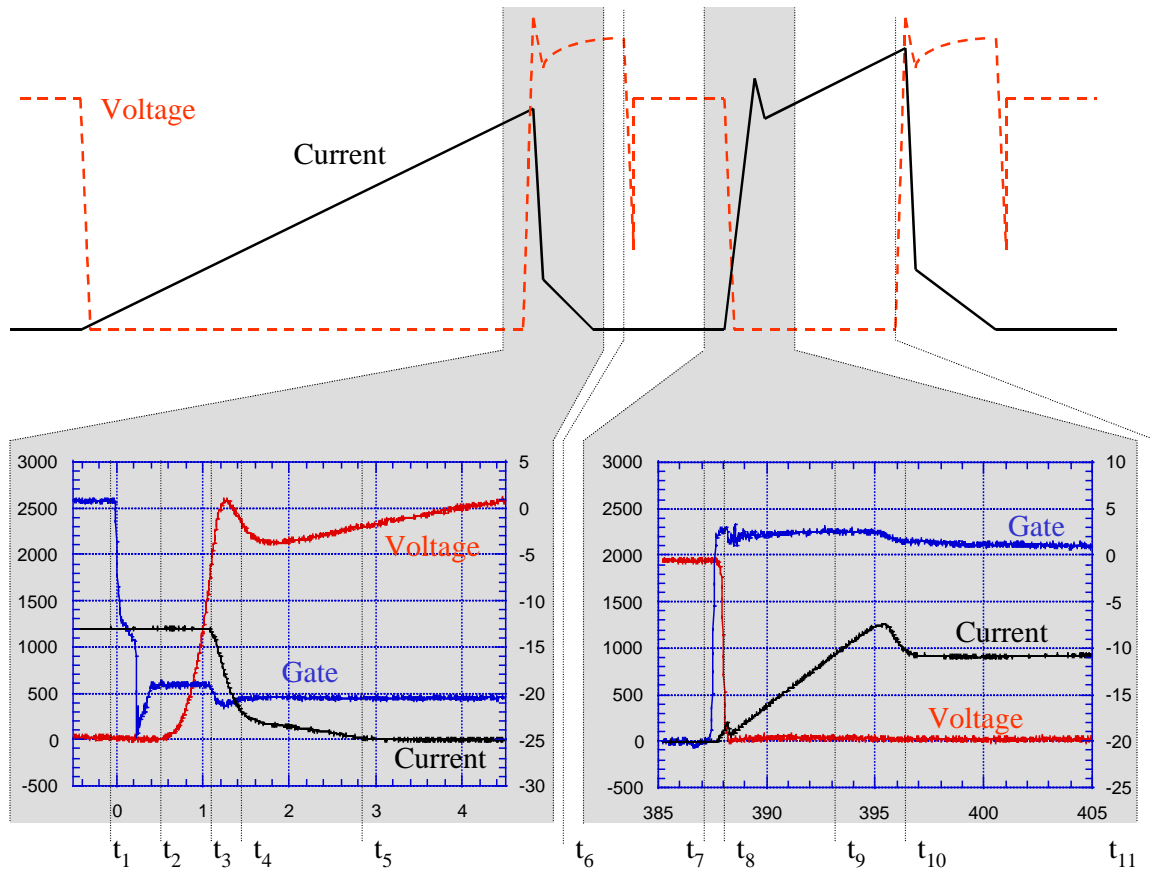


Figure 5: Pulse tester schematic diagram



**Figure 6: Double-pulse tester waveforms**

In the typical test, the Device Under Test (DUT) is initially off, and the high voltage capacitor bank is charged to set the voltage the DUT will experience during switching. As shown in Figure 6, the double-pulse test consists of the following events:

- $t_0$ – $t_1$ : At time  $t_0$ , the control system initiates a pulse to the gate driver for the DUT. The DUT turns on and the high voltage capacitor bank charges the load inductor. After the current reaches the desired value at  $t_1$ , the DUT's gate driver is commanded to turn off.
- $t_1$ – $t_2$ : From the time  $t_1$  until  $t_2$ , no changes to the device are seen. During this time, referred to as the storage time, internal processes in the device initiate the turn-off process.
- $t_2$ – $t_3$ : At time  $t_2$ , the anode voltage begins to rise, as the turn-off process has begun. The free-wheeling diode is still reverse biased so the current cannot begin to fall yet.

## Chapter 2 – High-Power, High-Speed Devices

- $t_3$ - $t_4$ : At time  $t_3$ , the anode voltage reaches the bus voltage and the main device current begins to fall. The current that had been flowing through the DUT is commutated into the free-wheeling diode. This is the highest stress interval of the turn-off transition, as the current and voltage are simultaneously high during this interval
- $t_4$ - $t_5$ : At time  $t_4$  the main current fall is completed and the current tail phase begins. The current tail continues until  $t_5$ . At this point the device can be said to have completed the turn-off process.
- $t_5$ - $t_6$ : During this time the  $di/dt$  snubber resistor carries the current, inducing additional voltage stress on the main DUT. The snubber inductor is charging during this time, and becomes charged at  $t_6$ . The snubber diode then goes through a reverse-recovery process.
- $t_6$ - $t_7$ : During this time the DUT is off and blocking a voltage equal to the input capacitor voltage. The current is still free-wheeling through the load inductor and the free-wheeling diode. This current will continue to circulate for a long time as the only energy dissipation is due to the conduction voltage of the free-wheeling diode.
- $t_7$ - $t_8$ : At this time the controller initiates the second pulse in order to test the turn-on of the device. Nothing external happens until  $t_8$ , which is the end of the turn-on delay time.
- $T_8$ - $t_9$ : During this time the load current begins to commutate into the DUT from the free-wheeling diode. The  $di/dt$  snubber inductor determines the rate of current transfer.
- $T_9$ - $t_{10}$ : At the time  $t_9$  the load inductor current is completely commutated into the DUT and out of the free-wheeling diode. The free-wheeling diode undergoes reverse recovery during this period and releases a significant amount of reverse current into the DUT. It is important that the DUT must have fully switched on by now or the diode recovery current will induce large power loss.
- $T_{10}$ - $t_{11}$ : During this time the device is on and the current is rising due to the input voltage divided by the load inductance. This is equivalent to the interval  $t_0$ - $t_1$  from the first pulse. The same sequence will continue for the second pulse's turn-off as from the first pulse.

The current through the device under test is measured with a precision current shunt in series with the cathode (or emitter for an IGBT). All delay times are defined with respect to the actual gate of the device, so gate driver internal delays are not included. Conventionally fall time is defined as when the current decreases from 90% of its initial value to 10%, but a different definition is used here. For the high voltage devices, the current tail value can be greater than 10% of the initial current value, so it is unreasonable to include this time in the fall time. Therefore the definition used here is that the fall time ends and the tail time begins when the current slope visibly changes. This is physically justified because for all three devices the current tail means that the main turn-off process is complete and the open base PNP transistor is removing remaining carriers. A sample waveform is shown in Figure 7. Current tail time is defined from the end of the current fall time until the anode/collector current decreases to 1% of the initial current.

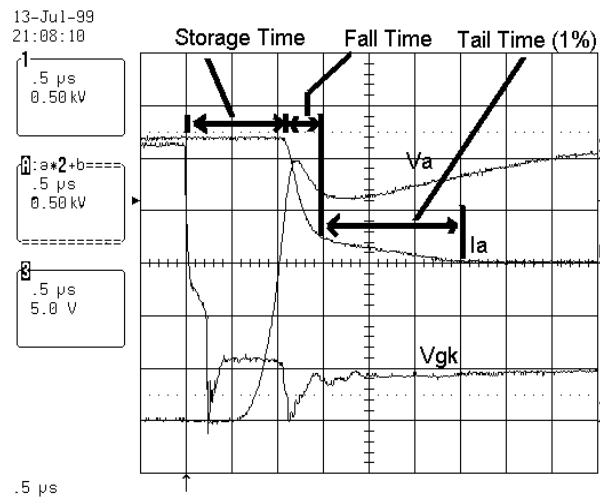


Figure 7: Switching time definition waveform

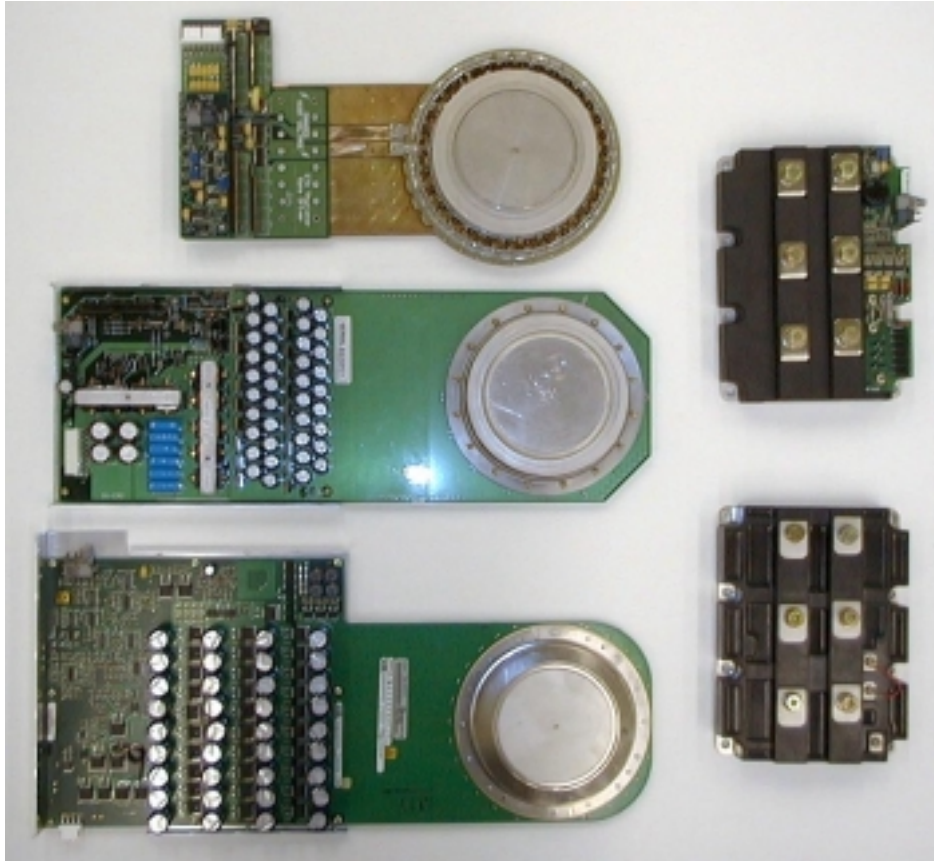
### 2.3 Devices Used for Comparison

To compare these various semiconductor technologies, two IGBTs, an IGCT, a GCT, and three ETOs were used [12]. One IGBT and the GCT are made by Mitsubishi, and the ETOs are developed at CPES. The other IGBT is made by EUPEC, and the IGCT is from ABB. The IGBTs, CM1200HA-66H and FZ1200R33KF2, are rated for 1200 A (DC) and 3300 V, and are packaged in plastic modules 14 cm by 19 cm in size. The IGCT and the GCT are both 4500 Volt devices which are rated for 4000 Amps maximum controllable



current. The first ETO used, ETO4060s, is rated for 6000 V and 4000 A controllable current, and is based on a Toshiba GTO. The IGCT, the GCT, and the ETO4060s are packaged in 93 mm press-packs, and with gate drivers have a maximum width of around 20 cm. The second ETO used, ETO1045s, is a small (53 mm) device rated for 4500 Volts and 1000 Amps. This ETO is based on a Westcode GTO. The ETO1045s is obviously of a lower rating than the GCT and IGCT, but it is using a fast conventional GTO, where the ETO4060s is based on a GTO designed for about 300 Hz. One final device used is a newly designed ETO, the ETO4045A, which is based on an ABB GTO similar to the thyristor used in the IGCT. The average current ratings for the IGCT, GCT, ETO4045A, and ETO4060s are 1200 Amps, while the ETO1045 is suitable for about 450 Amps average. When the IGBT's switching losses and a safe temperature margin are considered, the average operating current for this device should be between 600 and 800 Amps. A photograph showing most of the devices tested is shown in Figure 8.

One significant difficulty in comparing this type of device is that the ratings, and even the ratings system, are different for the different devices. For GTO-based devices, the current ratings are the peak controllable current, while IGBTs use a DC current rating. The IGBTs being tested have a controllable current rating of twice the DC rating, which translates to a 2400 Amp rating in the GTO system. These IGBTs consist of many small dies in parallel, giving a net current density much smaller than that of the GTO based devices. The RMS current for the IGCT, the GCT, and the ETO4045A is about 1800 Amps, and the RMS current rating of the ETO 4060 is about 1600 Amps, although the devices have the same average rating (1200 A) from the manufacturers.



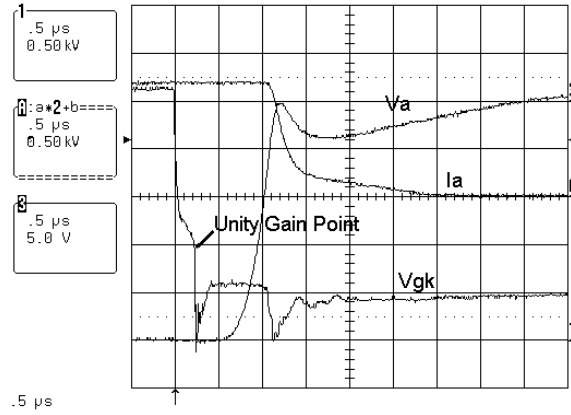
**Figure 8:** (clockwise from top left) ETO4060, EUPEC HVIGBT, Mitsubishi HVIGBT, ABB IGCT, Mitsubishi GCT

## **2.4 Unity Gain Verification**

Due to the strict requirements on the gate loop stray inductance for the IGCT and the ETO, it is very difficult to directly insert a current probe to monitor the gate current. Fortunately, the unity gain of the IGCT and the ETO can be verified by observing easily probed voltage signals. It is critical for the performance of these devices that unity gain has been achieved, so some effort is made to verify unity gain and predict the maximum current which can be turned off while maintaining the hard-driven condition.

In the case of the IGCT, monitoring the gate to cathode voltage at the terminals of the IGCT thyristor can show the unity gain. When the gate voltage becomes  $-20$  V, which is equal to the power supply in the gate driver, then clearly no voltage drop is occurring across the parasitic gate inductance. This in turn implies that  $dI_G/dt$  is zero, so the gate current has

completed commutation. A typical GCT waveform showing the gate voltage is shown in Figure 9. The inside of the GCT driver box is shown in Figure 10.



**Figure 9: GCT unity gain**



**Figure 10: Mitsubishi GCT gate driver**

Unity gain of the ETO can be verified by observing the drain to source voltage of the series switch. When the current is commutating, the voltage across this switch quickly rises to the breakdown voltage of the MOSFETs (60 V). When the voltage across this switch begins to fall, then the net cathode current of the GTO is negative which discharges the output capacitors of the MOSFETs. Therefore the ETO's unity gain corresponds to the falling edge of the emitter switch voltage. A turn-off waveform showing the ETO's emitter switch voltage is shown in 11.

Based on the unity gain observation, the rate of current commutation for the devices can be estimated by dividing the anode current by the time required for unity gain. This method yields a lower result than truly occurs because the total current commutated is slightly greater than the anode current due to a reverse recovery effect of the gate to cathode p-n junction. Even with this conservative estimation of the gate current's  $dI/dt$ , the GCT and the ETO are both capable of approximately 6000 A/ $\mu$ s commutation rate.

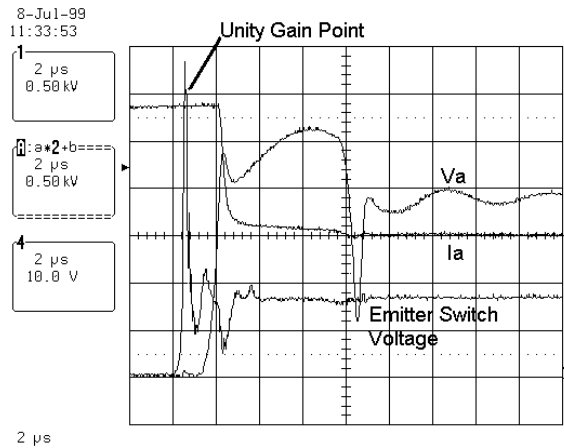


Figure 11: ETO4060 unity gain

## 2.5 Gate Drive Circuits

The performance of all semiconductor switches depends on the gate driver circuit. This is especially true for the GCT, where the device will be unable to operate in the snubberless mode if the gate driver is not drawing the gate current out fast enough to achieve unity gain. The drivers for the ETO and IGBT are less difficult to implement since the driver is not required to provide high current.

From a schematic point of view the GCT driver is very simple, consisting primarily of a capacitor bank and a switch made from many parallel MOSFETs. The PCB layout and component selection is critical due to the very strict stray inductance requirement imposed on the switching loop. Additionally there is a portion of the driver devoted to turning on the GCT. This is done by injecting a high current (200 A) pulse into the gate for 5  $\mu$ s and then injecting 10 Amps into the gate throughout the on-time. This part of the driver dissipates

significant power due to the linear transistors controlling the exact current level, but the implementation of this part of the gate driver is easy. The GCT driver contains minimum on-time and off-time protection in order to allow the device to always be in a uniform state prior to switching. No overcurrent protection is used for the GCT at the driver level. Although the total gating power is still very small compared to the main power, all of the gating power must be supplied by an external isolated supply which must have an isolation capability and  $dV/dt$  rejection to match that of the GCT.

Due to the different thyristor design used by ABB in the IGCT, the driving power for this device has been greatly reduced. This is accomplished by increasing the current gain of the thyristor so less gate current is required to maintain the on-state. This leads to a DC injection current of only 2 Amps. In addition, the IGCT driver uses a switching rather than linear circuit for pulse injection, which reduces losses as well.

For the ETO driver, three gates have to be controlled – the GTO's current injection, the emitter switch, and the gate switch. Fortunately the emitter switch and gate switch are easily controlled by using one inverting driver and one non-inverting driver controlled by the same input. The only function of the GTO gate is to inject the turn-on current just as in the case of the GCT. The ETO driver developed at CPES also contains minimum on-time and off-time protection. In addition, the emitter switch MOSFET can be used as a linear resistor to approximate the anode current, which can be used for on-driver overcurrent protection. Like the GCT driver, the ETO driver requires an external isolated power supply, although the power consumption is much lower. The development of the ETO's gate driver is detailed in chapter 6.

The IGBT driver is very easy to implement, since it has only a single MOS-gate to control. The peak gate current for the tested IGBT is about 10 Amps, which flows for about 2  $\mu$ s at every switching event. The IGBT driver can be used to actively control the  $dI/dt$  and  $dV/dt$  of the collector, but this feature was not implemented for this test. Information about active driver techniques can be found in many papers such as [5]. The IGBT driver implements an overcurrent protection by means of desaturation detection. IGBT drivers

consume so little power that commercial DC/DC converter modules can be used to internally provide the isolation for the high-side switch.

## 2.6 Forward Conduction Loss Characterization

The forward current versus voltage characteristics for all of these devices can be found easily. As can be seen from Figure 12, the thyristors have a clear advantage in conduction loss over the IGBT, even though their active die area is less than that of the IGBT. If the relationship between breakdown voltage and conduction loss is found, the advantage of the latching devices becomes even greater. The 4.5 kV thyristors have the lowest conduction loss, followed by the 6 kV thyristor, and then the IGBT are the worst even if the loss is not normalized to die area. ABB’s transparent anode and punch-through base design show an advantage in the forward conduction test, as the higher gain allows the device to latch into an extremely low loss conduction mode. This holds true for ABB’s own IGCT as well as the ETO4045A, which is based on an ABB GTO with the same transparent anode and punch-through base design.

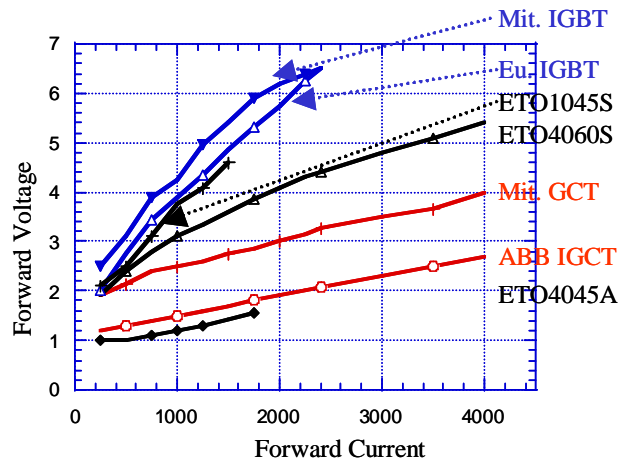
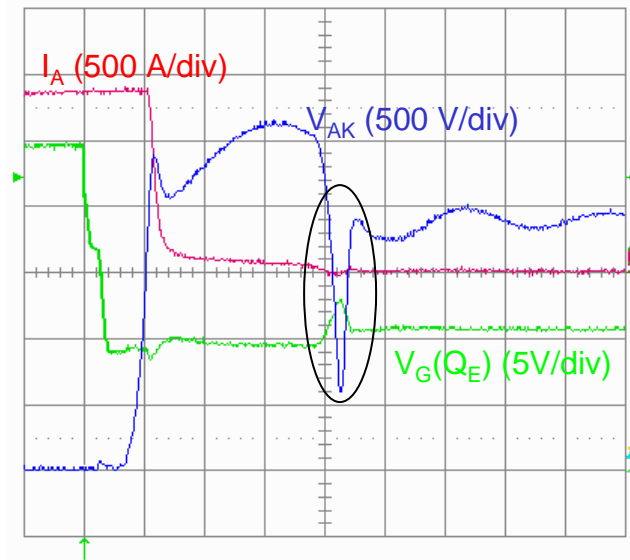


Figure 12: Forward conduction voltage

## 2.7 Switching Tests

Switching performance of high-power devices has been greatly enhanced by the hard-driven GTOs and the HVIGBTs appearing to challenge the slow GTO technology. Typical

operation frequencies of the high-power GTOs range from line frequency (50/60 Hz) to a high of about 500 Hz. In contrast, the HVIGBT can be operated at up to 1500 Hz, and the hard-driven GTOs can operate at 1 kHz or more. This increase in frequency leads to dramatically reduced filters and lower distortion in the typical inverter applications.



**Figure 13: Typical turn-off waveform**

To evaluate the performance of these devices, they were operated with DC voltages of 1.5 kV and 2 kV on the pulse tester without any turn-off snubbers. The limiting factor in the amount of current that could be switched off safely was the clamping diode used to limit the voltage spike on the switch. During reverse recovery, the voltage across this diode approaches its breakdown (4.5 kV) at the same time the anode (or collector for IGBTs) voltage of the device under test approaches zero, as circled in Figure 13. For the GCT and the ETOs, no reverse voltage was acceptable due to the lack of either reverse conduction capability (such as an anti-parallel diode) or reverse voltage blocking capability. GTO based devices can achieve reverse voltage blocking easily, but these tested GTOs are anode-short types, which trades away the reverse blocking capability for better switching performance, especially in the current tail phase. ABB's design uses a transparent anode rather than anode shorts, which also eliminates the reverse blocking capability. The transparent anode technology makes the current gain of the device change as a function of the current flowing so that it will have a high gain at low current and a lower gain at high current. The switching

losses for each device were calculated by first multiplying the voltage across the device by the current being conducted, and then integrating this instantaneous power during the switching time in order to find the switching loss. The results of the switching loss tests were compared for the IGBT, the GCT, and the ETOs. These results are shown for a 2kV bus in Figure 14.

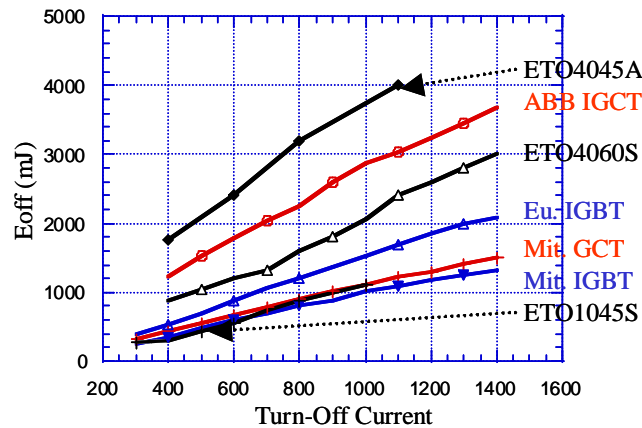


Figure 14: 2 kV snubberless switching loss

As expected, the IGBT holds the advantage in this test with the lowest turn-off loss overall. Surprisingly, the loss of the GCT and the ETO1045 is only marginally higher than the IGBT's loss. The IGBT's primary advantage in switching loss is in the initial voltage rising phase, which occurs much faster than in the thyristors. This is because the MOSFET channel in the IGBT can turn off faster than the NPN transistor in the GTOs, and the channel is better distributed through the IGBT than the GTOs' gates are. The amount of carriers stored in the GTOs is also higher than in the IGBT, resulting in slower  $dV/dt$ . It is not surprising that the ultra high voltage ETO4060 has significantly more switching loss than the lower voltage devices. The probable reasons for this device's high switching loss are a high carrier lifetime in the GTO, a strong PNP transistor which can maintain the current longer with the base open, and a GTO design optimized for low frequency, high power operation. The theory of hard-driven GTOs predicts no improvement in turn-off loss when compared to traditionally driven GTOs, only an improved safe operating area and higher speed. This shows that the GCT is very well optimized for performance as well as for a low internal inductance. The ABB IGCT's transparent anode proved a disadvantage in this test, as switching times and switching losses were noticeably worse than the anode shorted devices.



As can be seen in Figure 15 the switching times for all of these devices are short and very consistent. The ETOs and the GCT have long storage times at very low current levels, but the storage time is very consistent at 600 Amps and beyond. The current fall times for all devices characterized except the IGCT are around 250 ns and are essentially independent of the current being switched, as shown in Figure 16. The IGCT has a very long current fall time at low current levels, although the speed improves at higher currents. The IGCT tail has a very large magnitude, which again shows that the anode short structure of the GCT and the ETOs offers advantage in this area.

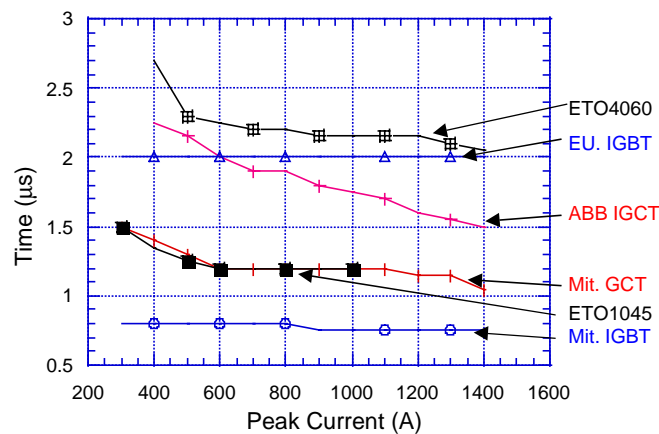


Figure 15: Storage (or delay) time comparison

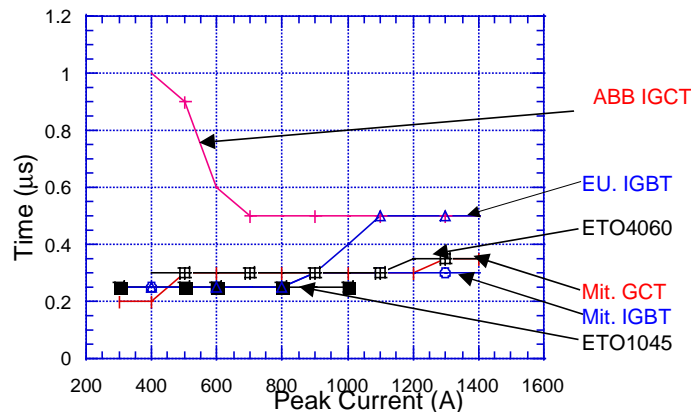


Figure 16: Fall time comparison

Due to the large (10 μH) turn-on inductor, the turn-on loss for all devices is negligible. All of the thyristors hold a very slight advantage over the IGBT in terms of voltage fall time at turn-on, but the current is so low during this time that there is no

significant difference in loss. It must be noted that the IGBT can be operated without the turn-on snubber at the expense of significantly increased switching loss, but doing so requires a more complex gate driver design. This is due to the IGBT's ability to control the exact collector current by operating in the linear region. The GCT completely lacks this operating mode. Theoretical analysis predicts the existence of this forward biased SOA for the ETO [4], but no experimental verification has been performed except at low current [15]. For current tail comparison, the tail current was examined on a very high resolution (10 A/div) in order to see all of the effects. Immediately after the main current fall, the tail current decreases rapidly for all of the devices tested. However, the current tail can take a long time to finish decreasing to zero after this initial fast fall. The detail of the GCT's current tail is shown in figure 15 after turning off 1200 Amps. The current tail can indicate the strength of the PNP transistor within an IGBT or a GTO. The long tail observed for the ETO4060 indicates a stronger PNP, which helps reduce the conduction losses. The GCT demonstrates the shortest current tail of all of the devices tested, which is further evidence of the very good internal design. The drawback of this performance is that the effective current gain of the GCT is reduced, thus requiring more DC gate current injection during conduction. The IGBT and the ETO1045 have only slightly worse current tails than the GCT.

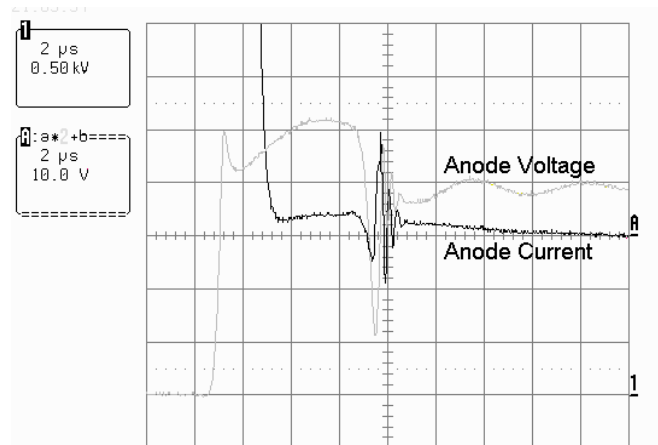


Figure 17: GCT current tail detail

Traditionally, the GTO switching frequencies were limited by the times required for the GTO to complete the switching transitions. In particular, a very long minimum off-time had to be observed due to some parts of the GTO remaining latched for more than 100  $\mu$ s. The devices tested here all have very fast switching times, but the switching loss is rather high due to the very large currents and voltages considered. Therefore, the switching frequency is thermally limited by the switching loss. Soft switching techniques may allow these devices to achieve much higher operating frequencies ( $\sim$ 10 kHz) if the switching loss can be reduced.

### *2.8 Discussion*

Packaging technology is very different for the IGBT modules compared to GTO packaging. The IGBT modules use many parallel dies, which are wirebonded and housed in a plastic module. Since a GTO can be fabricated on a single wafer, press-pack (“hockey-puck”) housings are utilized. The reliability record for the press-pack devices is much higher than wirebond modules, largely due to a better tolerance for thermal cycling. Additionally the press-pack allows double-sided cooling in order to lower the thermal impedance. However, the IGBT still achieves similar thermal impedance overall due to the much larger die area and the consequently large baseplate. The IGBT baseplate is electrically isolated from the heatsink, but the press-pack heatsinks are directly connected to the anode and cathode terminals. As a result liquid-cooled systems with press-pack devices must rely on oil or deionized water in order to prevent the coolant from conducting current. The main advantage of the IGBT module is its ease of use, with the isolated baseplate leading to easy heatsinking. The collector and emitter terminals are conveniently located for connection to a laminated busbar to reduce the parasitic inductance and hence the voltage spike. Additionally, the IGBT module does not require any external mechanical clamp for mounting as the press-pack housing requires. The press-pack’s reliability is a key issue and this package is preferred for many applications where long life is necessary.

Although failures are obviously unwanted, the characteristics of the device after a failure should be considered. This can make a big difference in how much damage is done to

the rest of a system and how difficult repair will be. After a failure, any of these devices will become short-circuited. The current will then increase until either all energy available has been consumed or an external circuit acts to stop the fault current. For the wirebond IGBT, all of the current will concentrate into the die that broke down. This will usually destroy the wirebonds for that die due to the huge current flowing. After failure the IGBT can become an open circuit. This is a very dangerous condition for series connected devices or multilevel converters, as the voltage will no longer be shared exposing the other devices in the chain to the risk of overvoltage [10]. The press-pack devices will remain shorted since the die is directly connected with the metal contacts. There is some concern about the wirebond MOSFETs in the ETO's emitter and gate switches, although no failure of these MOSFETs has been seen yet even after destruction of the GTO. Another issue related to the packaging is explosion damage. The press-pack is very strong and as a result explosions are very unlikely in this type of package. Plastic modules can easily shatter the housing which leads to damage to nearby components.

As previously mentioned, an IGBT can actively control the collector voltage and current during the switching events. This feature of the device can lead to reduced EMI as well as elimination of the  $di/dt$  (turn-on) snubber. However, elimination of this snubber in high power, quasi-zero impedance source (voltage-fed) converters may not be desirable due to the other benefits which the snubber offers. These include elimination of damage due to cross-conduction of bridge switches (“shoot-through”) or load short-circuiting, and improved fault management. If the rate of rise of current in a fault condition is controlled, a fast device such as the (IGCT, ETO, or IGBT can respond in time to turn off the fault current with the semiconductor switches. For GTO systems, the GTO could not respond in time to interrupt a fault current so the protection commonly used was to turn all of the bridge switches on and wait for fuses to open. The ability of the ETO and IGBT to automatically detect and respond to overcurrents enhances the safe operation of high power systems. In addition, the IGBT can self-limit the current which will be conducted, so operation within the device's switching capability can be insured. Thyristor devices will conduct an extremely high surge current that is much higher than their interrupting capability, which requires the control logic to prevent the devices from switching off during this time.

## **2.9 Comparison Conclusions**

As can be seen from the switching times, all of the devices tested here offer very fast switching times relative to their power ratings. In addition, even the worst conduction loss from the IGBT is still acceptable when compared to the blocking voltage. For very high power systems, the IGCT, the GCT, the ETO4045A, and the ETO4060s are capable of handling extremely high power levels. The GCT is very fast for its high rating, and the only drawback is the difficult to make gate driver and its power consumption. ABB's IGCT and the ETO4045A trade away switching loss to reduce driver power and conduction loss, so these devices are particularly suited to advanced topologies which reduce the necessary switching frequency or to soft-switching applications which can reduce the switching loss. The ETO4060 offers very high ratings with minimal driving power, although the switching is not quite as good as the GCT, although better than the IGCT. The IGBT offers the best switching speed and loss of any of the devices tested and the simplest drive. However, the GCT and small ETO are amazingly close to the IGBT in switching loss considering their latching nature and nearly 50% higher voltage rating. The performance of all devices tested here is very good, especially compared to the conventional GTO applications.

## Chapter 3 - ETO-based DC/DC Converter

### 3.1 Objective

Three-phase inverters are typical high power industry applications. A phase leg, composed of two switches and their anti-parallel diodes, is a standard building block for almost all high power (voltage-fed) topologies. As the initial step of building an ETO application system, a simple configuration of the ETO system that makes use of a phase leg is shown in Figure 20. This topology can be run in either a buck or a boost mode. However, the boost topology was selected in order to achieve a high voltage stress on the ETO without using a high voltage power supply.

This phase leg was constructed using the smallest ETO developed, ETO1045HS, which has a maximum snubberless turn-off capability of 1000A. However, limited mainly by thermal capabilities, this device is capable of 300-400A average current and can work at a bus voltage up to 3000V with a switching frequency of 1 kHz under the double-sided cooling condition.

### 3.2 ETO1045HS Characteristics

The system was designed based on ETO1045HS, a 4.5kV/1.0kA hard switching ETO as shown in Figure 18. The snubberless turn-off capability of ETO1045HS has been verified at up to 2.5 MW of instant power dissipation in the ETO during the turn-off transient [14]. A typical hard switching waveform is shown in Figure 19. The snubberless switching shows only a slight increase in turn-off switching loss compared to that with a 2 $\mu$ F dV/dt snubber, and shows a dramatic decrease in turn-on loss due to the lack of discharge current from the dV/dt snubber during the voltage fall time. The overall switching loss is reduced when operating in the snubberless condition. At elevated temperature, the GTO is much slower than at room temperature so the switching loss increases.



Figure 18: Picture of ETO1045HS

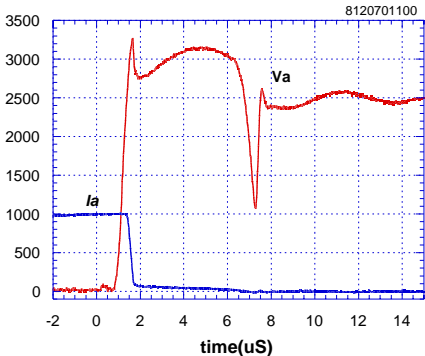


Figure 19: ETO1045HS hard turn-off at 1kA, 3.3 kV

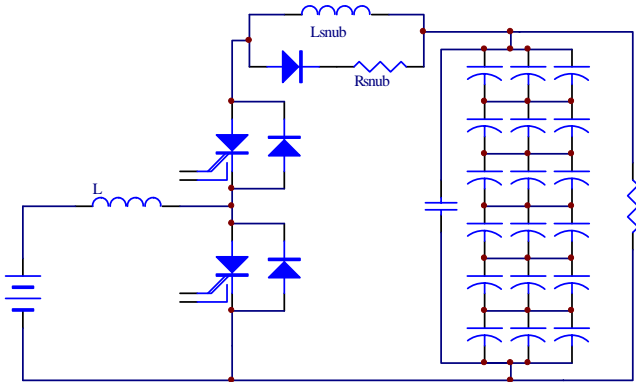


Figure 20: Boost converter based on a standard phase leg.

### 3.3 ETO Phase Leg Design

The first necessity in order to build a high-power converter from the ETO was to develop a phase leg (half-bridge) based on two ETOs, two diodes, the gate drivers and

suitable heatsinks. The ETOs used are ETO1045HS, which are rated for 1000 Amps maximum turn-off current and 4500 Volts blocking. The ETO1045HS is a 53 mm die device based around Westcode’s GTO WG10045S, so a 53 mm diode was chosen to simplify mechanical construction. The selected diode, SM45CXC624, is a fast-recovery type 4500 volt diode from Westcode also. The ETOs and the diodes are in press-pack (“hockey-puck”) packages, so a mechanical clamp is necessary in order to use these packages. The phase leg uses liquid cooled heatsinks and a matching clamp. The phase leg includes five water-cooled heatsinks so each device is double-sided cooled. Due to the fact that the switches will be dissipating more power than the diodes, the design was made to keep the two ETOs separated from each other. Another requirement for the design of the phase leg is that the path from each ETO to the opposite diode should be the same in order to equalize the voltage spike on the switches. The design of the phase leg is shown in Figure 21, and the completed phase leg is shown in Figure 22.

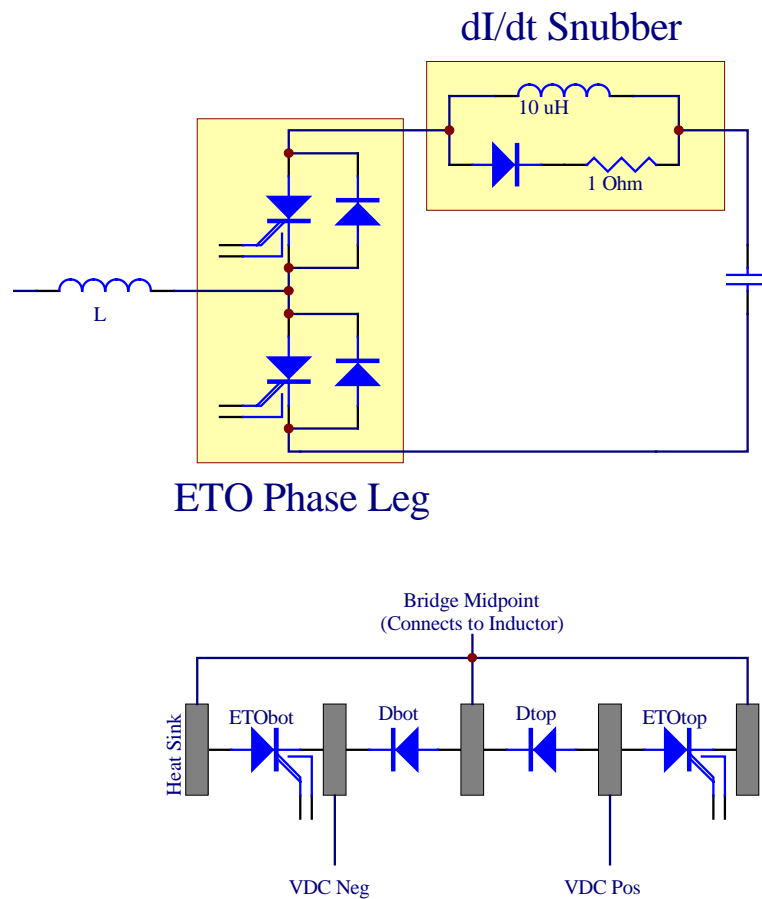
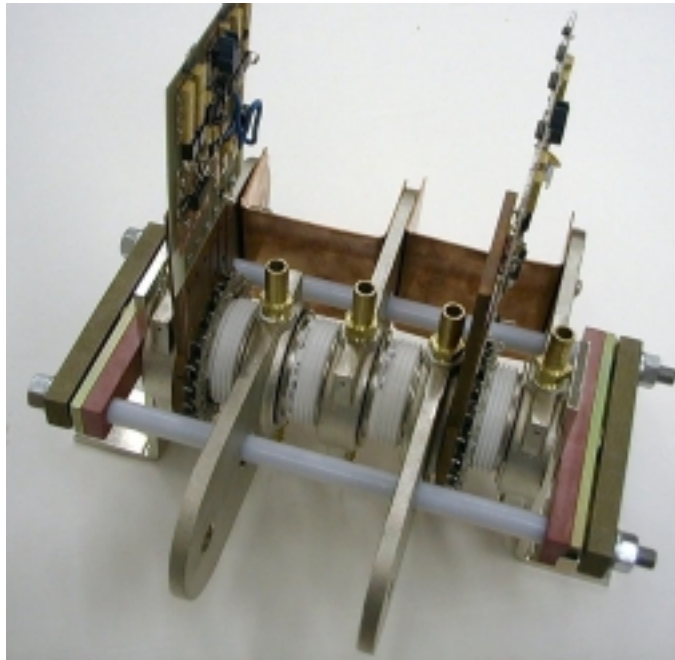


Figure 21: ETO phase leg design.





**Figure 22: Photograph of completed phase leg**

### ***3.4 DC Bus Design***

High voltage systems require considerable effort in the bus design in order to reduce the stray inductance without causing insulation failure. The conventional laminated buses used in low voltage (<1 kV) applications are not suitable in high voltage due to partial discharge in any bubbles in the laminating film. A different type of insulation is required in this application, so an epoxy laminate was chosen due to its high dielectric strength, high mechanical strength, and high temperature capability. Due to the high voltage considerations, each connector going to the back layer of the bus is enclosed in an insulator rather than relying on the insulation capability of air in this portion. The DC insulation capability of the bus has been tested to be at least 8000 V. A photograph of the completed DC bus with one layer of insulation removed can be seen in Figure 23.

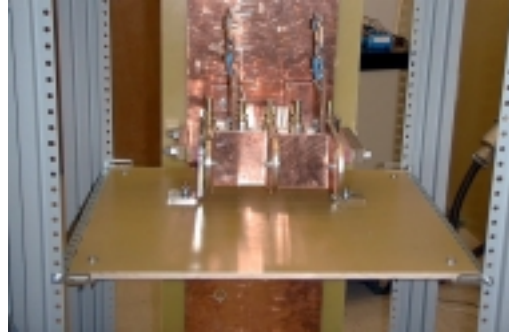


Figure 23: DC bus shown with phase leg installed

### 3.5 *dI/dt Snubber Design*

Although the ETOs have a snubberless turn-off capability, the diodes do not. Therefore a  $dI/dt$  snubber is needed to prevent diode failure. This snubber also greatly reduces turn-on switching loss in the ETOs, and the snubber protects the phase leg from damage due to “shoot through” when both the top and bottom switches are on simultaneously. Shoot-through is a common problem when a switch turns on with a very high  $dV/dt$ , and the noise induced causes a false triggering of the logic in the other switch’s gate driver. The value of the snubber inductance is easily found from the DC bus voltage and the desired  $dI/dt$ , which is determined by the characteristics of the diode employed. After the inductance is designed, the snubber resistance is chosen from a tradeoff analysis.

$$L = \frac{V_{dc}}{dI/dt} \quad 3-1$$

$$\tau = \frac{L}{R} \quad 3-2$$

$$V_{pk} = V_{dc} + I * R \quad 3-3$$

For high frequency operation, a short time constant of the snubber is required. However, a short time constant demands a large resistor, which increases the voltage stress on the switch. The snubber resistor must be selected based on the relative demands of time constant and voltage stress. For this converter, a snubber inductance of 20  $\mu\text{H}$  was selected, in order to maintain the  $dI/dt$  to 100  $\text{A}/\mu\text{s}$  under a 2 kV bus. With the 20  $\mu\text{H}$  inductor, a

resistor of 2.5 Ohms was selected in order to give a time constant of 8  $\mu$ s. With 300 Amps of peak current, the maximum possible additional voltage stress is 750 Volts.

### **3.6 System Construction**

Using the laminated bus and the ETO phase leg, a DC/DC boost converter has been built. It uses the bottom switch of the phase leg and the top switch is always gated off. The cooling system for the boost converter uses deionized water with the resistivity maintained above 1 Megohm-cm. The converter operates at 1 to 2 kHz.



**Figure 24: An overall view of the converter**

### **3.7 System Performance**

The operating waveforms for the 100 kW test are shown in Figure 25, Figure 26, and Figure 27. The stress on the ETO was 120 Amps switching current and 2000 Volts DC (with 2250 Volts peak spike). Figure 11 shows the voltage spike on the device during turn-off transient. Because of the well-designed laminated bus, the stray inductance among the phase, di/dt snubber and the output capacitor is very low so that the voltage spike during the turn-off transient is very low, about 200V above the DC link voltage. The over-voltage due to the di/dt snubber is about 250V, which is reasonable compared to the DC link.

### 3.8 Thermal Performance

The ETO showed very little thermal stress in this test. With the cooling water maintained at 27 °C, the case of the GTO thyristor in the ETO had reached a temperature of 34 °C, and the small MOSFETs had reached a case temperature of 30 °C. Thermal modeling of the ETO is necessary to translate the case temperature to the junction temperature, but case temperatures this low mean that the silicon die is also quite cool. The maximum allowed switch current is about 400 Amps RMS at 1kHz switching and the maximum safe operating voltage is 3000 Volts DC. Therefore, the expected power capability for this boost converter is about 600 kW, assuming a boost ratio of 1 to 2 with 1500 Volts and 400 Amps input.

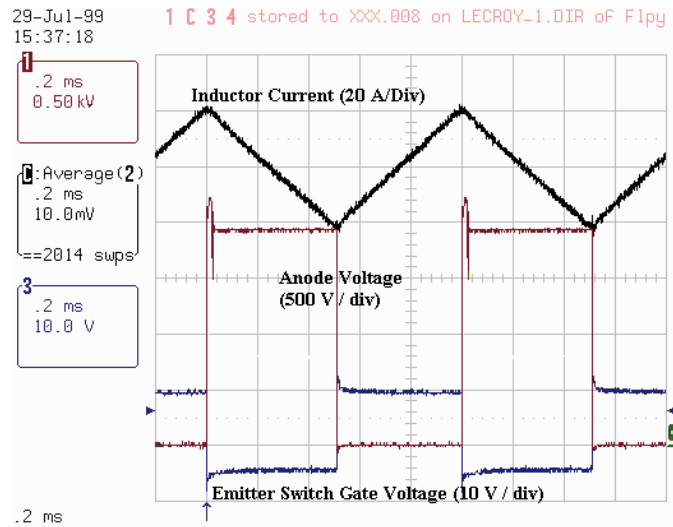


Figure 25: Waveforms of ETO boost converter running at 100kW

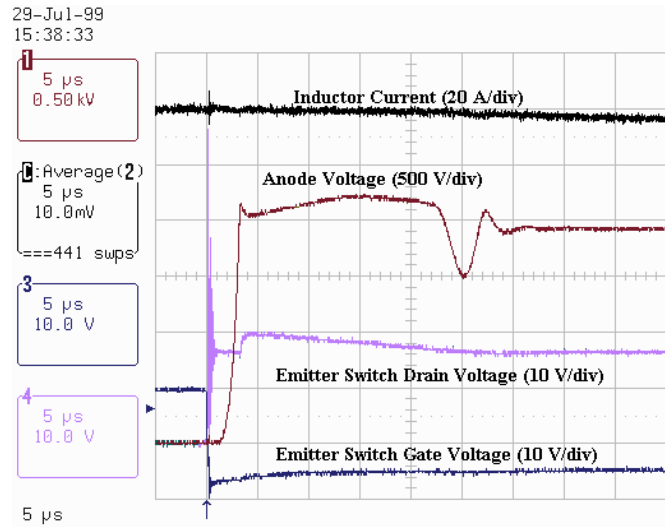


Figure 26: Voltage stress during device turn-off at 100kW

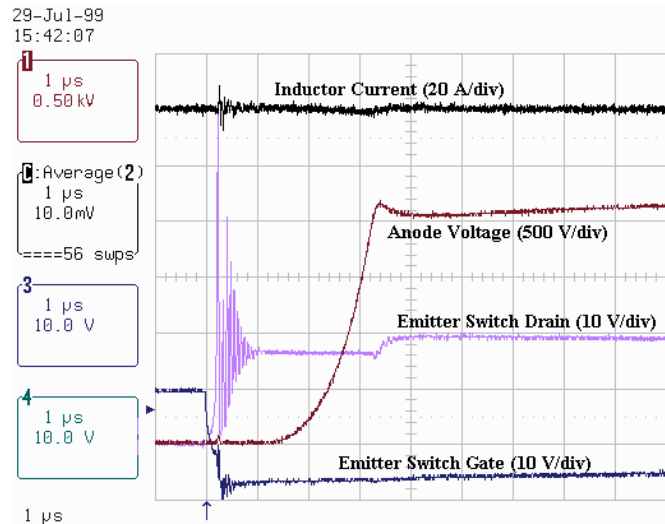


Figure 27: Detail of the turn-off transient

### 3.9 Buck Mode Testing

After the successful testing of the ETO converter in the boost topology, the converter was turned around in order to operate as a buck converter. Although the voltage stress on the switch is low in buck mode, the current stress is increased. Additionally, the isolated power supply for the gate driver can be tested because the cathode of the top switch is not grounded like the boost switch is. The converter was run in buck mode with 1000 V/100 A input and 550 V/ 180 A output as shown in Figure 28 and Figure 29. Testing of the converter in buck mode showed that the turn-off time of the ETO was greatly reduced due to the higher

operating current, as shown in Figure 29. There are several reasons for this phenomenon, which is also exhibited by IGCTs[8]. One is because the GTO's junction capacitance is significant, and the higher operating current can charge this capacitance more quickly during the voltage rising phase. Also, the open base PNP transistor which appears during the turn-off transient[1] can sustain a low current for a long time compared to the time it can sustain a higher current. The buck mode test showed the performance of the top switch while the boost mode test showed the bottom switch, so the phase leg has been tested. The next logical step is to utilize both switches in an inverter.

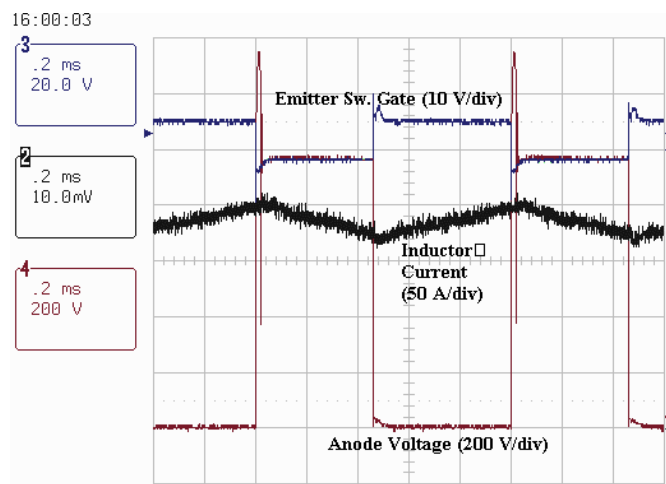


Figure 28: Buck mode PWM waveforms

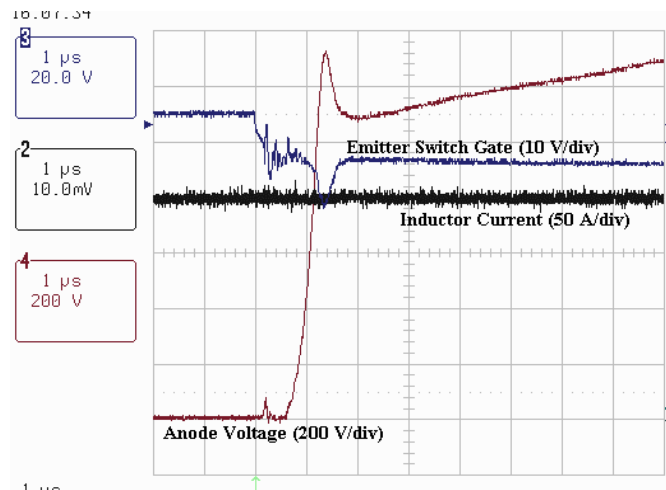


Figure 29: Detail of the buck mode turn-off transient

### **3.10 DC/DC Converter Conclusions**

The ETO based boost converter has been built and tested at the 100kW level, with a switch stress of 120A/2250V. The system exhibits a high operating frequency for thyristors at 1kHz, good thermal management, snubberless turn-off capability as well as ease of control. The saving on the system passive components is obvious. No dv/dt snubber is required, and higher operating frequency also reduces filter inductor and capacitor size in the system. By eliminating the dv/dt snubber, the phase leg can be more compact, so the stray inductance can be minimized which in return reduces the voltage stress on the switch.

## Chapter 4 - ETO Based Three-Phase Inverter

### 4.1 System Configuration

Three-phase inverters are typical high power industry applications. A phase leg, composed of two switches and their anti-parallel diodes, is a standard building block for almost all high power (voltage-fed) topologies. A diagram of the ETO inverter which was developed is shown in Figure 30. The phase leg was constructed using the smallest ETO developed, ETO1045HS, which has a maximum snubberless turn-off capability of 1000A. However, limited mainly by thermal capabilities, this device is capable of 300-400A average current and can work at a bus voltage up to 3000V with a switching frequency over 1 kHz under the double side cooling condition. For this inverter, the switching frequency was raised to 1.5 kHz which is enough to give high quality output waveforms without overly stressing the device.

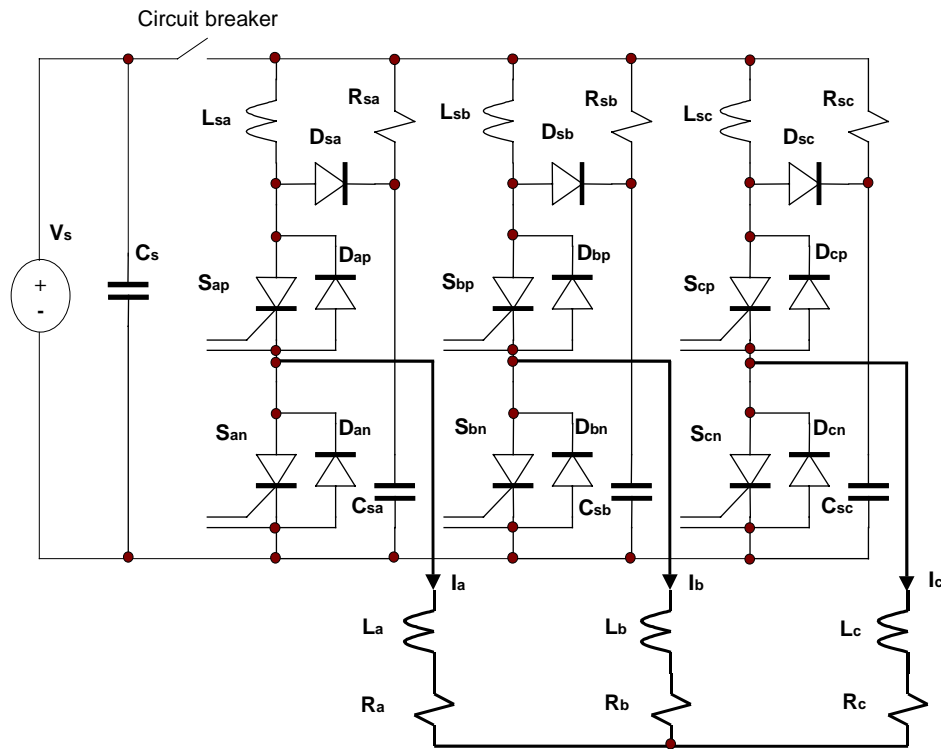


Figure 30: ETO-based three-phase inverter



## 4.2 ETO1045HS Background

The inverter system was designed based on ETO1045HS, a 4.5kV/1.0kA hard switching ETO as shown in Figure 31. This is the same ETO that was used in the previous DC/DC converter, so the characteristics of this device are very well known now. The measured conduction loss curve is shown following in

Figure 32. The snubberless turn-off capability of ETO1045HS has been verified at up to 2.5 MW of instant power dissipation in the ETO during the turn-off transient. The snubberless switching shows only a slight increase in turn-off switching loss compared to that with a  $2\mu\text{F}$   $dV/dt$  snubber, and shows a dramatic decrease in turn-on loss due to the lack of discharge current from the  $dV/dt$  snubber during the voltage fall time. The overall switching loss is reduced when operating in the snubberless condition. The snubberless turn-off loss curves for 1kV and 2kV buses are shown in Figure 33 and Figure 34.



Figure 31: Picture of ETO1045HS

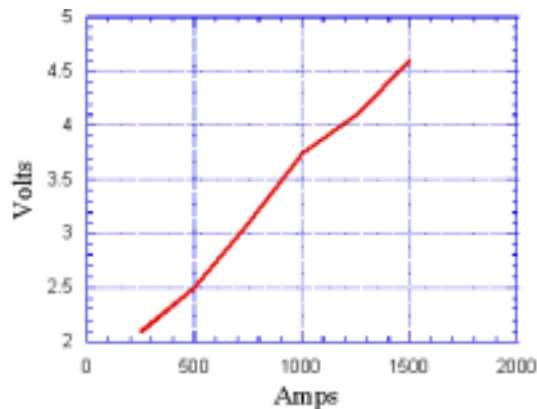
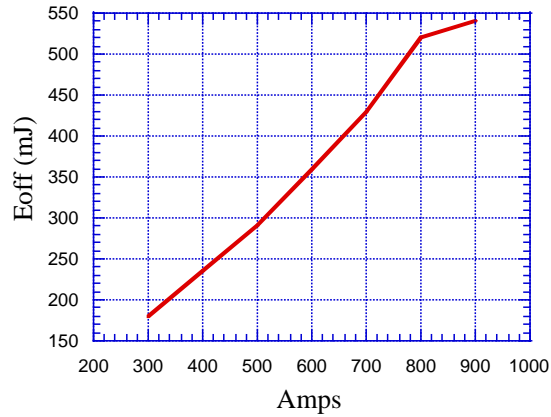
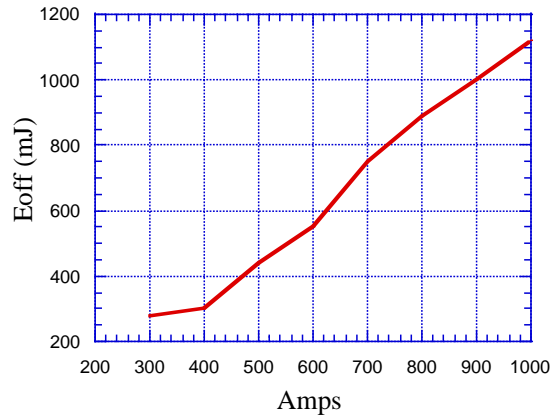


Figure 32: ETO1045HS conduction loss



**Figure 33: 1kV Snubberless turn-off loss**



**Figure 34: 2kV Snubberless turn-off loss**

### 4.3 ETO Phase Leg

Building on the work carried out in the DC/DC converter work, a redesign was carried out on the phase leg (half-bridge) based on two ETOs, two antiparallel diodes, one clamp diode, the clamp capacitor, the gate drivers and suitable heatsinks. The ETOs used are ETO1045HS, the same device used in the DC/DC converter, which are rated for 1000 Amps maximum turn-off current and 4500 Volts blocking. The diodes used initially were ultrafast recovery ABB diodes 5SDF 05F4502. The ETOs and the diodes are in press-pack (“hockey-puck”) packages, so a mechanical clamp is necessary in order to use these packages. The phase leg uses liquid cooled heatsinks and a matching clamp. The phase leg includes five water-cooled heatsinks so each device is double-sided cooled except for the clamping diode, which dissipates very little power.

Due to the fact that the switches will be dissipating more power than the diodes, the design was made to keep the two ETOs separated from each other. Another requirement for the design of the phase leg is that the path from each ETO to the opposite diode should be the same in order to equalize the voltage spike on the switches. The design of the phase leg is shown in Figure 35, and the completed phase leg is shown installed in the enclosure in Figure 36.

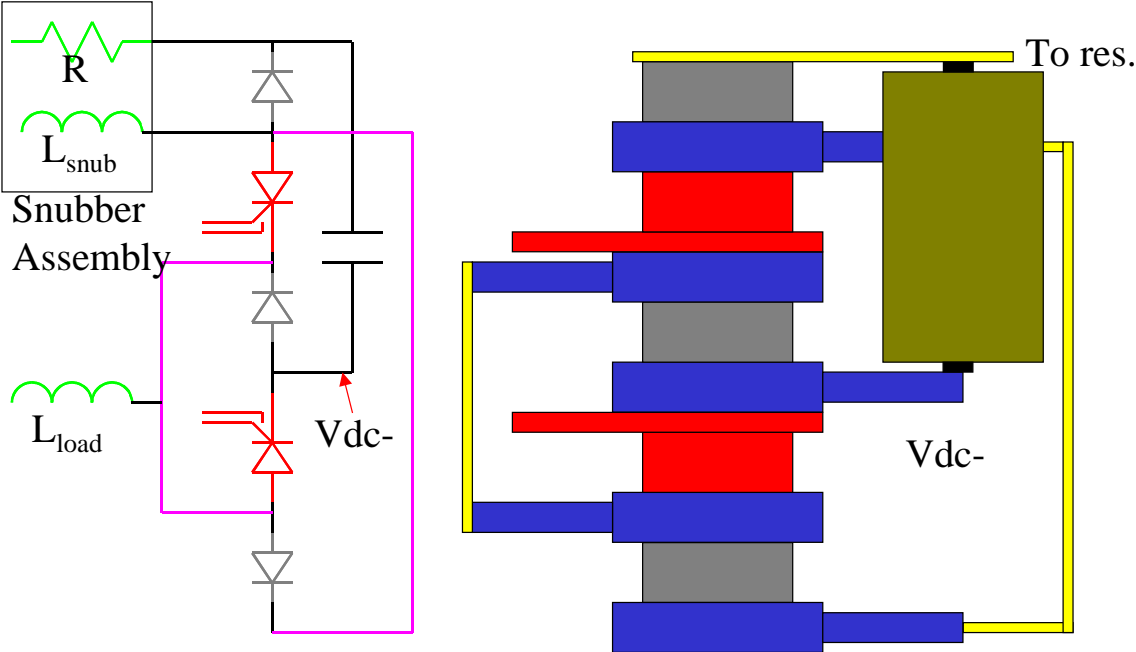


Figure 35: ETO Phase leg design.

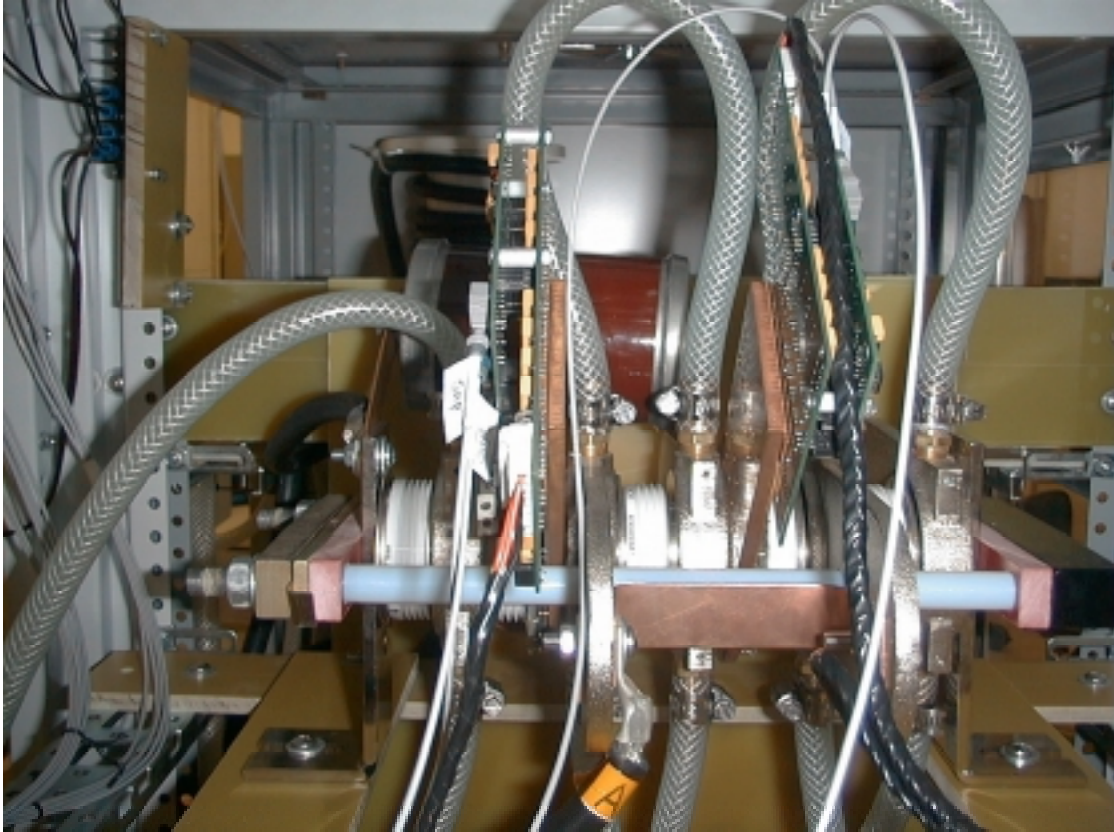
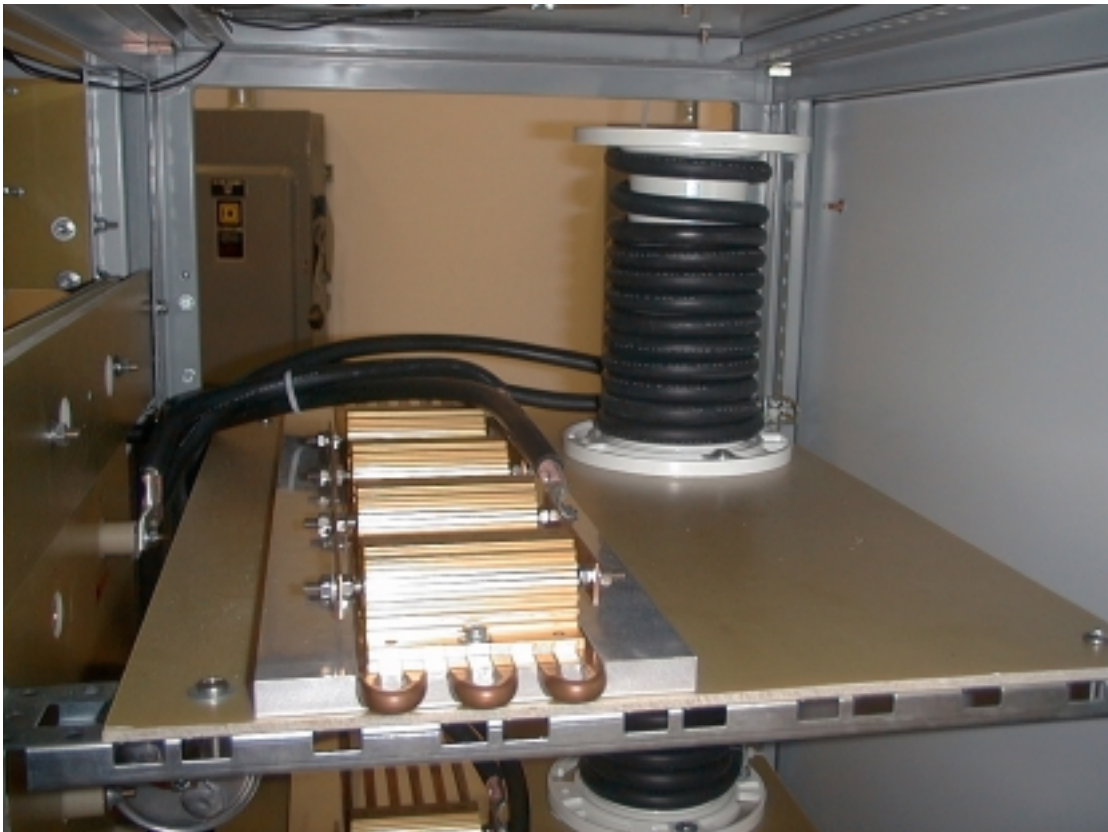


Figure 36: Photograph of completed phase leg

#### **4.4 *di/dt Snubber and Voltage Clamp Design***

Although the ETOs have a snubberless turn-off capability, the diodes do not. Therefore a di/dt snubber is needed to prevent diode failure. This snubber also greatly reduces turn-on switching loss in the ETOs, and the snubber protects the phase leg from damage due to “shoot through” when both the top and bottom switches are on simultaneously. Shoot-through is a common problem when a switch turns on with a very high dV/dt, and the noise induced causes a false triggering of the logic in the other switch’s gate driver. The diodes used can stand a maximum di/dt at turn-off of 500 A. For this inverter the di/dt was selected to be lower than the maximum, so the di/dt was designed to be about 375 A/μs at the maximum bus voltage. A conventional RLD snubber is used. With a designed maximum of 2.5 kV bus, this led to the selection of the snubber inductor by equation 3-1, as in the case of the DC/DC converter.

In order to minimize voltage stress on the ETOs a clamp circuit is integrated into the phase leg. This circuit consists of a diode and a high frequency, low impedance capacitor. This capacitor is mounted very close to the ETOs so it can absorb any energy in the parasitic bus inductance. The clamp diode is the same diode that is used for the  $di/dt$  snubber. This integration reduces the parts count and simplifies construction, and can be seen in Figure 30. A picture of the  $di/dt$  assembly for one phase leg is shown in Figure 37.



**Figure 37:  $di/dt$  Snubber inductor and resistor**



Figure 38: Picture of the ETO-based inverter

## 4.5 Inverter Capability Determination

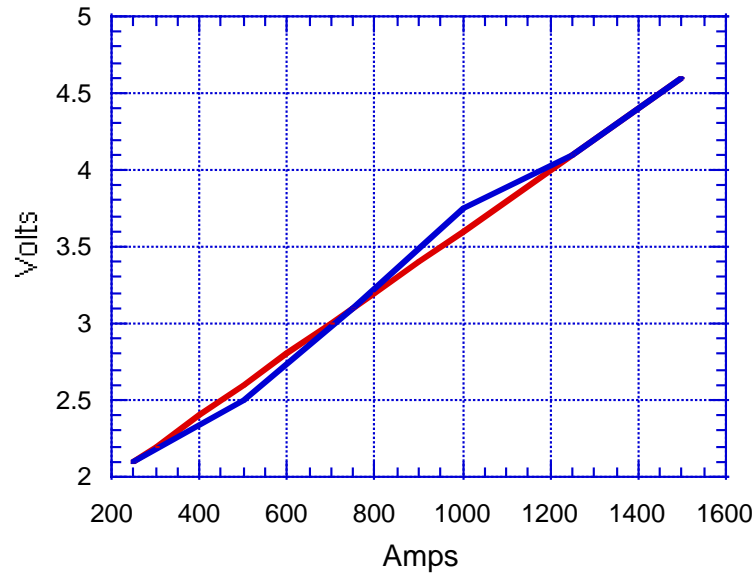
Because the goal of this inverter was to demonstrate the performance of a particular ETO, the system power handling capability is determined by the characteristics of the device used. The determination of the actual power handling capability is important in order to know how the ETO would perform for practical applications. The first rating which must be determined is the allowable DC bus voltage which can be used. The conventional practice for a high voltage device such as the ETO is to set the bus voltage to about half of the breakdown voltage of the semiconductor switch. This allows for voltage spikes above the DC bus due to inductance and the turn-on snubber circuit's charging, and also includes a safety factor which is determined by long-term stability analysis, which is provided by the manufacturer on the data sheet. Some newer designed devices, such as the ETO4045A, are designed for a bus voltage up to two thirds of the breakdown voltage, but the ETO1045HS is designed around a traditional GTO. The bus voltage is therefore selected to be slightly above half of the 4500 volt breakdown, so the bus will be at 2500 volts.

With the DC bus calculated, the next factor in the power handling capacity calculation is to determine the allowable output current at a given switching frequency. This will be done by calculating based on the dissipation and the thermal budget of the device in use. For the ETO1045HS used in this inverter, the measured thermal impedance from the junction to the case is about 35°C/kW. Assuming a heatsink temperature of 55 °C, finite thermal impedance between the case and the heatsink, and a maximum die temperature of 100 °C, the maximum allowable dissipation,  $P_{max}$ , can be estimated to be just over 1 kW. The losses that will be in the device can be separated into conduction loss, turn-on loss, and turn-off loss. Due to the large turn-on snubber, the turn-on loss is neglected as mentioned in chapter 2. The conduction loss and turn-off loss are the dominant dissipation, and both are related to the current level.

From Figure 32, the conduction loss of the ETO1045HS can be seen to be approximately linear. The conduction loss can be approximated by 4-1:

$$V_{on}(I) = 1.65 + \frac{I}{500} \quad 4-1$$

As can be seen in Figure 39, the linear approximation of the conduction loss is reasonably close, and should serve for capacity calculations.



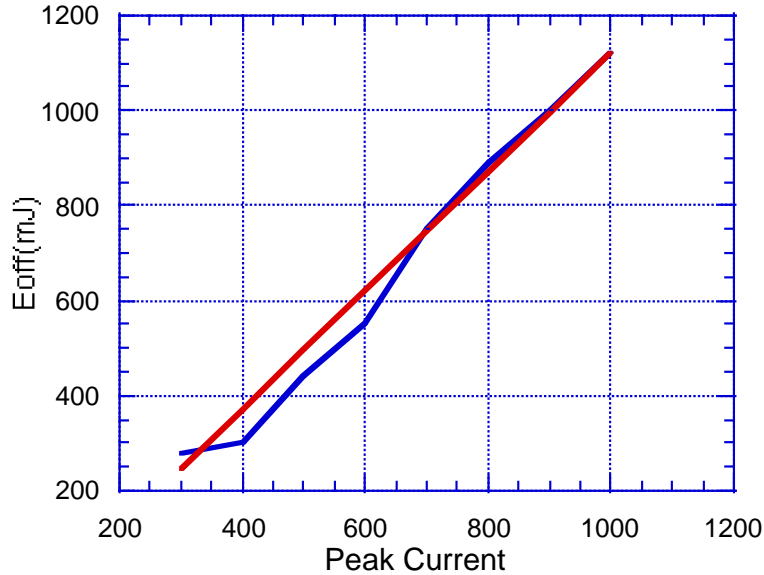
**Figure 39: Measured conduction loss and linear approximation of conduction loss**

Next, the switching loss will be approximated linearly as well. The approximation is carried out by the equation 4-2:

$$E_{off}(I) = I * 1.25 - 130 \quad \text{mJ} \quad 4-2$$

Figure 40 shows the approximated switching loss compared to the measured loss. This has more discrepancy than the conduction loss calculation, especially at low current.





**Figure 40: 2kV snubberless turn off loss and linear approximation**

Because the calculated switching loss is higher than the actual loss, use of this approximation is still reasonable, since it will build a safety factor into the designed values. The neglected turn-on loss can also be absorbed into this error, so the calculation of the output power can be continued.

The amount of current the inverter can deliver depends on the application. For a utility application where the AC frequency is fixed (e.g. 50, 60, or 400Hz) then the switch can rest for half of the line cycle, so the average current can be high. This means that the switch can dissipate twice its rated power half of the time, so the average dissipation is still allowed. However, for a motor drive application the wide speed range may make this impossible. For example, if a motor is starting then the output frequency will be quite low, possibly a fraction of a Hertz. In this case, the switch would overheat during half of a line cycle, because a several second cycle must be treated similar to DC. For this reason a motor drive inverter must be designed so it can provide its rated current constantly like a DC/DC converter, where a utility inverter only needs to be able to deliver a specified average current.

## **4.6 Utility Inverter Capacity**

For a utility inverter, the current flows through a switch for half of a line cycle and then the current is zero through that switch for the other half of the cycle. Therefore the average

current through the switch is half of the average current during the half-cycle where it conducts. The actual average current through the switch is also proportional to the duty cycle, which is given by the following expression:

$$D(\alpha) = \frac{1}{2} \cdot [1 + M \cdot \sin(\alpha + \phi)] \quad 4-3$$

M is the modulation depth,  $\alpha$  is the angle within the sine wave and  $\phi$  is the angle of the load impedance. The instantaneous conduction loss for the main switch is given by:

$$E_{cond}(\alpha) = I(\alpha) \cdot V_{on}(I(\alpha)) \cdot D(\alpha) \quad 4-4$$

where

$$I(\alpha) = I_{max} \cdot \sin(\alpha) \quad 4-5$$

The power dissipation due to conduction loss is the average of the instantaneous conduction loss over a line cycle. Remembering that the switch conducts only for half of a line cycle (as reflected in the limits of integration), this is given by:

$$P_{cond} = \frac{1}{2\pi} \cdot \int_0^\pi E_{cond}(\alpha) \cdot d\alpha \quad 4-6$$

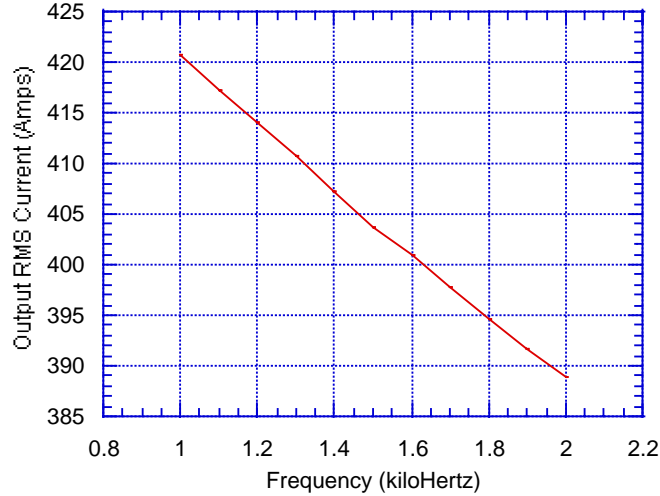
It can be seen that the highest conduction loss occurs at a load angle of zero, as the duty cycle is then maximum at the same time that the current is maximum. The determination of the system's capacity will therefore assume a load angle of zero, which is the worst case. The other component of the dissipation in the switch is the turn-off loss, which can be calculated easily. The switching power loss can be found as the average switching energy loss across a line cycle multiplied by the switching frequency. The expression is given by:

$$P_{sw}(I) = f_{sw} \cdot \frac{1}{2\pi} \cdot \int_0^\pi E_{off}(I(\alpha)) \cdot d\alpha \quad 4-7$$

The total power dissipation on the switch is equal to

$$P_{loss} = P_{cond}(I) + P_{sw}(I) \leq P_{max} \quad 4-8$$

Based on this estimate, the output current as a function of the switching frequency can be calculated, assuming a modulation depth  $M$  of 1 and a load angle of zero, and that the switch power dissipation is the limiting factor in the system. The graph is shown in Figure 41.



**Figure 41: Output current versus frequency**

The modulation scheme is assumed to be either space vector modulation or sinusoidal PWM with the third harmonic injected. In either case, the maximum line-to-line voltage will be equal to the modulation depth  $M$  multiplied by the DC bus voltage. In this example, with  $M$  at 0.9 and the bus voltage at 2500, the maximum output voltage is:

$$V_{o_{peak}} = V_{dc} \cdot M = 2250 \quad 4-9$$

$$V_{o_{RMS}} = \frac{V_{o_{peak}}}{\sqrt{2}} = 1590 \quad 4-10$$

The three-phase output power is equal to:

$$S_{o_{RMS}} = \sqrt{3} \cdot V_{o_{RMS}} \cdot I_{o_{RMS}}(f) \quad 4-11$$

This function can be plotted, as shown in Figure 42.

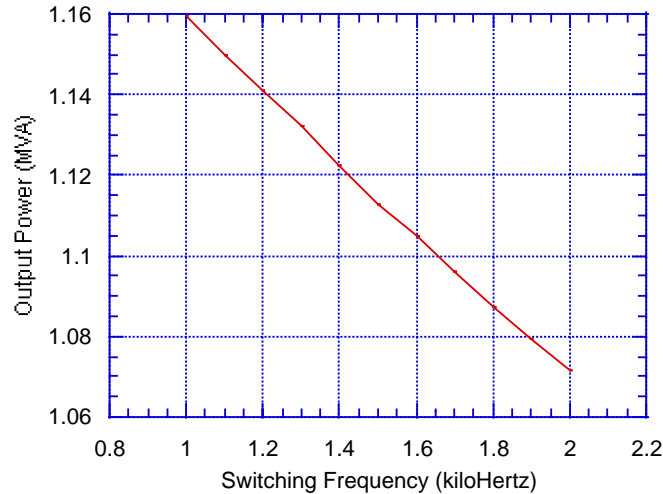


Figure 42: Output power versus frequency

### 4.7 Motor Drive Power Capability

The calculation of the capacity of a motor drive inverter is much easier if the motor drive must operate for extended times at extremely low output frequencies. If the motor drive only operates at line frequencies similar to the utility, then the calculations above hold. When the output period is much longer than the thermal time constant of the switch, then the inverter can be treated as a DC converter. In this case, the conduction loss and switching loss are given as:

$$P_{cond}(I) = I_{o_{peak}} \cdot V_{on}(I_{o_{peak}}) \quad 4-12$$

$$P_{sw}(I) = f_{sw} \cdot E_{off}(I_{o_{peak}}) \quad 4-13$$

This can also be plotted as a function of output current versus frequency, as shown in Figure 43. The three-phase output power can also be plotted, as shown in Figure 44. The inverters power handling capability is clearly much lower if it cannot cool down during part of the line cycle. This high stress operation is typical of motor starting where the current will be high for torque production and the output frequency will be low, as the motor speed will be low.

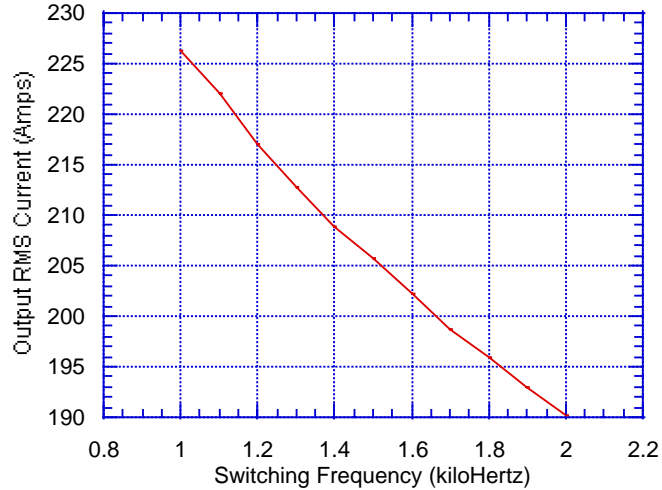


Figure 43: Output current versus switching frequency for low-frequency AC output

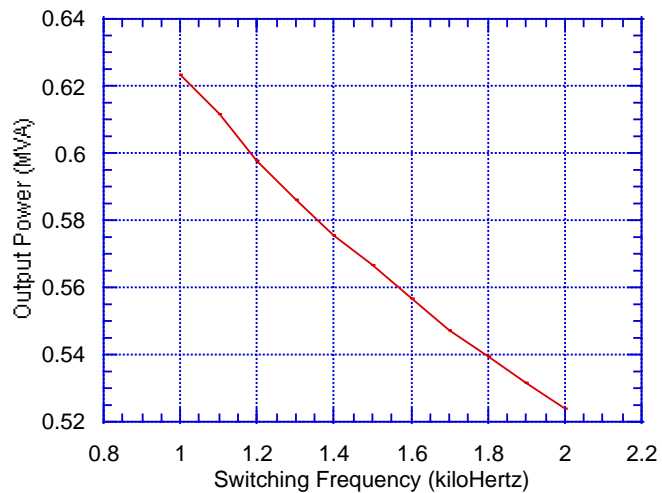
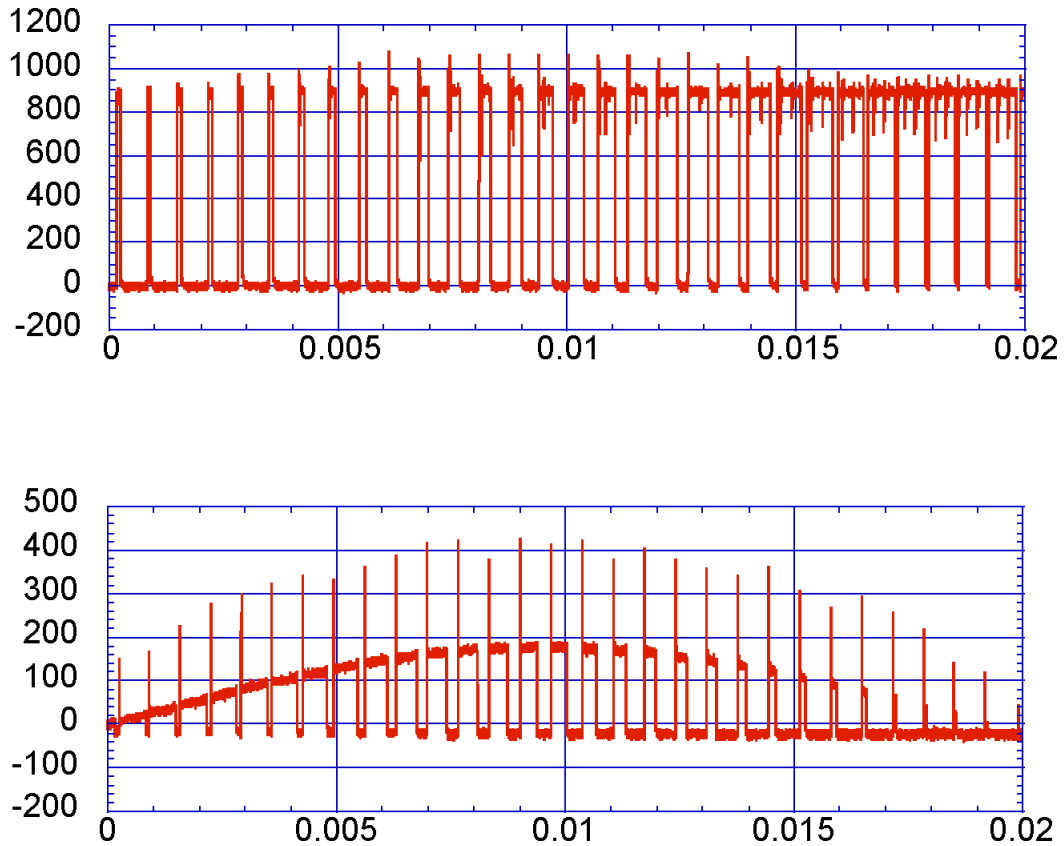


Figure 44: Output power versus switching frequency for low-frequency AC output

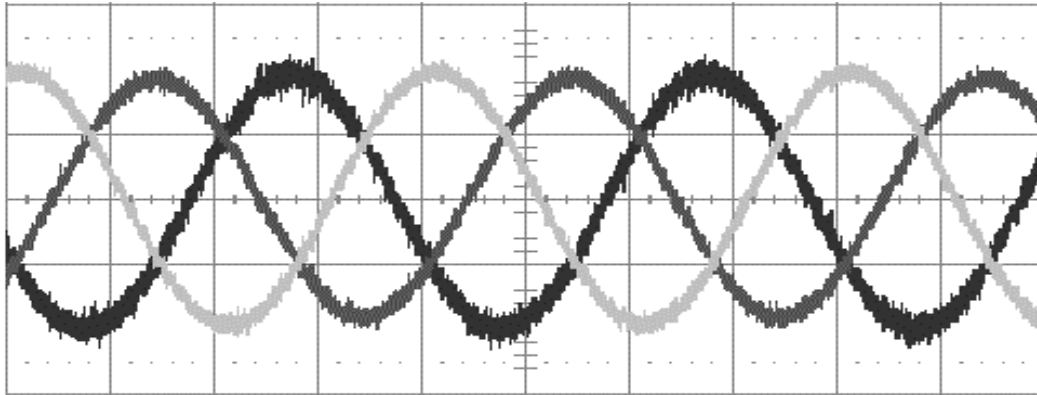
### 4.8 System Test Results

The inverter has been tested in reactive mode up to 200 Amps per phase peak with a 900 Volt bus. The limiting factor in the current is the load inductors, and the power supply is the limit for the voltage. The operating waveforms for the inverter over a line cycle are shown below. These waveforms were taken with an input of 900 Volts, and an output line frequency of 25 Hz. This frequency is low in order to reduce the impedance of the load inductors, thus allowing a higher output current. The waveforms are equally good at 50/60 Hz, but the output current is much smaller due to the higher reactance.



**Figure 45: ETO voltage (top) and current (bottom)**

As can be seen from current waveform, there is significant diode reverse recovery, with the recovery current becoming as high as the load current, so the peak current through the ETO is 430 Amps. This is because the high-speed diodes originally installed had to be replaced with slower diodes as detailed in chapter 5. The three-phase output waveforms are shown following in Figure 46.



**Figure 46: Three-phase output currents**

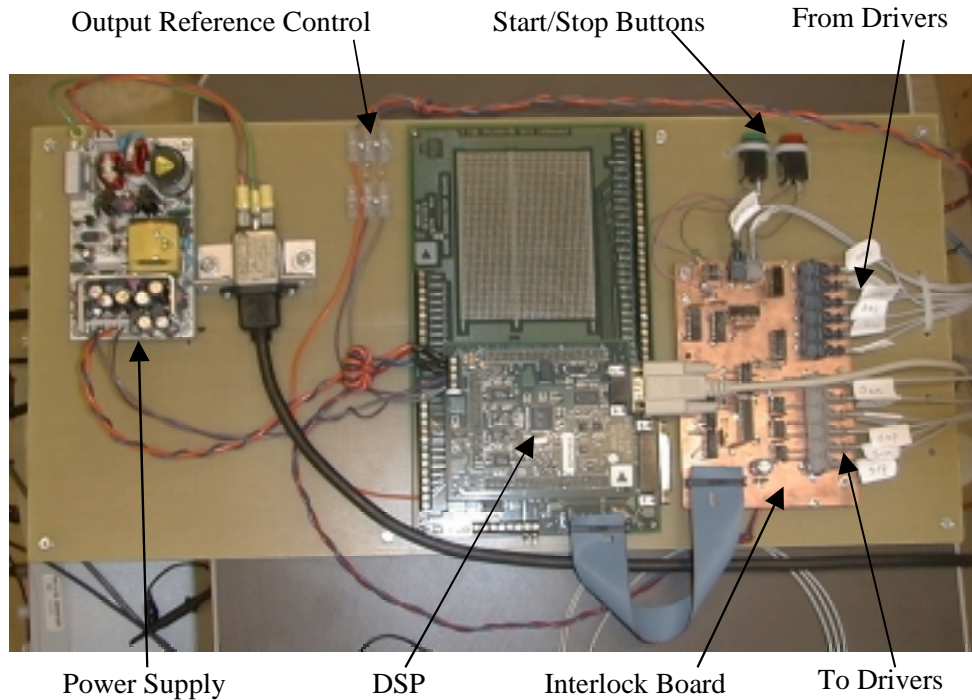
As can be seen from the output current waveforms, the performance of this inverter is good due to the high switching frequency. These results indicate that the ETO is a promising device for use in high-frequency systems.

## **4.9 Protection**

In order to protect this converter multiple stages of protection are employed. One section is the interlock, which is designed to prevent shoot-through. The interlock compares the feedback signal from the gate drivers against the command signal by means of an exclusive-OR gate, which will indicate a malfunction if they are different. The interlock also injects the dead-time at every switching transition, where both switches in the phase leg are held off simultaneously for a short time. The dead-time is measured from the end of the feedback pulse from the outgoing switch, so this logic prevents the incoming switch from turning on until the outgoing switch has been off for the specified time. This automatically prevents shoot-throughs even if the DSP were to malfunction and command both switches in a leg to turn on simultaneously.

When the interlock system detects a fault, it freezes the state of all of the gate driver commands and orders the active circuit breaker to turn off. This is because the ETOs can safely conduct a very high current for a short time, even if that current is well beyond their safe turn-off capability. This will allow the active circuit breaker time to open and clear the fault. After a fault condition, the interlock board must be manually reset. If the active circuit breaker detects a

fault with its current sensor, this condition also trips the interlock. The interlock board can be seen together with the DSP in Figure 47, and its schematic is shown in the appendix.



**Figure 47: DSP and interlock board**

#### **4.10 Three-Phase Test Conclusions**

The testing of the ETO-based three-phase converter has shown that the higher switching frequency that the ETO offers can produce good performance, with high-quality output current waveforms. For this reason, the ETO is well suited for application in energy storage applications, where the quality of the power is very important when connecting to the grid. The ETO is also well suited to motor drives, where harmonics in the output are unacceptable because they cause increased heating of the motor. A new failure mode of the ETO was identified, which resulted from unintended conduction of a parasitic diode between the gate and the anode, and is discussed in chapter 5. This failure mode can be eliminated by the use of an external diode with low conduction loss, although more work is necessary in order to consider additional solutions. The performance has shown the expected benefits of the ETO, and should remain good as the power level is increased to the designed rating.



# Chapter 4 – ETO Based Three-Phase Inverter

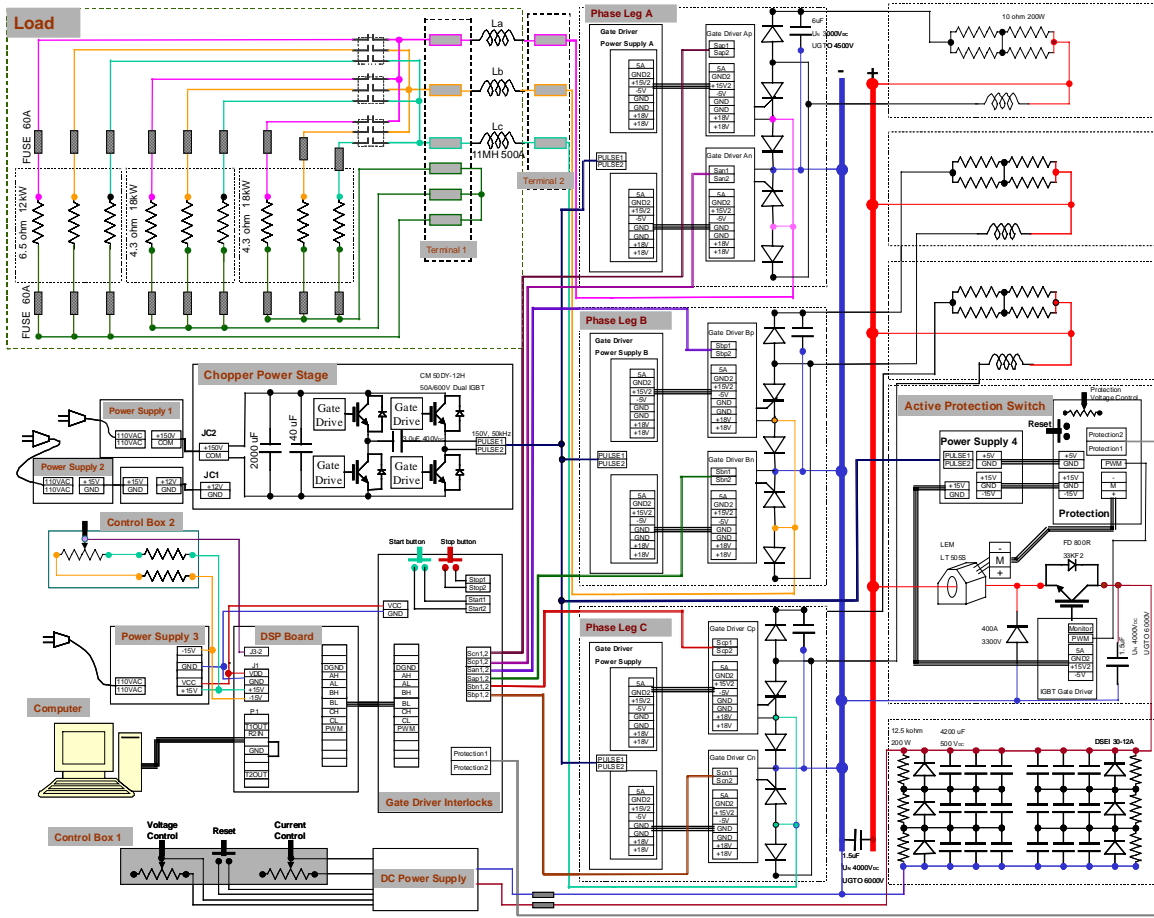


Figure 48: Complete ETO voltage source inverter system

## Chapter 5 - Unconventional Failure Issues

### 5.1 Anode Short Structures

In order to increase the switching speed of many GTOs, a structure known as anode shorted is employed. In this structure, a small portion of the internal n- region is connected to the anode contact, which partially bypasses the p region at the anode. Because this short is only a small fraction of the total area, it is very resistive. This structure, shown in Figure 49, serves to reduce the gain of the PNP transistor portion of the GTO. The result of this reduction in gain of the PNP transistor results in a reduction of the positive-feedback loop gain for the entire GTO structure. With this gain lower, the switching times reduce, especially the current tail phase.

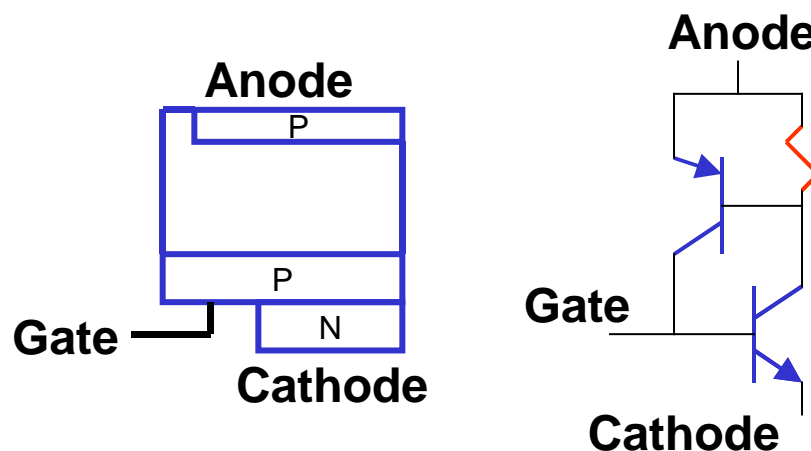
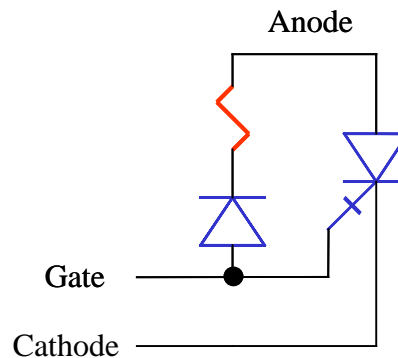


Figure 49: Anode short GTO structure and equivalent circuit

The obvious drawback of the anode shorted structure is the loss of the ability to block reverse voltage, since the junction that is bypassed is the one which normally blocks reverse voltage. Although the gate to cathode junction can block some reverse voltage, the breakdown of this junction is only about 20 Volts. Another drawback of the anode shorted structure is a significant increase in conduction loss for a GTO, due to the reduced current gain resulting in the device operating in a less deeply saturated mode.

## 5.2 Anode Short Parasitic Diode

Another problem with the anode shorted structure which is less obvious is that there is now a diode present from the gate to the anode. Since this diode is parasitic, its switching performance will be very poor, since the junction was optimized to be part of a thyristor. This is important to consider when using the ETO and the IGCT, as unintended conduction of this diode can occur. An equivalent representation of the GTO is shown in Figure 50 with this anode short diode.



**Figure 50: Anode short GTO equivalent representation**

From the equivalent circuit of the ETO, it can be seen the conditions which can cause this parasitic diode to come into conduction. As always, current will attempt to take the path of lowest impedance. If the total voltage drop through the path which includes the parasitic diode is less than that of the discrete diode, then current will start to flow through the parasitic diode. When the ETO is gated ‘ON’ this is unlikely, since this diode appears in series with the body diode of the gate MOSFETs  $Q_g$ , which has a relatively high conduction voltage drop. However, when the ETO is gated ‘OFF’, the gate MOSFET appears as a small resistor rather than a diode. In this case, current can flow through the parasitic diode of the GTO if that diode’s conduction voltage is less than or even similar to that of the external discrete diode. The situation where this is likely to occur is during the dead-time of an inverter, where both switches in a leg are gated off simultaneously.

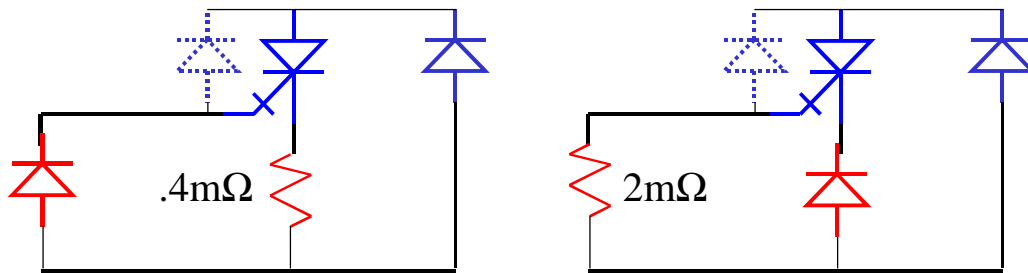


Figure 51: Equivalent circuit of the ETO gated 'ON' (left) and 'OFF' (right)

### 5.3 Parasitic Diode Failures

The significance of this parasitic diode was shown during testing of the three-phase inverter described previously. Two failures occurred which were not consistent with normal failure modes of the ETO. In this failure mode, the GTO die is damaged at the point of connection to the gate lead, but nowhere else. In a normal ETO failure, due to a turn-off SOA violation, the die is damaged in a line parallel to the gate lead, as all of the current crowds this section since it is the path of minimal inductance. A detailed description of the ETO's failure mode can be found in [13]. Since this damage observed in the inverter failures was inconsistent with a normal turn-off failure, the reverse recovery of this parasitic diode was suspected. In order to verify this, a test was conducted on the phase leg at low power with current probes on the ETO and the antiparallel diode. These results, shown in, show that even though the discrete diode carries the majority of the current, the GTO diode is responsible for the majority of the reverse recovery current. Keeping in mind that this diode is very small in area (due to the small area of the anode shorts relative to the total die size), the current density of this recovery current is quite high. These test were performed with a high-speed antiparallel diode, ABB's 5SDF 05F4502, which is a 4.5 kV diode designed for application with the IGCT, and is optimized for good recovery characteristics. These waveforms, shown below in Figure 52 and Figure 53, show that the current is initially carried by the diode as expected. However, when the gate driver for the ETO gives the turn-off command, the current starts to move into the GTO's reverse diode. When the other ETO turns on, the reverse recovery process shows that the GTO produces  $2/3$  of the total recovery current, even though it carries only  $1/4$  of the total current right before turn-off. All of this current passes through the gate lead, and this diode is not intended to conduct. It is clear that the parasitic diode is able to conduct a significant amount of total current, so the conduction loss of the diode must be similar to that of the external discrete diode.

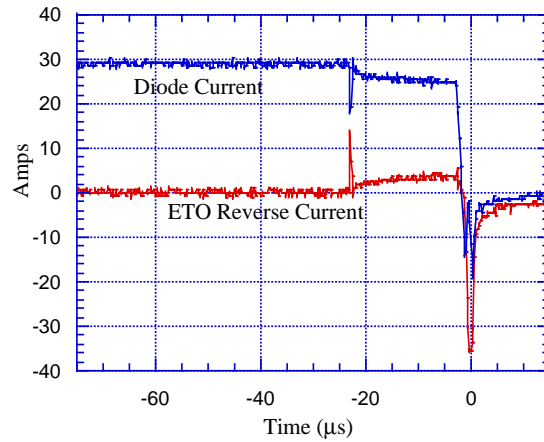


Figure 52: Diode and GTO reverse recovery waveforms ( $V_{bus}=200$ )

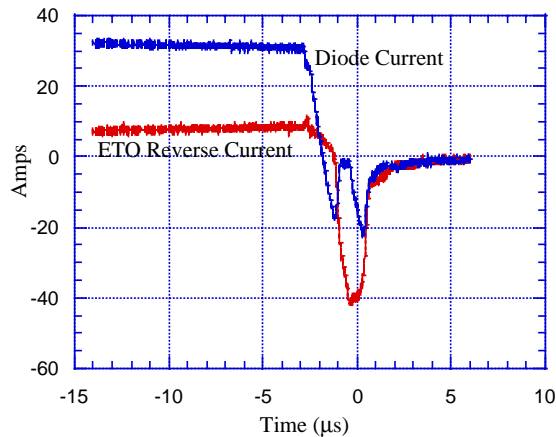
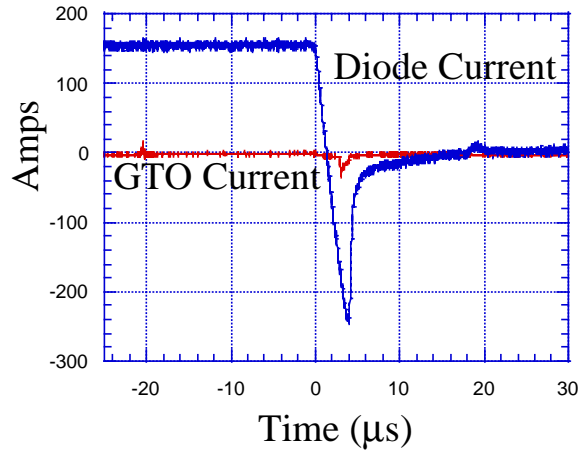


Figure 53: Detail of reverse recovery of GTO parasitic diode

## 5.4 Proposed Solutions

From the analysis of the reason for the current flowing through the parasitic diode, there are two obvious solutions to this problem. In order to prevent this diode from conducting, the impedance of the path through the discrete diode should be much less than that of the parasitic diode's path. This can be done by lowering the conduction loss of the external diode or by increasing the conduction loss of the path through the parasitic diode. The first alternative is easily implemented, as slower diodes have less forward conduction voltage than the high-speed diodes initially used. To explore this method, the phase leg was reconstructed with slower diodes and the test was repeated. With the slower diodes installed, the reverse recovery current of the GTO was dramatically reduced, as the discrete diode now conducted almost all of the current. From the waveform, shown in Figure 54, it can be seen that the GTO's parasitic diode

did not carry any current at all until the reverse recovery process of the main diode began. During the reverse recovery process, the impedance of the diode is increasing so the current transfers a small amount into the GTO's diode. However, with this greatly reduced current the safe operation of the GTO is insured. With the changes made, the converter was able to operate at high voltage and high current without any recovery problem from the GTO diode.

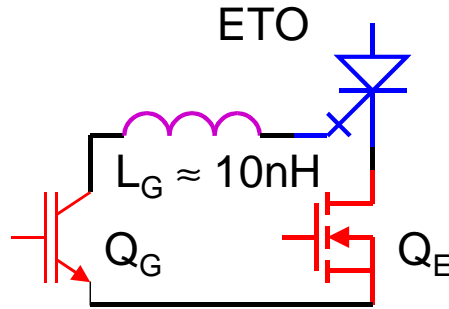


**Figure 54: Reverse recovery with slow diodes (Vbus=900)**

It is clear that the slower external diode has significantly more reverse recovery than the fast diode initially used had. For this reason, better solutions to this problem than the slow diode are needed. If decreasing the impedance of the path through the discrete diode can alleviate the problem, increasing the impedance of the path through the parasitic diode can also help. One obvious way to do this is to replace the MOSFETs used for the gate switch on the ETO with other devices that can block reverse voltage. One such device which can be used is a small IGBT as shown in Figure 55. For the ETO's emitter switch, only MOSFETs are reasonable since the conduction loss of this switch must be minimal. However, the gate switch only conducts for very brief intervals, so conduction loss is not critical. No prototypes of this technique have yet been constructed.

Another option which is available is to use a GTO which does not have this parasitic diode present. Such GTOs are readily available, but their switching performance is dramatically inferior to that of the anode shorted GTOs. The increased reverse recovery loss of a slower

diode may not be as high as the increased switching loss of a reverse blocking GTO. The anode shorted GTOs are used in the ETO and the IGCT at present, although reverse blocking prototypes of each have been developed for use in current-fed circuits [26,27].

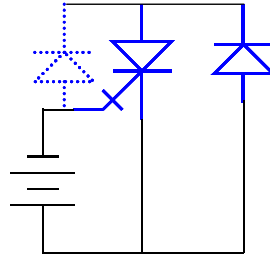


**Figure 55: ETO using IGBT for gate switch**

One other place where this parasitic diode plays a major role is in resonant commutation circuits such as soft-switching converters. In this case, the parasitic diode is even more conductive than usual since the junction is flooded with carriers from when the device was in forward conduction. In an experiment with a (Mitsubishi) GCT, 50% of the reverse resonant current flowed through the GCT's parasitic diode and only 50% went through the discrete diode.

### **5.5 IGCT Issues**

The IGCT has this parasitic diode as well, but it does not have the same problem with this diode coming into conduction. The reason is clear from looking at the circuit of the IGCT's gate connection. To turn an ETO off, the gate is grounded and the cathode is floated. However, an IGCT turns off by leaving the cathode grounded and driving the gate negative. The difference is that the parasitic diode appears in series with the turn-off power supply for the IGCT, so the current will not go this way as long as there is an external diode present. The equivalent circuit for the IGCT gated off showing the parasitic diode is shown in Figure 56.



**Figure 56: GCT circuit showing parasitic diode**

Although the IGCT's gating circuit protects it from the unintended reverse conduction of the parasitic anode short diode, there is a different problem unique to the IGCT involving a circulating current with the antiparallel diode. The issue arises when the IGCT switches off a very low current relative to its maximum current, such as happens near the zero-crossing of a line cycle in an inverter application. In this situation, the NPN transistor turns off very quickly, but the PNP portion is still highly conductive, since the low current does not quickly remove the charges from the base. During this time, the anode is effectively shorted to the gate, which is 20 volts below ground. This 20-volt supply is applied to the antiparallel diode as well as any stray inductance present. Since the diode is forward biased, it turns on and begins to conduct current, and the full 20 volts are applied to the stray inductance. Since normal phase-leg design techniques call for minimizing the stray inductance between the switches and the diodes, this inductance will be quite small, and the current will rise quickly. This current will continue until the PNP portion of the IGCT recovers its blocking capability, which will correspond to the time when the anode voltage rises. At this point the diode will do a very hard turn-off, as the current is removed instantaneously and the voltage is immediately reapplied. This situation can be made even worse if a reverse conducting (integrated antiparallel diode) IGCT is used, where the stray inductance will be extremely low. Although this process will probably not lead to immediate failure of the diode, it will increase the stress on the diode. Since the diode is flooded with carriers when the voltage is reapplied, a significant reverse current will flow.



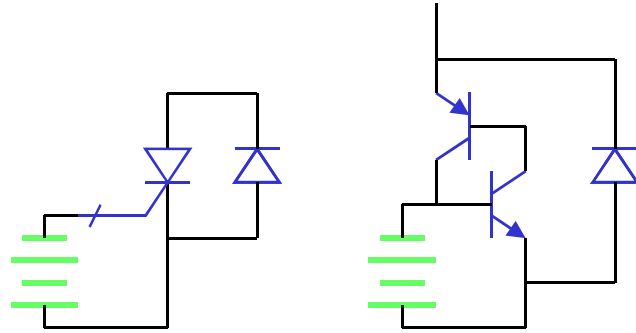


Figure 57: IGCT two-transistor equivalent circuit

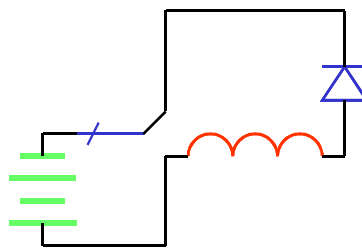


Figure 58: IGCT equivalent circuit after recovery of NPN before recovery of PNP

The impact of this can be seen in the following waveforms. In Figure 59, it is clear that the anode voltage become negative shortly after the gate driver applies the turn-off command. The DC bus voltage is very low at this point, so the reverse recovery current is not significant, although it is visible.

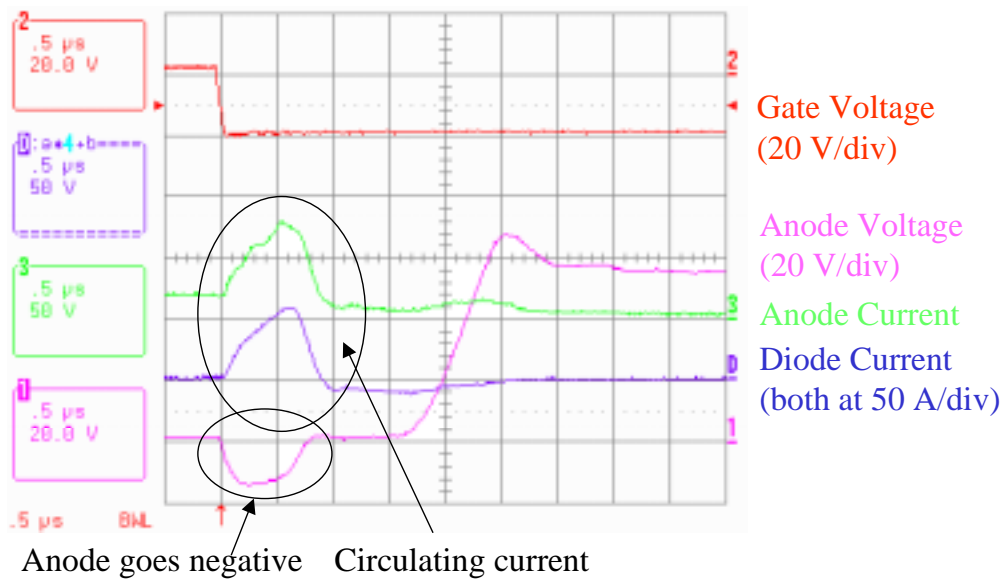
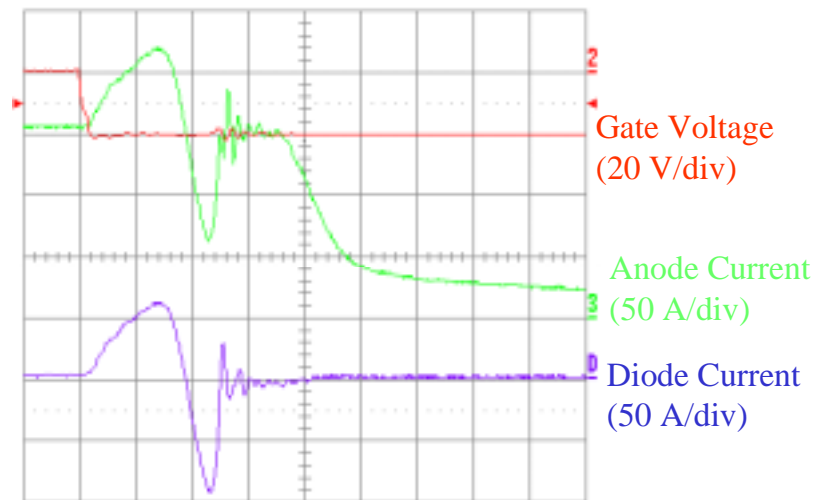


Figure 59: Circulating current in IGCT due to negative anode voltage

A more significant reverse recovery of the antiparallel diode is shown in Figure 60. This result was taken with a 400 volt bus and a turn-off current in the IGCT of 160 Amps. The peak reverse recovery current of the diode is 85 Amps at this condition. For comparison, this same diode, a fast recovery model, gives less reverse recovery current at a 2kV bus voltage when it turns off 300 Amps when it turns off with the  $di/dt$  limited by an appropriate snubber. This circulating current and unexpected reverse recovery should be consider in the design of an inverter. The extra reverse recovery lead to increased thermal stress on the diode, as it is switching twice as often as expected. The results shown here were taken with a relatively high inductance between the switch and the diode, so the results may be worse in a practical implementation rather than a single-pulse tester or with an integrated diode.



**Figure 60: Reverse recovery of the antiparallel diode due to circulating current**

## Chapter 6 - ETO Gate Driver Design

### 6.1 Requirements

In order to drive the ETO, three separate gates have to be controlled. The emitter switch and the gate switch are both MOS-gated devices, and the GTO's gate requires current injection to turn on, although the ETO does not require turn-off current from the driver. To realize these functions, a block diagram of the driver is shown in Figure 61.

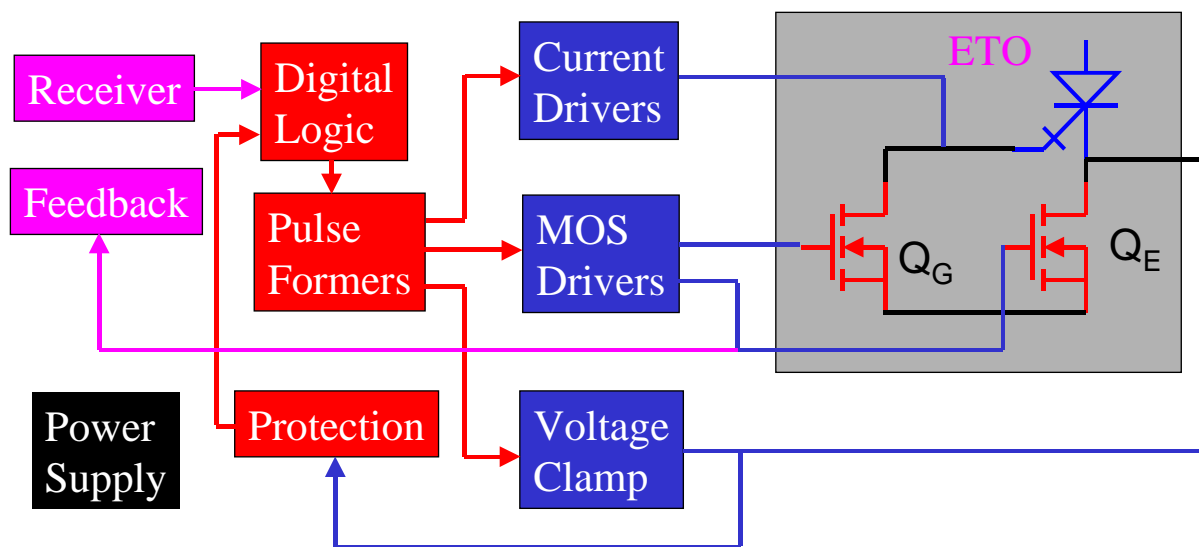
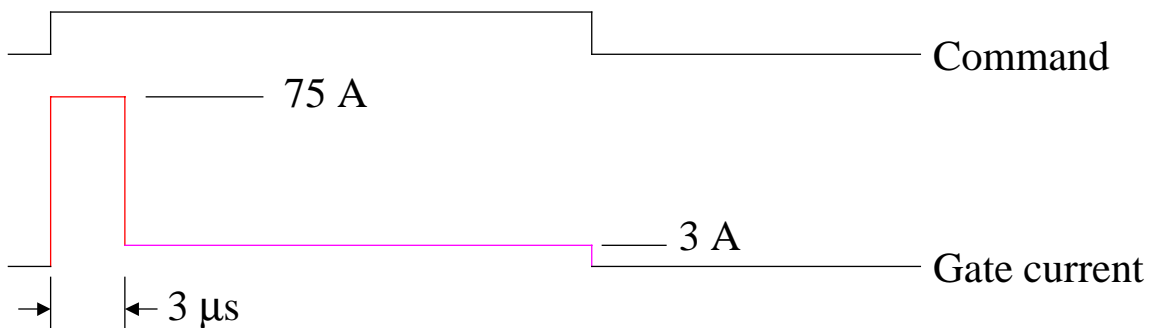


Figure 61: ETO gate driver block diagram

To make sure that the device always has a uniform current distribution prior to turn-off, a minimum on-time protection is incorporated into the gate driver that requires that the device stay on for at least 20  $\mu\text{s}$  every time it turns on. Also, a minimum off-time protection is included so that all current will be flowing through the  $dI/dt$  snubber inductor rather than the diode and resistor at the switching instant. The time required here is related to the time constant of the  $dI/dt$  snubber, and is typically set to 20  $\mu\text{s}$ . This insures that the snubber will properly control the turn-on process. Additionally, instantaneous overcurrent protection is incorporated into the ETO's gate driver. This takes advantage of the emitter switch's characteristic in that it behaves like a linear resistor, so the current through the device can be approximated by observing the voltage across the emitter switch. This voltage is fed to a comparator which will terminate the

on state pulse if the current is too high. The actual status of the gate driver is returned to the master controller by transmitting the emitter switch gate signal back on an optical fiber. In this way the controller can verify proper operation of the drivers and can detect overcurrent when the driver is commanded on but prematurely terminates the pulse.

Turning the ETO on requires that the gate of the emitter MOSFETs be driven high and that the MOSFETs connected to the GTO's gate be turned off by applying a negative voltage to the gate. In addition, turning the ETO on also requires that a large pulse of current be injected into the gate of the GTO for about 3  $\mu$ s in order to provide some carriers initially so that the GTO may begin to latch, as shown in Figure 62. While the ETO is on, a small DC current is provided for the GTO's gate in order to ensure that the GTO remains in a low conduction loss state. Turning the ETO off requires that the emitter MOSFETs be turned off and the GTO gate MOSFETs turned on by applying appropriate voltages to the MOSFET gates. Additionally, when the ETO is off the voltage on the drain of the emitter MOSFETs is clamped to a minimum of 18 volts by the driver to ensure that the GTO's gate to cathode junction remains reverse biased and that the body diode of the diode does not conduct.



**Figure 62: GTO turn-on current requirement**

The control logic for the ETO driver receives commands from the system controller by means of an optical fiber link. The driver feeds the actual state of the gate output back to the master controller so that faults can be easily detected. The control logic generates commands for all other sections of the driver such as the pulsed current injection and the active clamp. The minimum on-time and minimum off time are controlled by pulse generators that are in the

control logic section. The timing diagram of the logic section is shown in Figure 63. As can be seen, logical OR and AND operations are used in conjunction with the input signal and pulses generated at transitions in order to generate the real output, which is sent directly to the gate drive of  $Q_E$ . By observing the timing diagram, it is clear that the drive signals for  $Q_G$  and the voltage clamp are both complementary of  $Q_E$ .

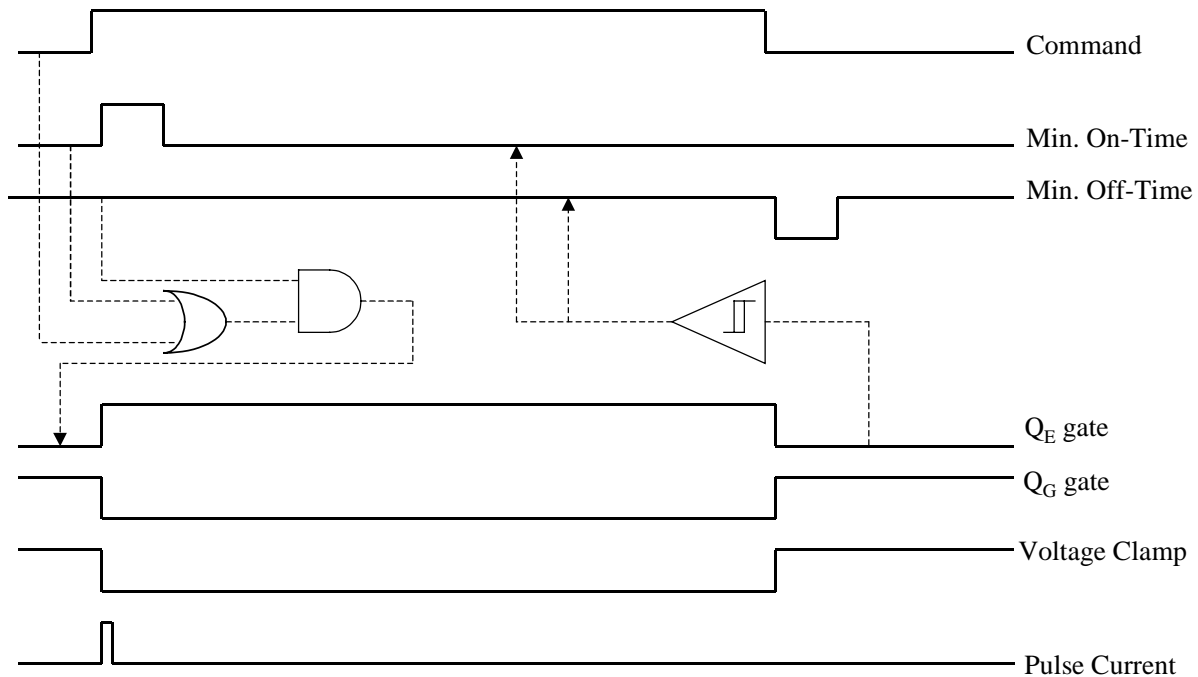


Figure 63: ETO driver timing diagram

## 6.2 MOSFET Driver Section

The MOSFET driver section is very simple. The emitter MOSFETs  $Q_E$  are driven by a bipolar transistor based push-pull section, while all other MOSFETs are driven by CMOS IC drivers. The drivers are optically isolated from the control logic where appropriate when the reference is other than ground, as is the case for the pulse current injection and the voltage clamp. The MOSFET drivers apply 12 Volts to the gates when the MOSFETs are commanded on, and apply -5 Volts when the MOSFETs are commanded off.

### 6.3 Active Clamp Section

The ETO's hard switching capability is strongly dependant on the voltage clamp section of the gate driver. This is fully explored in [13], and a brief explanation follows. When the ETO turns off, there is a large current flowing in the gate which is equal to the anode current. A short time later, the anode current falls very quickly to the tail value. At this time, the gate current is still flowing and is held on by the gate inductance. From Figure 64 and Kirchoff's Current Law, it is apparent that the difference of the gate current and the anode current must be flowing *into* the cathode of the GTO. Initially this current is provided by discharging the output capacitance of the MOSFETs comprising  $Q_E$ , but that capacitor does not store enough energy to discharge the gate inductance fully. The current will still need to flow into the cathode, and can easily do so by means of the body diode of  $Q_E$ . Once the gate current reaches the anode current so the cathode current goes to zero, a resonant process will begin involving the junction capacitance of the GTO, the stray inductance of the gate loop, and the recovering diode of  $Q_E$ . If any of this current is allowed to flow into the gate and out of the cathode of the GTO, it will initiate a retriggering of the GTO, which leads to turn-off failure. If the diode of  $Q_E$  is not undergoing reverse recovery, there is no path for current to flow coming out of the cathode, so this resonance will not occur. It is therefore imperative to make certain that the diode is either fully recovered by the time the gate current decreases to the current tail level, or that the diode never carries current so that it does not need to recover. Several schemes to accomplish this were proposed, but the best one found was to apply an external voltage source across the emitter switch when the ETO is off. This provides three benefits – a reverse bias for the gate of the GTO, and it can either recover the body diode of the MOSFETs or prevent it from conducting at all.

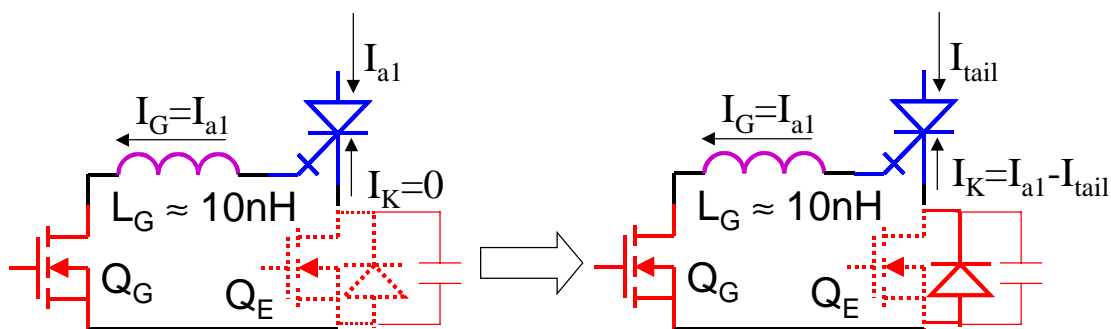


Figure 64: ETO at the unity gain point (left) and in the current tail (right)

The stray inductance in the clamp circuit, the gate loop inductance, and the rate of fall of the anode current combine to determine whether the clamp will recover the diode or prevent the diode from conducting. If the stray inductance of the clamp is high, then the current will initially flow through the diode of the MOSFETs. However, the clamp will be trying to force that diode to block voltage, so the clamp will take over the current into the cathode. Once the diode stops conducting, the reverse recovery current can flow being supplied by the clamp circuit, so the recovery process can finish before the GTO gate current decays to the current tail value. If the clamp circuit's inductance is suitably low, then the current required by the GTO will come from the clamp always, and the diode will never conduct.

The ETO1045 was tested at a range of turn-off currents ranging from 300 Amps to its rating, 1000 Amps. The minimum voltage allowed on the emitter switch by the clamp circuit was measured, in order to verify the correct operation of this clamp. As can be seen in Figure 65, the minimum voltage allowed decreases as the current being turned off increases. The higher bus voltage causes the anode current to fall faster, so the clamp voltage falls further as the bus voltage rises. If the ETO operates at 400 K (125 °C), then it is slower than at room temperature, and the minimum clamped voltage is not as low. It is clear that in all of these cases, the inductance of the clamp is low enough that the current required by the ETO's cathode is provided exclusively by the clamp circuit, and that the body diode of  $Q_E$  does not ever conduct, as evidenced by the diode never becoming forward-biased. It is important to note that the ETO does not fail at the point where the clamp voltage reaches zero, as this only indicates conduction of the body diode. Failure will occur only when the body diode conducts and the clamp circuit is unable to recover the body diode before the gate current falls to the current tail level.

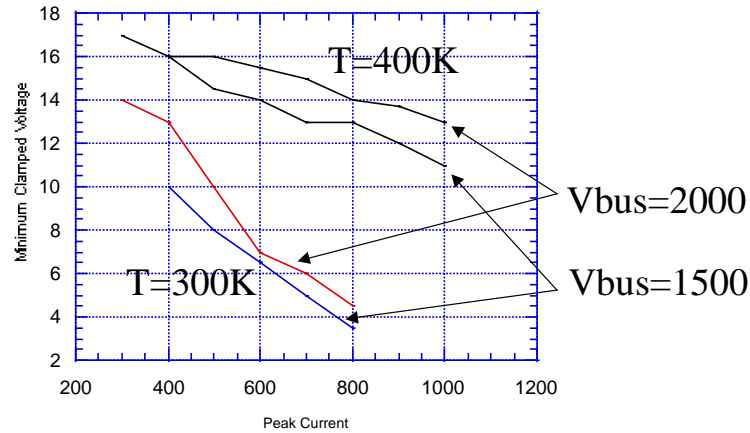


Figure 65: Clamped voltage compared to turn-off current

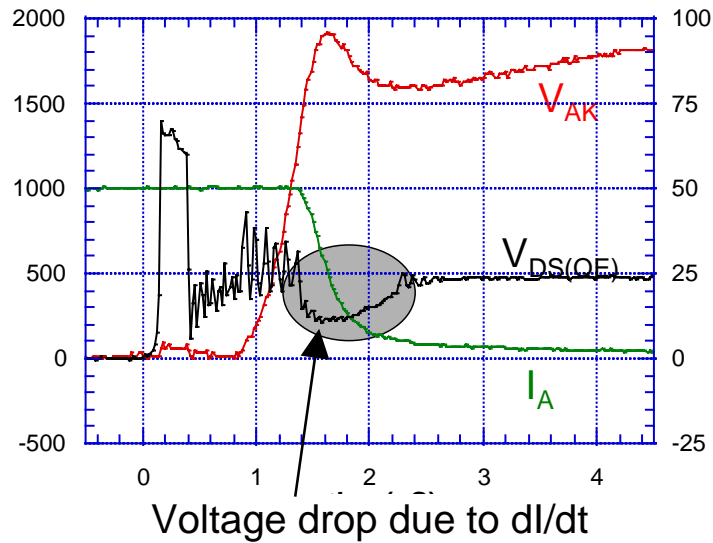
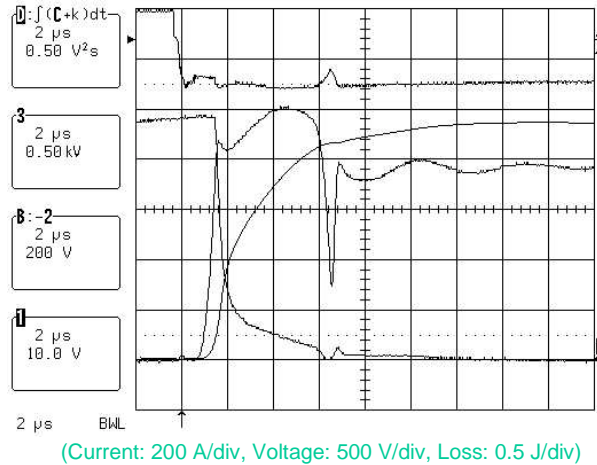


Figure 66: Detail of emitter switch voltage during turn-off transient

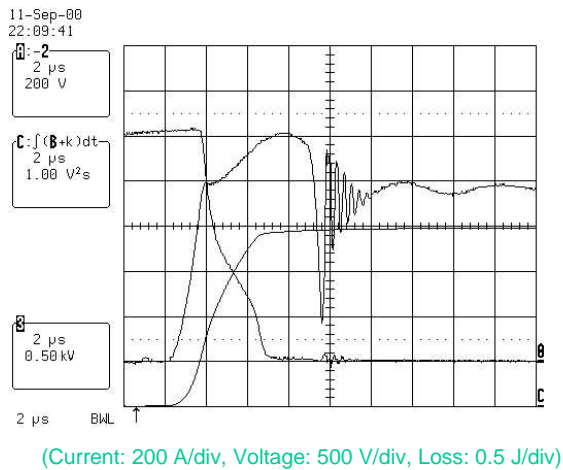
The best case for this clamp is when the gate loop inductance is very low. In this case, the gate current can fall as quickly as the anode current, so there is no need for any current to be provided into the cathode. For a conventional GTO this is nearly impossible, as the anode current falls very quickly once the unity-gain turn-off initiates. However, the transparent anode devices such as the IGCT have a slower current fall and a higher initial current tail value, which makes them ideally suited to making ETOs with reduced gate driver stress. For comparison, the turn-off of a normal (anode shorted) ETO and a transparent anode ETO are shown in Figure 67 and Figure 68. As can be seen, the current fall of the transparent anode device is much slower,



and the current tail has a higher initial value, but it also has a shorter duration current tail. The current required from the gate driver's voltage clamp circuit is reduced to about 50% of the normal ETO's value in the transparent anode device.



**Figure 67: Normal (anode shorted) ETO turn-off**



**Figure 68: Transparent anode ETO turn-off**

The active voltage clamp is implemented by means of a capacitor bank and a switch which is connected to the drain of the emitter MOSFETs. This switch is kept off when the ETO is on and turns on when the ETO needs to turn off. The switch is implemented by a MOSFET in series with a diode, which allows the emitter switch voltage to rise to a high value during current commutation but to drop no lower than the capacitor voltage while the ETO is off. A simplified diagram of the clamp is shown in Figure 69. The primary concern in the design of this clamp is

to minimize inductance and provide adequate current handling capability. For these reasons, the clamp is implemented by paralleling many capacitors, MOSFETs, and diodes. In this way the package inductances appear in parallel so the effective inductance is greatly reduced.

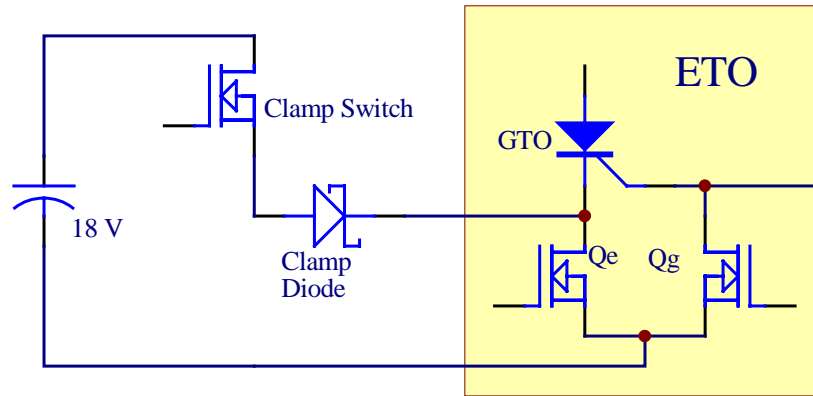


Figure 69: Voltage clamp schematic

#### 6.4 GTO Turn-On Current Injection Section

To provide the required current waveform into the GTO's gate, two circuits are used. One circuit uses a MOSFET switch to provide a large pulse of current into the GTO's gate which is limited by a small inductor. This MOSFET is gated very briefly and then a freewheeling diode allows the inductor energy to continue to provide high current into the GTO gate for about 20  $\mu$ s after the MOSFET turns off. This pulse current source receives energy from the same capacitor bank used for the active voltage clamp. A DC current source is implemented by means of a DC/DC converter which runs in current control mode. This converter runs constantly and its output is shunted by the MOSFETs connected to the GTO gate when the ETO is off, and flows into the GTO's gate when the ETO is on. The pulse current source is shown in Figure 70.

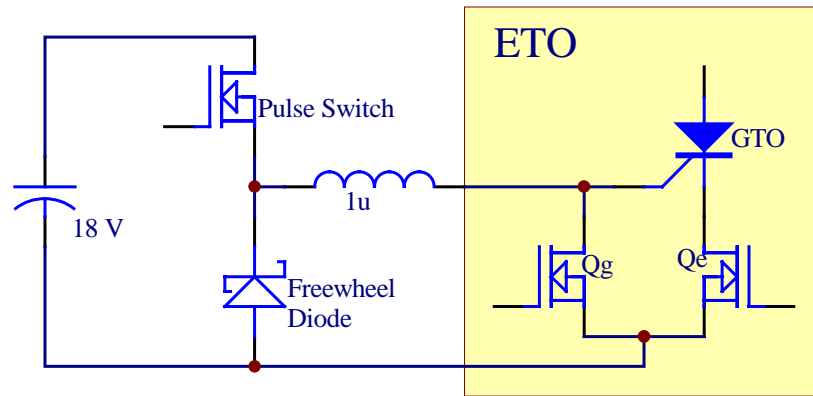


Figure 70: Pulse current source

The driver as designed is shown in Figure 71, along with the ETO4060. This driver requires a separate, isolated DC supply to provide the multiple voltages required for operation. The next logical step in the design of the ETO driver is to integrate the power supply on board.

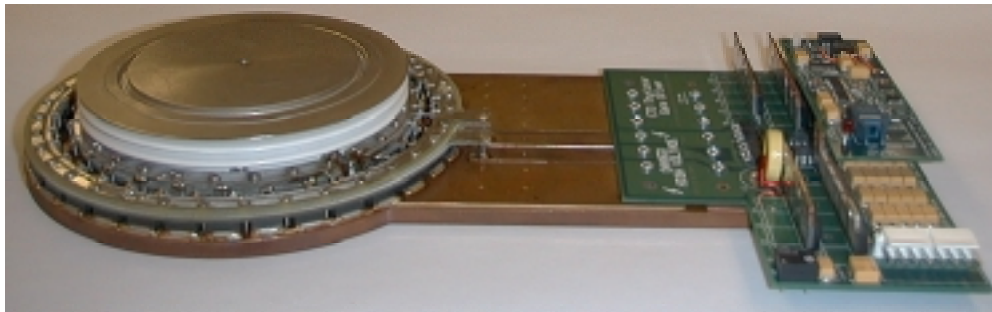
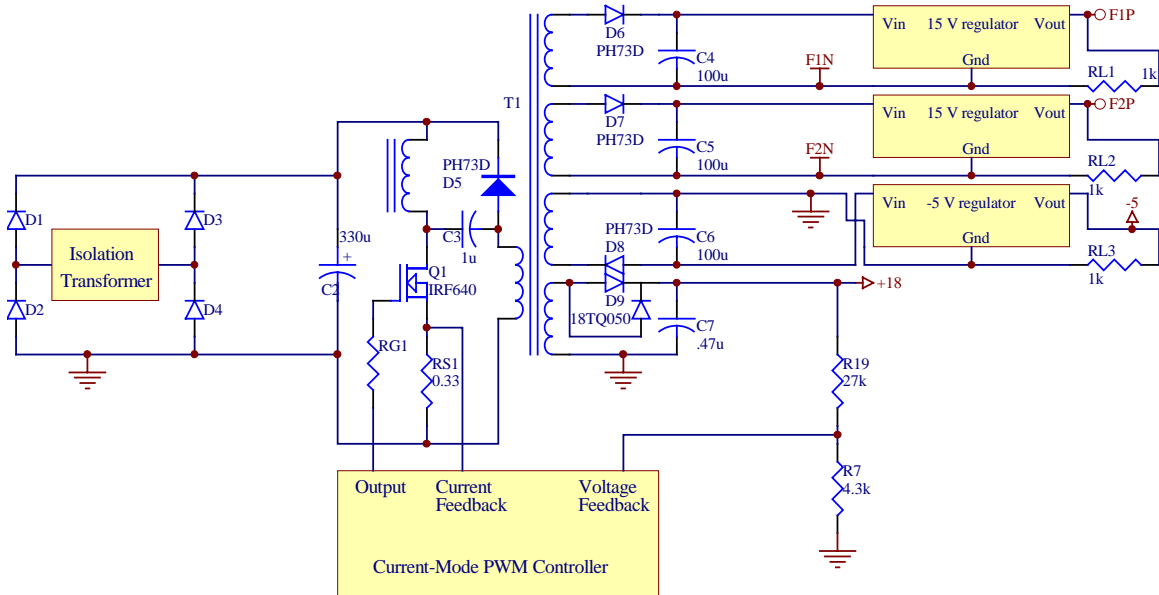


Figure 71: ETO4060 and 1<sup>st</sup> generation gate driver

## 6.5 Power Supply Section

The power supply for the current ETO driver needs to provide several voltage levels, as well as a constant current source. In order to simplify the power supply design, a flyback converter with multiple secondary windings was selected to provide the voltage regulation. The primary power consumption of the ETO gate driver is the voltage clamp and the pulse current source, which share the same 18 V power supply. Therefore this output was selected to be the one regulated by feedback control of the flyback converter, while the other windings use linear

regulators. The primary circuit of the flyback converter, shown in Figure 72, uses two windings and a capacitor to recover leakage and magnetizing energy as detailed in [20]. With this design, efficiency is very good and the flyback switch operates at nearly room temperature with natural convection and no heatsink at full load, which allows for reduced space required on the driver board.



**Figure 72: Double-primary flyback converter**

The constant current source is implemented by means of a forward converter operating in constant current mode. This converter features the same double-primary clamp circuit as the flyback converter, and the forward switch also operates at room temperature without a heatsink. Both of these power converters will be integrated with the gate driver on a single board in a newer design, which is shown in Figure 73 and Figure 74.

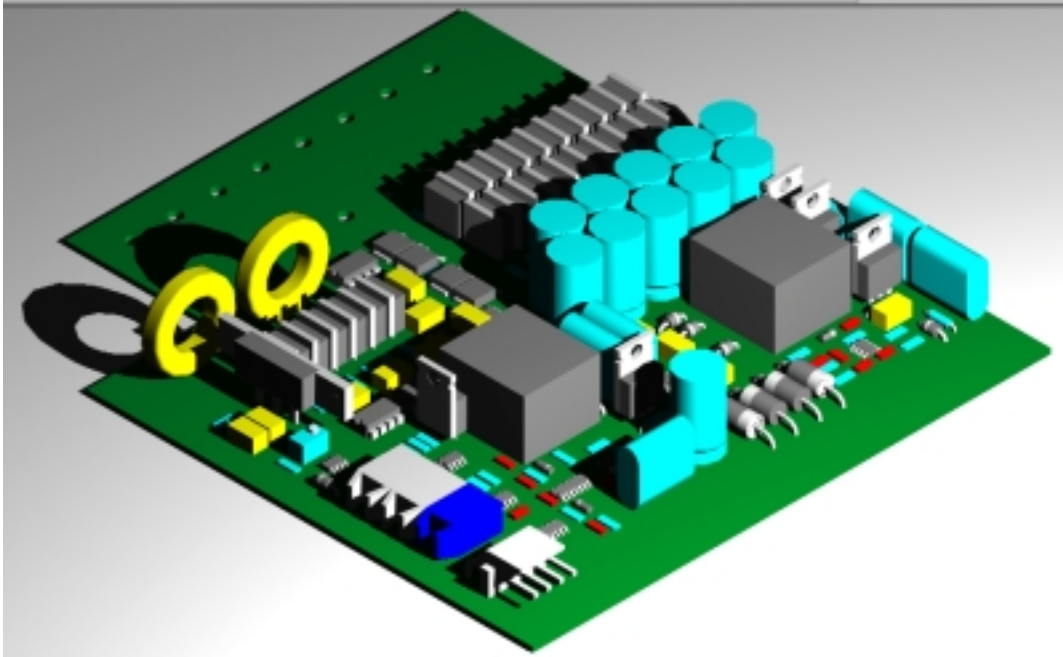


Figure 73: Newer design ETO gate driver with onboard power supply

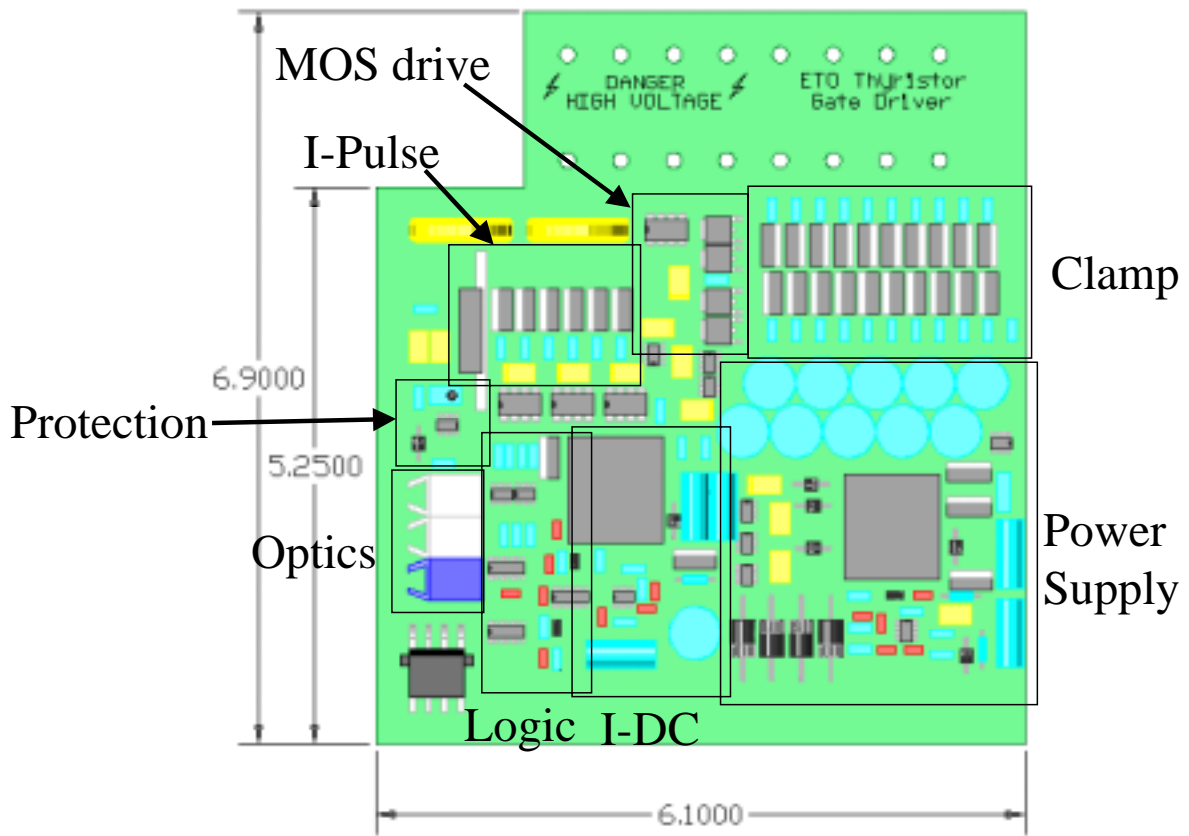


Figure 74: Dimensions of the new gate driver (in inches)

These two converters are not easily capable of meeting the isolation requirements for the ETO while still maintaining closed-loop control, since the feedback would have to cross the isolation boundary. For this reason, the isolation for the gate driver is provided by a high frequency transformer driven by a central inverter. There is a single such inverter power all of the gate drivers in a system, so this can be thought of as a high-frequency AC distributed power system. The central inverter is an IGBT-based full bridge, which switches at 50 kHz and generated a 300 V square wave, which is used to drive the isolation transformer for each gate driver. This inverter is shown in Figure 75 and Figure 76.

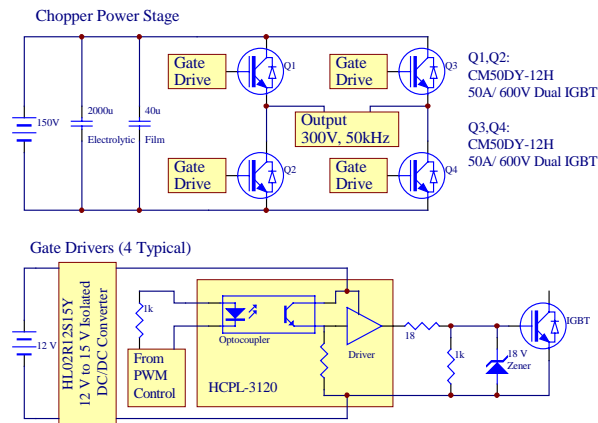


Figure 75: 300V, 50 kHz inverter



Figure 76: Gate driver inverter hardware

# Chapter 6 – Gate Driver Design

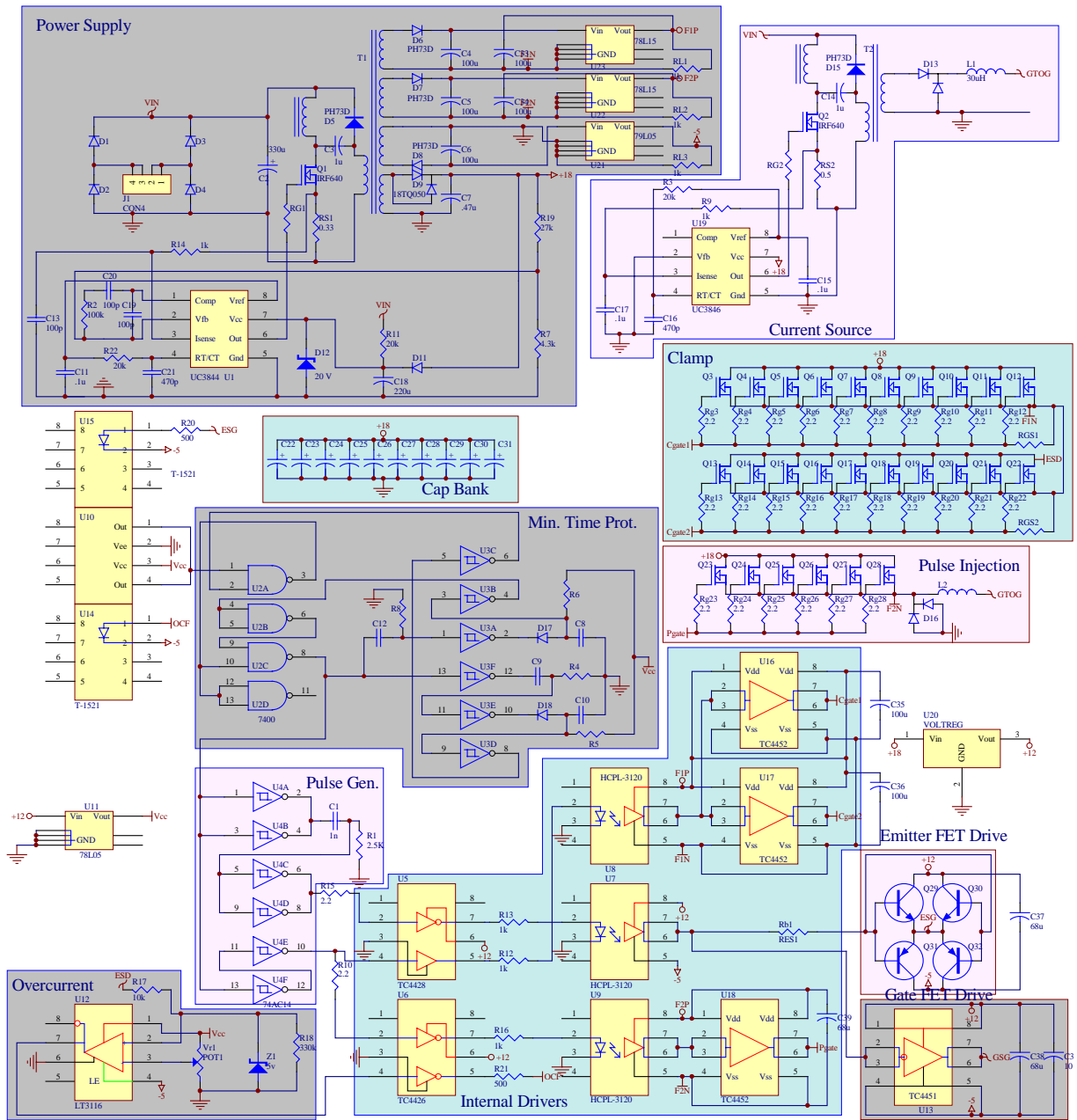


Figure 77: Complete ETO gate driver schematic

## Chapter 7 - Soft Switching for High-Power Devices

### 7.1 Introduction

To improve the switching frequency and current handling capabilities of the high-power devices, soft switching may be useful. Soft switching techniques use auxiliary resonant components in order to decrease or eliminate the overlap between voltage and current at switching transitions. Many soft switching techniques have been developed, and can be broadly classified into Zero Voltage Transition (ZVT) and Zero Current Transition (ZCT) types. The ZVT type soft switching circuits reduce the voltage across the switch to zero before it turns on, so there is reduced turn-on loss. With these ZVT circuits a snubber capacitor can be directly connected across the switch instead of an RCD snubber, so the turn-off loss can be reduced as well. ZCT circuits normally divert the current through the switch to zero before the switch turns off, so the turn-off loss is greatly reduced. Some ZCT circuits have been proposed [16, 17] which also help reduce the turn-on loss and the diode recovery. For application in the high power region, the following characteristics are desired for a soft switching circuit:

- Low auxiliary parts count
- Soft turn-off for the diodes – the diode turn-off is a major problem at high voltage
- No coupled inductors – these are bulky for high-power applications
- No saturable reactors – these are impractical to make at high current
- Soft switching for the auxiliary switches as well as the main switches
- Reasonable voltage stress on the resonant capacitor(s)
- Low number of auxiliary circuit operations
- Minimal impact on inverter modulation schemes
- Tolerance to mistakes in auxiliary timing without destructive failure

The soft switching topologies developed for inverters can be classified into AC-side resonant circuits and DC-side resonant circuits. The AC-side circuits add an auxiliary bridge for each main bridge, but the operation of each phase does not impact the other phases. DC-side soft switching uses a single auxiliary circuit connected in the DC bus to provide soft switching for all



of the main switches. The DC-side soft switching requires less auxiliary switches but these switches must work every time any phase switches, so the frequency of the auxiliary switches is higher than that of the main switches. DC-side soft-switching also requires modification to the control scheme of the inverter, because the operation of the phases is no longer independent.

## 7.2 ARCP Inverters

One AC-side Zero Voltage soft switching technique, the Auxiliary Resonant Commutated Pole (ARCP) circuit [25] has been tested by ABB with IGCT-based inverters [19]. The performance of the IGCTs was good under the soft switching condition, but there is no tolerance for mistakes in timing. If the auxiliary circuit misses a pulse, then there is no reactor in series with the DC link to limit the reverse recovery of the diode, so destruction is likely. Also, the  $dI/dt$  reactor in the DC link helps limit fault current if there is a short circuit applied to the output of the inverter. Based on the test results in [19], the turn-off losses for the main devices were decreased significantly, and the total loss in the converter was reduced by up to 37% compared to a snubberless inverter of the same power rating. However, the problem with the lack of fault current tolerance makes the ARCP inverter risky for use in high power applications, where reliability is more important than efficiency. The efficiency of the inverter tested by ABB was 98.9% snubberless, and 99.3% with ARCP, so the efficiency is good regardless.

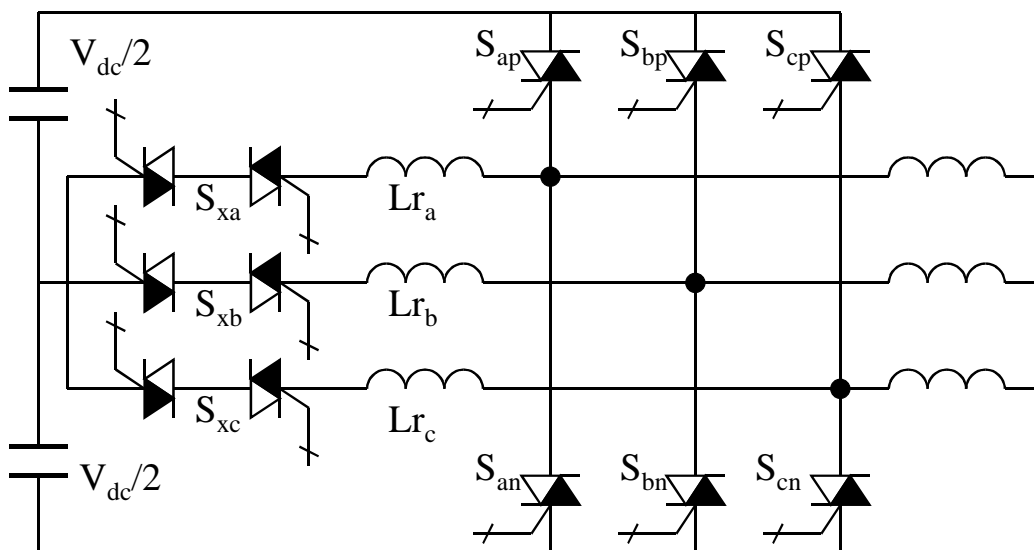


Figure 78: ARCP inverter with reverse-conducting IGCTs

### 7.3 Quasi-Resonant DC-Link Three-Level Inverter

In order to solve the problem of the fault current tolerance, a topology with an inductor in series with the DC link is appropriate. One such topology, a 1.5 MVA quasi-resonant DC-link inverter, was tested with IGCTs as the main switches [18]. The tested circuit is shown in Figure 79. This circuit is a DC-side zero voltage type soft switching, where the link voltage is resonated to zero before a switch turns on, and the resonant helps reduce the turn-off loss. The results for this circuit showed that although the resonant action reduced the switching losses in the main switches to about 50% of the hard switching losses, the high losses in the auxiliary switches are enormous. The tested inverter had auxiliary circuit losses that were 10 times higher than the losses in the passive clamps of conventional inverters, so the total losses of the inverter were 55% higher than in a normal snubberless inverter. Clearly, the quasi-resonant DC-link inverter is not useful for high-power applications, although it does possess the desired short-circuit current limiting inductor which the ARCP circuit lacks.

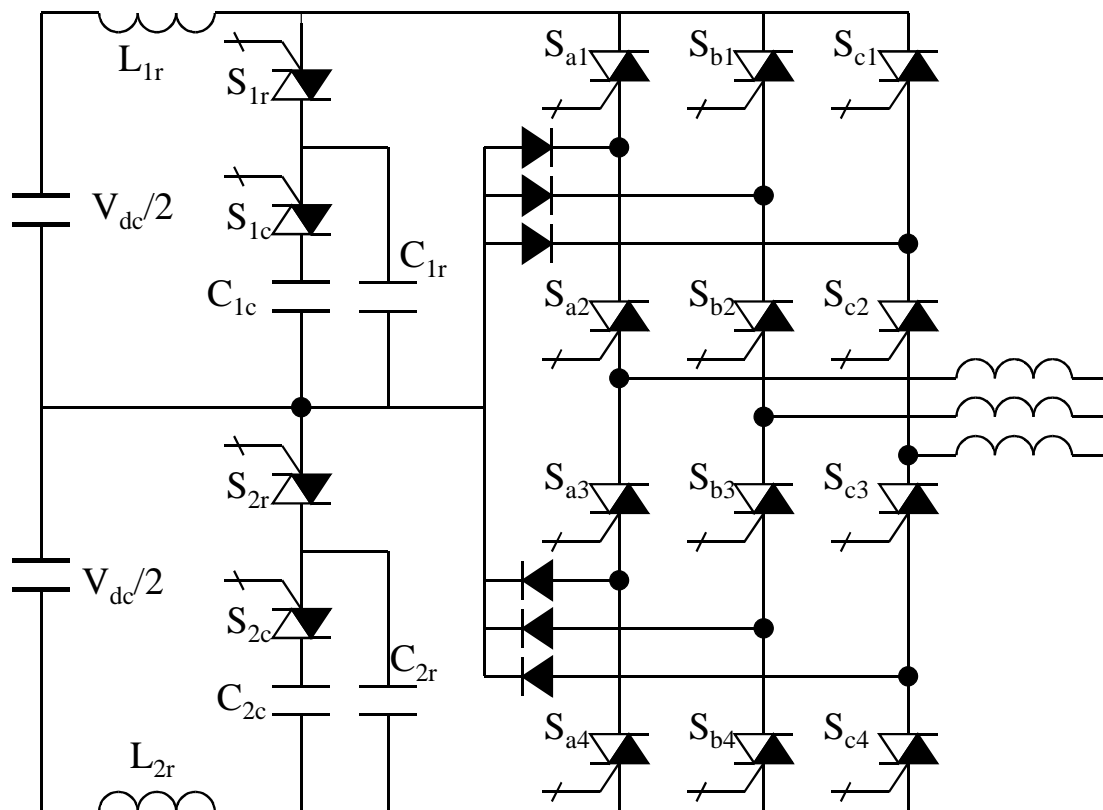


Figure 79: Quasi-resonant DC-link 3-level inverter with reverse-conducting IGCTs

## 7.4 Zero Current Transition Circuit

Testing results for IGBTs, ETOs, and IGCTs have shown that the decrease in turn-off loss by the addition of a snubber is not extremely large, especially as the current increases. For example, the typical reduction in the loss for the ETO4060 is 50% when using a 3  $\mu\text{F}$  snubber capacitor compared to the hard turn-off loss. Although this reduction in loss is not negligible, a ZCT circuit is expected to reduce the turn-off loss more dramatically. In addition, some advanced ZCT circuits also provide soft commutation for all diodes and auxiliary switches [16, 17]. One such circuit is shown in Figure 80. In this circuit, the bottom main switch is assisted by the top auxiliary switch at turn-on, and by the bottom auxiliary switch at turn-off. Likewise, the top main switch is assisted by the bottom auxiliary switch at turn-on, and by the top auxiliary switch at turn-off. This distributes the stress on the auxiliary switches throughout the line cycle, which is important in motor drive applications where the AC frequency can be quite low.

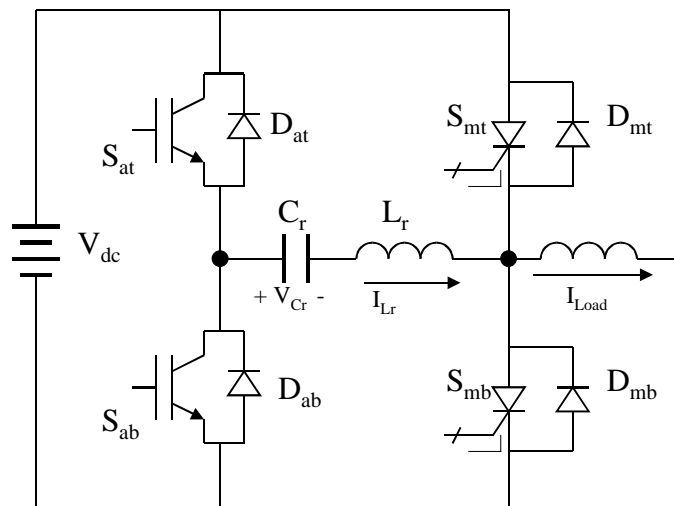
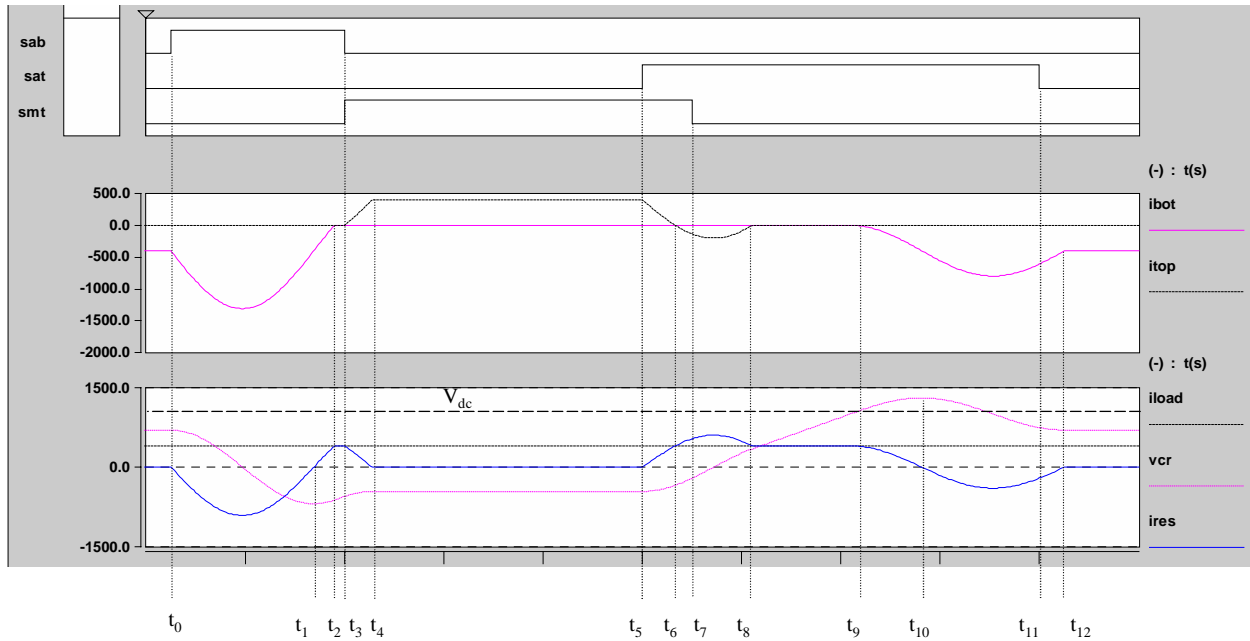


Figure 80: ZCT circuit considered with ETOs (main) and IGBTs (auxiliary)

## 7.5 ZCT Circuit Operation Principle

The theoretical operational waveforms for this circuit are shown following in Figure 81.



**Figure 81: ZCT Circuit theoretical waveforms**

The operation of this circuit is explained in [16]. The summary of the operation is repeated here for convenience in understanding the circuit. The operation of the circuit can be understood by looking at the two transitions, turn-on and turn-off. The waveforms used for demonstration refer to the top main switch carrying current, such that the inverter is delivering current into the load. The load was considered to be a constant current source for simplicity. Polarities of voltages and currents are as shown in Figure 80. The topological states of the circuit during turn-on are shown in Figure 82, and the states during turn-off are shown in Figure 83.

Initially the resonant capacitor is charged with a positive voltage and the bottom main diode is carrying the load current. When the decision is made to turn on the top main switch, the resonant circuit prepares for the transition by turning the bottom auxiliary switch on at time  $t_0$ . At this time, the voltage applied to the resonant inductor is the resonant capacitor's voltage, so the current will increase. This current flows through the main bridge, and increases the current through the main diode. This current also begins to discharge the resonant capacitor, so its voltage decreases and becomes negative. At time  $t_2$ , the resonant half-cycle is complete, and the resonant current returns to zero. However, the resonant capacitor's voltage is now negative and

greater in magnitude than the bus voltage, so the resonant current will be driven in the other direction. As the resonant current becomes larger, the current through the main diode begins to decrease. The auxiliary switch is no longer carrying the current, as it is instead carried by the antiparallel diode  $D_{ab}$ . In this way the auxiliary switch has achieved zero-current turn-off. At time  $t_2$ , the resonant current become equal to the load current, so the main diode is no longer carrying any current at all. The main diode has now achieved zero-current turn-off. Since the main switch has not turned on yet and the diode has turned off, the load current now flows through the resonant tank instead of through the main bridge. This constant current results in linear charging of the resonant capacitor. This continues until  $t_3$ , when the top main switch turns on. At the same time, the gate drive for the auxiliary switch is removed, as this switch has not carried current since  $t_1$ . The voltage applied to the resonant inductor is now equal to the difference between the resonant capacitor's voltage and the bus voltage, which is relatively small. The resonant inductor current discharges and reaches zero at  $t_4$ , and the main switch current increases to the load current at the same time. At  $t_4$ , the auxiliary diode turns off at zero current and the resonant action stops. The main switch is now carrying the full load current. Due to the slow increase in the current of the main switch combined with zero- or reduced-voltage turn-on, the switching loss of the main switch at turn-on is negligible, since it is only due to conduction loss.

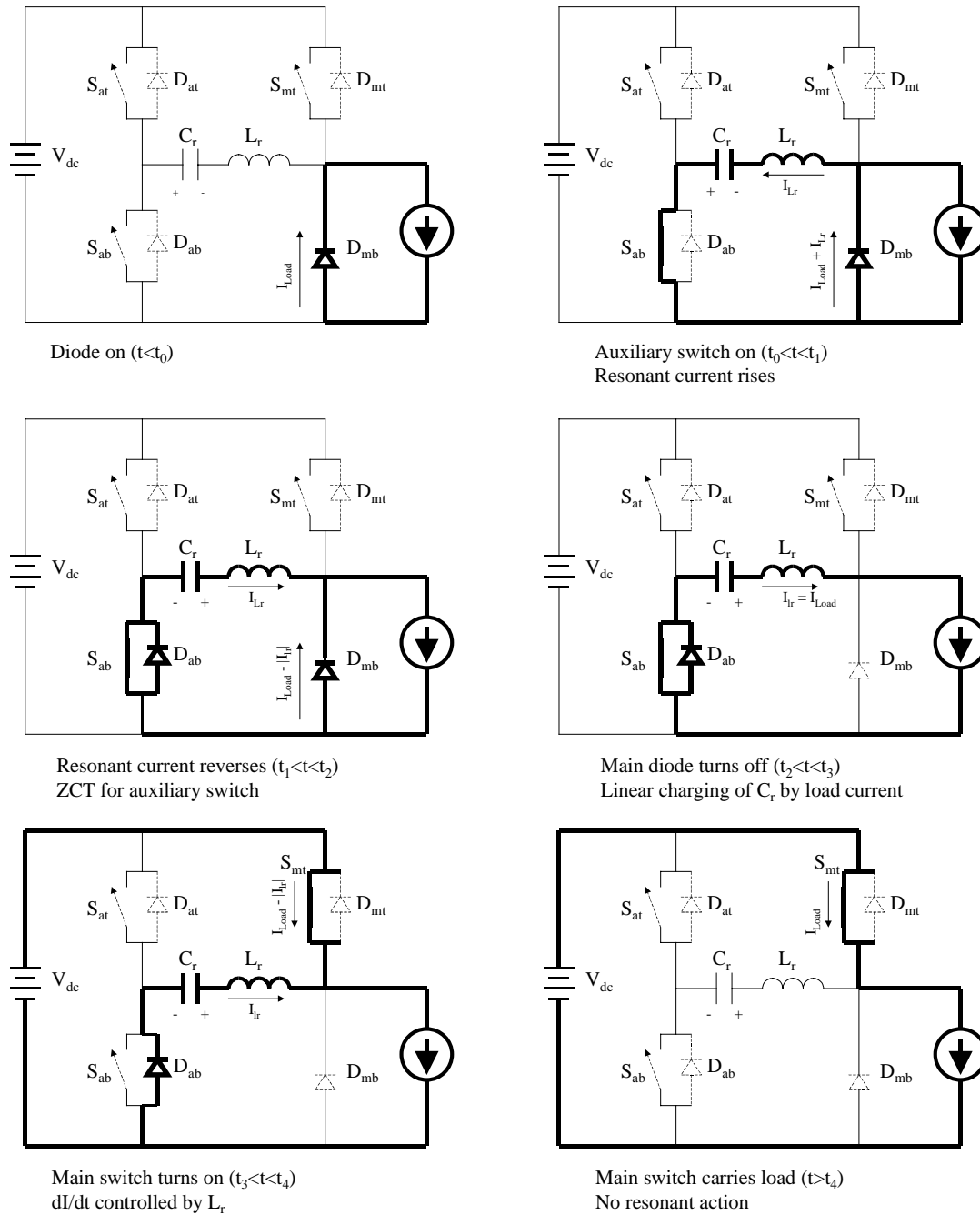


Figure 82: ZCT topological states during turn-on

When it is time to turn off the main switch, the top auxiliary switch is activated at time  $t_5$ . At this time, the resonant capacitor's is applied to the resonant inductor, so the resonant current begins to build and flows toward the main bridge. The current through the main switch decreases as the resonant current builds, and at  $t_6$  the main switch current reaches zero. Since the

resonant action continues to increase the resonant current, the main switch's antiparallel diode begins to conduct the current. A short time later, the gate drive signal for the main switch is removed at  $t_7$  since the main switch does not need to carry current now. The resonant cycle continues until  $t_8$ , at which point the resonant current is equal to the load current. The main switch's antiparallel diode now turns off at zero current. The resonant cycle cannot continue since the main switch is off so there is no way for the resonant current to flow other than through the load. The load current continues to linearly charge the resonant capacitor until  $t_9$ , when the resonant capacitor's voltage becomes equal to the bus voltage. At this point, the voltage across the resonant inductor is zero because the current is constant, so the voltage across the main diode is equal to the difference between the bus voltage and the resonant capacitor voltage. Since this difference is zero and trying to become negative, the main diode begins to turn on. Once the main diode begins to turn on, the resonant inductor's current is no longer forced to follow the load current. At this point, a resonant cycle begins where the resonant inductor's current begins to decrease and the resonant capacitor's voltage continues to increase. At time  $t_{10}$ , the resonant inductor's current reaches zero and the resonant capacitor's voltage reaches a peak. The resonant cycle continues, with the current now being carried by the auxiliary switch's antiparallel diode instead of the switch. The auxiliary switch's gate signal is removed at  $t_{11}$ , while the diode is conducting so the auxiliary switch has achieved zero-current turn-off. The resonant cycle continues until the resonant current returns to zero at  $t_{12}$ , where it remains until the next switching event for the main switch.

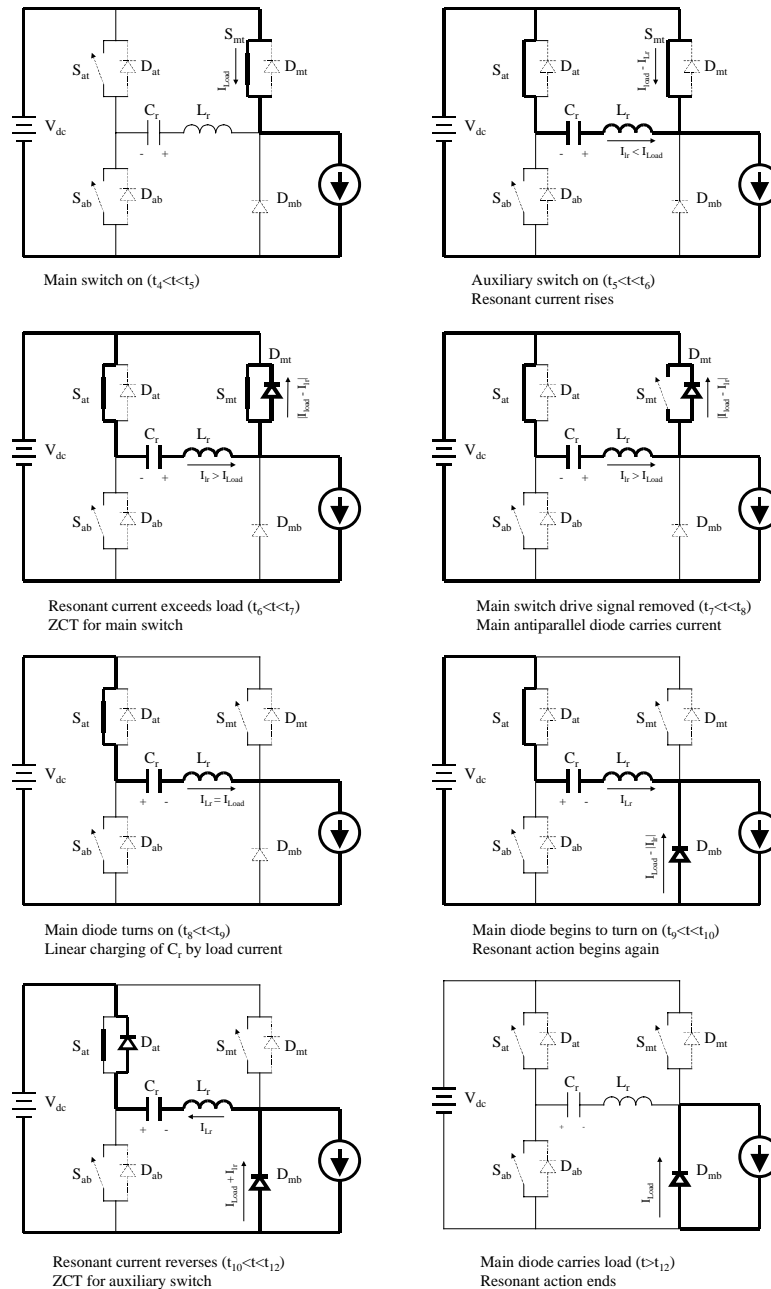


Figure 83: ZCT topological states during turn-off

## 7.6 ZCT Test Setup

In order to verify the operation of this ZCT circuit with high-power devices, a prototype was developed. With high voltage diodes, reverse recovery can be severe so it was expected that the operational waveforms of the prototype would differ somewhat from the theoretical waveforms with ideal diodes. The first step in the design of the ZCT test circuit was to design



the resonant components. Using the design procedure outlined in [16], the circuit can be designed. The requirement for achieving ZCT operation is that the resonant current peak must be higher than the highest output current. With this requirement in mind, one design parameter  $k$  is defined as:

$$K = \frac{I_{rpk}}{I_{max}} \quad 7-1$$

For proper operation,  $k$  should be at least 1.1 so the resonant current will exceed the main current. Next, the characteristic impedance  $Z_0$  of the resonant tank is defined as:

$$Z_0 = \frac{V_{dc}}{K * I_{max}} \quad 7-2$$

In addition, the resonant time period  $T_0$  must be selected. In order to reduce the switching losses, this period should be related to the carrier lifetime in the semiconductors so that the remaining free carriers will mostly recombine before voltage is reapplied to a switch or diode after turn-off. The resonant time constant  $T_0$  also controls the  $dI/dt$  of the diode current at turn-off of the diodes, so a longer  $T_0$  is desirable, so long as it does not cause excessive limitations on the duty cycle due to time occupied by the resonant processes. With these parameters determined, the resonant tank can be designed by the following equations:

$$L_r = Z_0 \frac{T_0}{2\pi} \quad 7-3$$

$$C_r = \frac{L_r}{Z_0^2} \quad 7-4$$

For the test circuit constructed, a DC bus voltage of 2 kV and a maximum load current of 1600 Amps were considered. The resonant time period  $T_0$  was selected to be 30  $\mu$ s in order to achieve a low  $dI/dt$  for the turn-off of the diodes. In order to have a significant margin for ZCT,

K was set to 1.5. With these parameters, the resonant tank was designed with the following values:

$$L_r = 7 \mu\text{H}$$

$$C_r = 6 \mu\text{F}$$

The resonant inductor is an air-core wound with 8 turns of AWG 2/0, 5000 V insulation motor lead on a 4-inch diameter plastic form. Due to the air-core design, there is no saturation problem for this inductor, so the peak and RMS currents are determined only by the capacity of the windings. The resonant capacitor is an oil-filled metallized polypropylene film capacitor rated at 3000 V DC, 4500 V peak. The resonant capacitor is THY-W4B-6.0-450 from ICAR, which is rated for 150 A RMS, 6000 A peak and has an internal inductance of less than 10 nH, and an internal resistance of 0.15 m $\Omega$  [datasheet].

To test the operation of the ZCT circuit, a test setup was constructed with the described resonant tank and a boost-type converter, which simplifies measurement of the main switch waveforms because it is ground referenced. The main switch tested was the ABB IGCT 35L4503, rated at 4000 Amps and 4500 Volts. This IGCT was selected because it had the highest switching losses and the lowest conduction losses of all the devices tested at that point (the ETO4045A was developed later), so this device seemed the most likely to benefit from soft-switching. The main diode and the antiparallel diode for the IGCT were both ABB diodes, model 5SDF 10H4502, which are high-speed diodes optimized for use with the IGCT. The auxiliary switches were selected as IGBTs from Mitsubishi and EUPEC, both rated at 1200 A, 3300 V. The IGBTs were selected for the auxiliary switches due to the easy mechanical layout of the plastic modules compared to the hockey-puck package stacks, and the simplicity of isolating the gate driver without using the AC distributed bus. Clearly, for practical implementations GTO-derived devices such as the ETO or IGCT would be preferable due to their superior surge current capacities. The schematic of the test setup is shown in Figure 84, and photographs of the test setup are shown in Figure 85 and Figure 86.

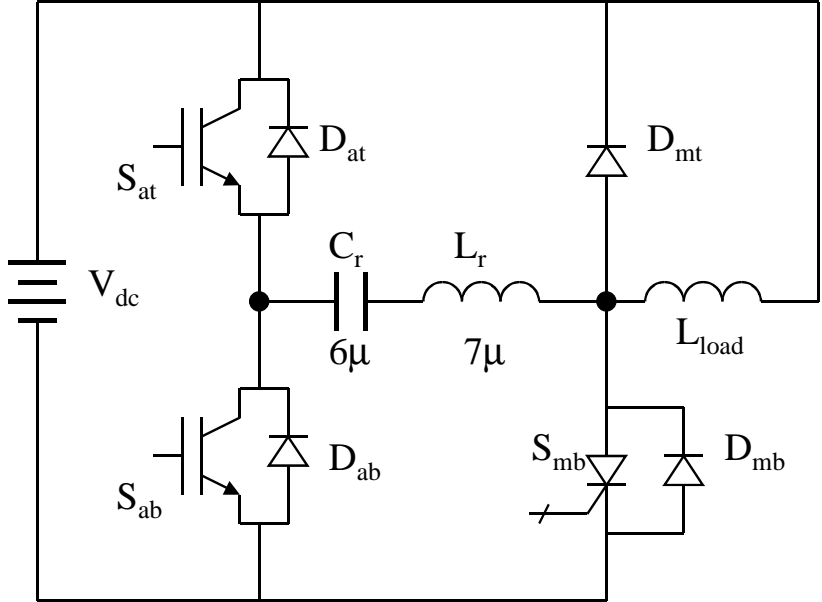


Figure 84: ZCT test setup

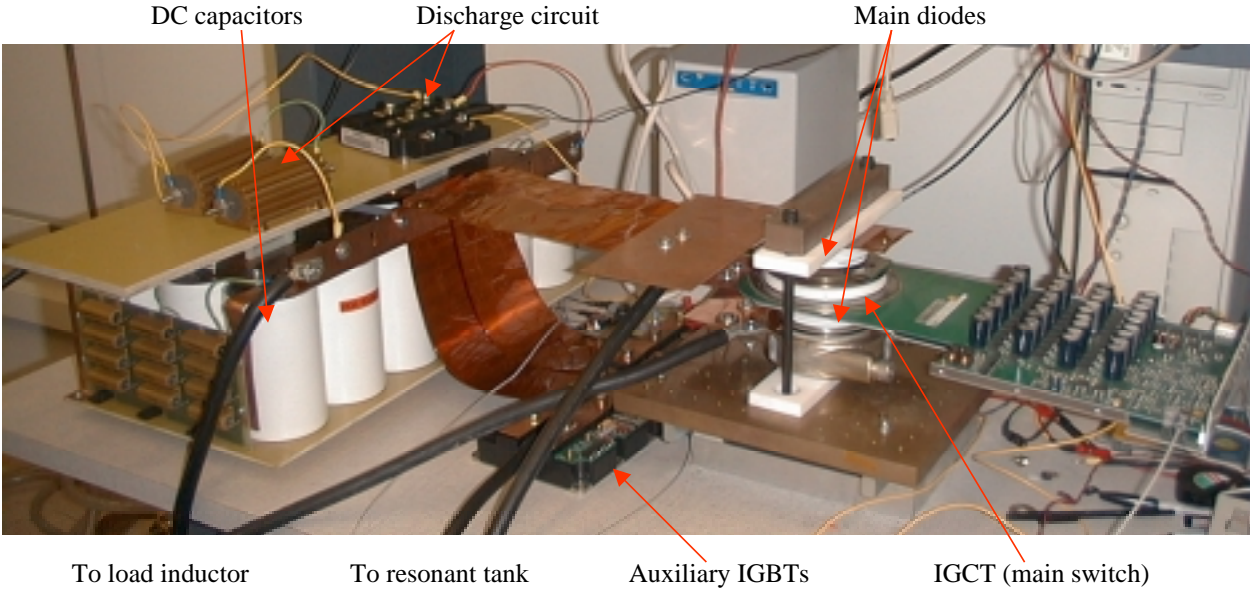


Figure 85: Photograph of ZCT test setup



**Figure 86: Resonant capacitor and inductor**

With the test setup described, the operation of the ZCT circuit was tested with a bus voltage of 1000, and a load current of 350 Amps. The test results show that there are several deviations from the theoretical waveforms. The first deviation is that the load inductor is not large enough to be treated as a constant current source. A very short pulse width is used so that the change in current during the switching cycle is not too significant. Another deviation is that even with the soft turn-off, the high-voltage diodes still exhibit some reverse recovery, although it is dramatically reduced. The energy lost during these recovery events impacts the resonant circuit energy storage.

## **7.7 ZCT Test Results**

The typical operational waveforms for the resonant tank are shown following in Figure 87. These waveforms were taken with the DC bus at 1000 Volts, and the peak resonant capacitor voltage was about 1350 Volts, which is 35% above the bus voltage. This voltage stress is very reasonable, as overshoots of this magnitude are common in hard switching circuits, so the capacitor is easily capable of this stress. The topology described in [17] has a peak stress of 2

times the DC link, so the circuit tested here is clearly superior from this aspect. The reverse recovery of the diodes is clearly visible as disruptions in the resonant current waveform. The primary recovery problems come from the auxiliary diodes, which are visible when the resonant current reaches zero at the end of the resonant cycles.

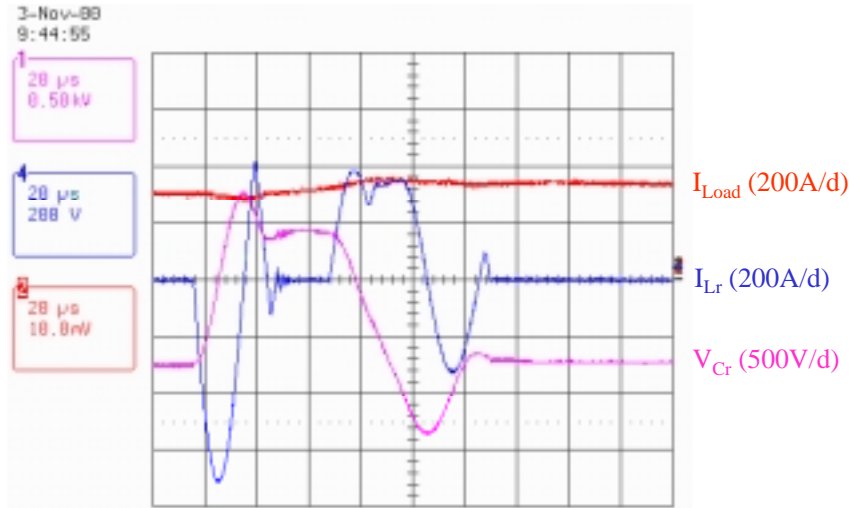


Figure 87: Resonant tank waveforms

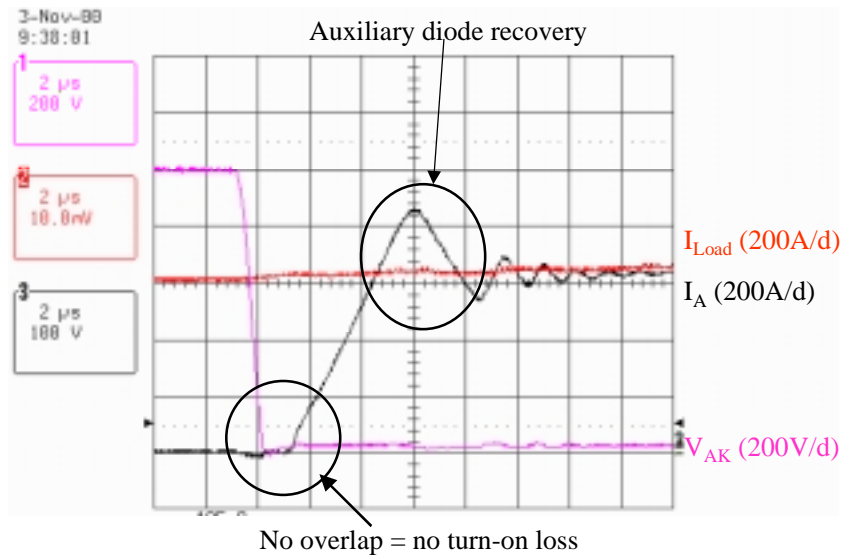
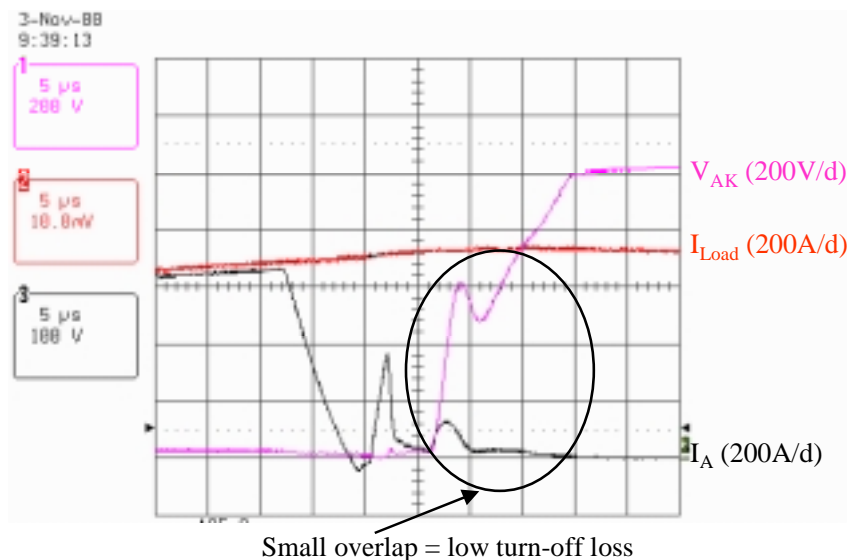


Figure 88: Main switch turn-on waveforms

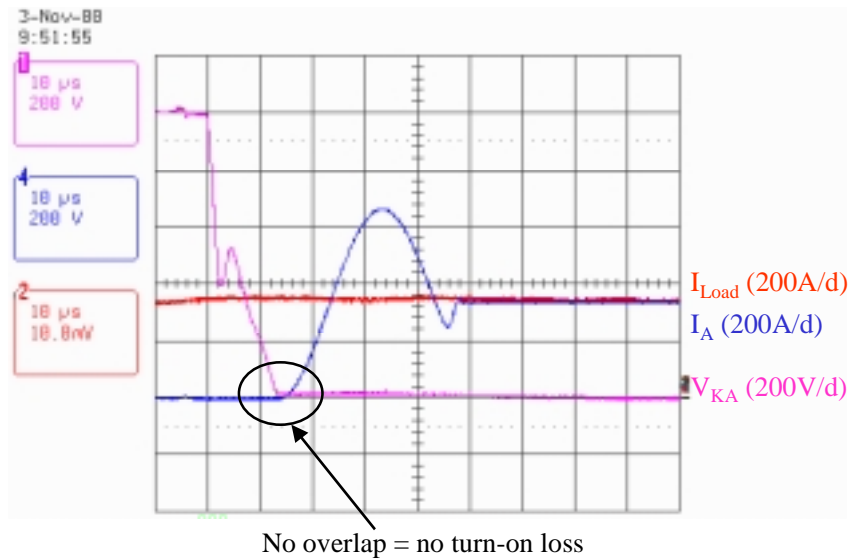
The waveforms for the turn-on of the main switch are shown in Figure 88. As can be seen, the voltage across the main switch decreases to zero about  $1.5 \mu\text{s}$  before the switch begins to carry current. When the current begins to rise, the resonant inductor limits the rate of rise of the current. There is no reverse recovery due to the main diode applied to the main switch, and the turn-on switching loss is nearly zero. There is some reverse recovery effect visible from the auxiliary diode, but the switch is fully on by the time this recovery occurs so the only result on the main switch is a slight increase in conduction loss during this time. The ZCT circuit has solved the turn-on problem of the main diode, which normally requires lossy snubbers. It is important to remember that with current high-voltage diode technology, a completely hard commutation is simply not possible, so the  $di/dt$  must be controlled by either a resonant circuit or a passive snubber.



**Figure 89: Main switch turn-off waveforms**

The turn-off characteristics of the main switch are also dramatically improved by the ZCT circuit, as shown in Figure 89. There is no voltage overshoot at all beyond the DC bus, which is much better than the case in hard switching or the use of a capacitive snubber. The current is resonated to zero by the auxiliary circuit, at which point the gate driver for the IGCT is given the command to turn off. The current pulse immediately following the turn-off command is the circulating current from the gate driver which was discussed in chapter 6. This circulating

current is not responsible for any switching loss, since the voltage is still near zero during this stage. When the voltage begins to rise, the  $dV/dt$  is limited by the charging of the resonant capacitor. There is some current which flows during the voltage rise phase. This current is due to a combination of factors. The first factor is that for a large area device such as the IGCT, a significant output capacitance must be charged in order to establish the depletion region to support voltage. Another component of this current is the free carriers which had not recombined being swept from the junction. The current is much lower than the current tail in hard switching, and the period of high power stress when full voltage and full current are applied during hard switching is not present. The switching loss of the IGCT was reduced to 70 mJ at 350 Amps turn-off into a 1 kV bus, which compares very favorably to the hard-switching loss of 650 mJ at the same level. This represents an 89% reduction in turn-off losses for the IGCT as well as the removal of the dangerous high-stress overlap region. The  $dV/dt$  is also significantly reduced, so the EMI and stress on a motor load may be reduced as well.

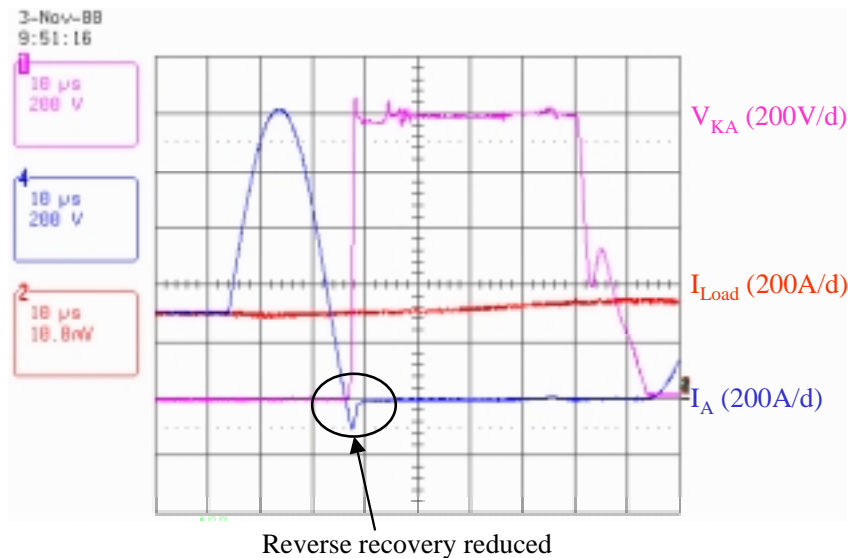


**Figure 90: Main diode turn-on waveforms**

The main diode is also very important to aid with soft-switching. The turn-on of the main diode is shown in Figure 90. As can be seen from this figure, the voltage of the diode reduces to zero before the diode begins to turn on. Because the resonant circuit limits the rate of rise of the current, no forward recovery (high initial conduction loss) effects are associated with

this transition. The peak current about twice as high as the load current, but a short current pulse is easily handled by the diode, as diodes have excellent surge current capacities.

For the main diode, turn-off is much more problematic than turn-on. If it is not handled, the reverse recovery can lead to catastrophic failure of a system. The ZCT circuit tested has the advantage of being able to allow a soft turn-off for the main diode, as shown in Figure 91. The resonant current adds to the load current, so the peak current stress in the diode is quite high. However, the diode has no problem with surge current, and the switching loss is dominant over the conduction loss for high-power diodes. The resonant circuit brings the current to zero slowly, so the diode's reverse recovery is reduced.

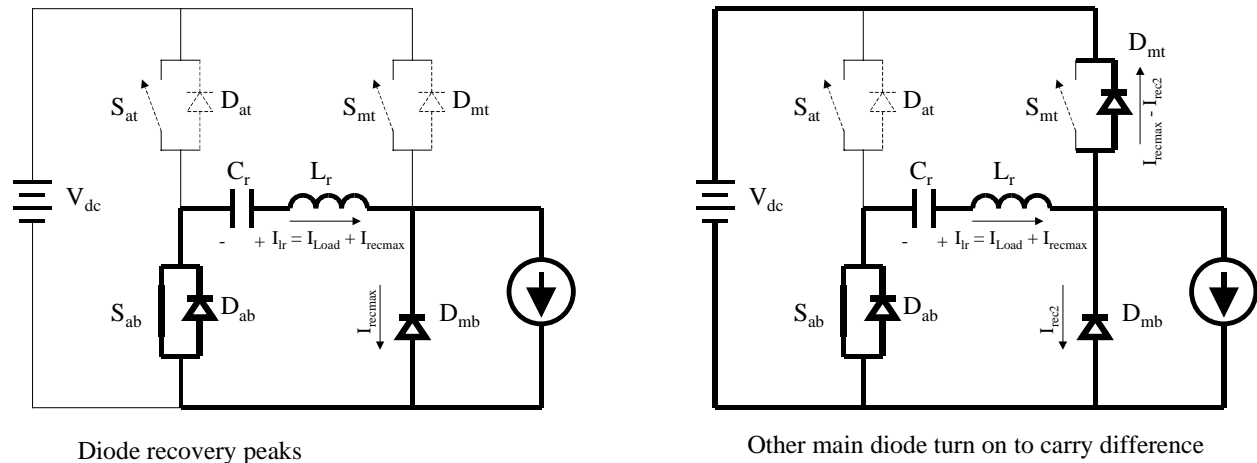


**Figure 91: Main diode turn-off waveforms**

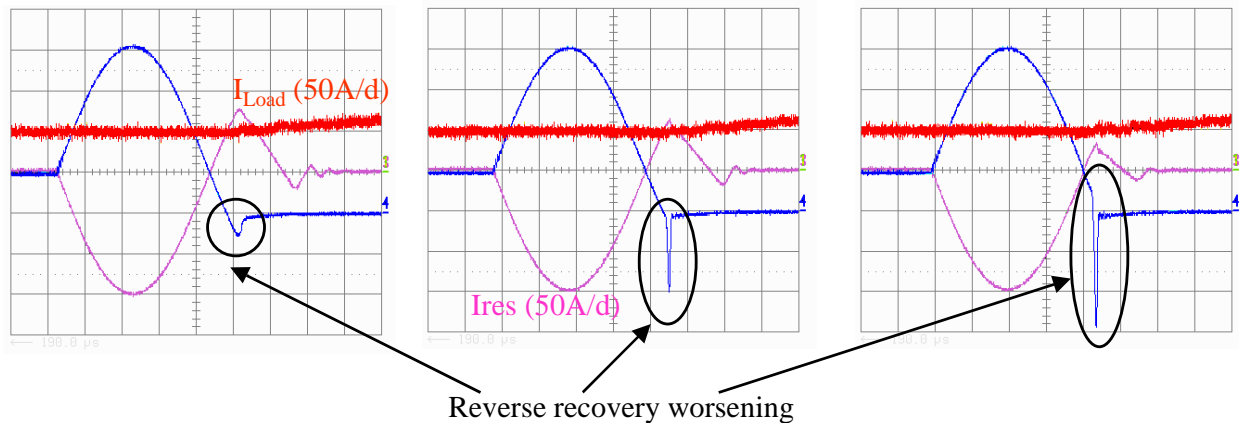
The main drawback is that the voltage across the diode immediately snaps to the full DC bus voltage as soon as the reverse current reaches its peak and begins to decline. The reason for this is obvious from an analysis of the circuit. With the load current assumed to be constant and the resonant current being unable to change instantly, the only way for the diode's current to snap back quickly is if another path opens to take the difference between the load current, resonant current, and the recovery current. The path that opens is the other main diode, which turns on immediately when the recovering diode's current begins to decrease. The circuit during



this phase is shown in Figure 92. The turn-on of the other main diode due to the reverse recovery of the outgoing diode causes the voltage across the incoming main switch to decrease to zero before that switch turns on, eliminating the turn-on loss for the switch.



**Figure 92: Reverse recovery process for main diode**



**Figure 93: Diode recovery trends as control timing decreases (l to r)**

The reverse recovery of the main diode is very sensitive to the control timing. Figure 93 shows the reverse recovery of the main diode as the auxiliary timing is decreased. The first waveform shows correct timing, where the reverse recovery effect is minimal. The middle figure shows the critical timing, where the diode current reaches zero just as the main switch turns on. Clearly, the reverse recovery is much worse, showing that the resonant current must be allowed to exceed the load current. The right figure shows that with the control timing reduced too

much, the diode turns off with forward current still flowing. The reverse recovery current in this case is quite high, although it is still better than completely hard switching. However, as previously mentioned the high voltage diode cannot survive completely hard switching, and it was not judged wise to further decrease the control timing.

Another important feature of the ZCT circuit is its capability to provide soft turn-off for the auxiliary switches. The operating waveforms for the auxiliary switches are shown in Figure 94 and Figure 95. It can be seen that the switch (in this case an IGBT) turns off while the anti-parallel diode is conducting. When the current returns to zero, there is some reverse recovery current from the auxiliary diodes. This current may also be due to the establishment of the depletion region within the auxiliary switch and the removal of remaining carriers from the switch. Because the auxiliary diode is inside the same package as the switch, it is not possible to determine how much of the current is due to the diodes and how much is due to the switches. However, the switching loss for the auxiliary switches is not too high, since they turn off into a reduced voltage. Some ringing occurs during the reverse recovery of the auxiliary diode, but the peak voltage is less than the DC bus for the bottom (turn-off) auxiliary switch, and only slightly (10%) higher than the DC bus for the top (turn-on) auxiliary switch. This ringing is cause for concern about EMI, although it does not appear in the output waveforms for an inverter so it is not a problem for a motor load.

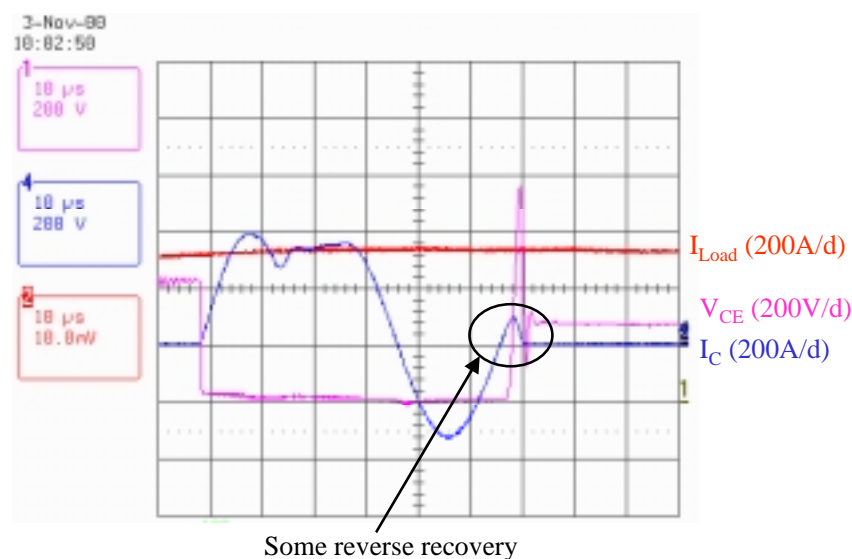


Figure 94: Bottom (turn-off) auxiliary switch waveforms

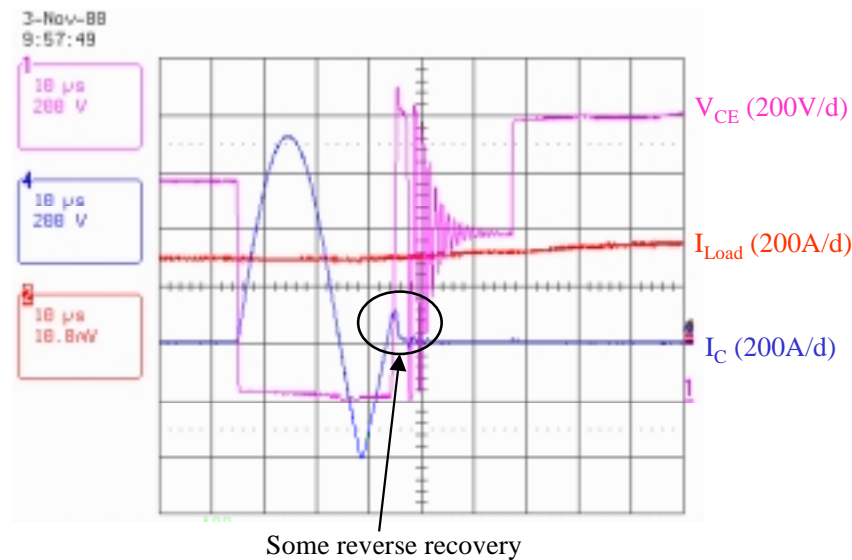


Figure 95: Top (turn-on) auxiliary switch waveforms

## 7.8 Soft-Switching Conclusions

The soft-switching ZCT circuit tested produced promising results. The turn-on loss was almost nonexistent for the main switch, and the main diode's reverse recovery was acceptably small. The ZCT circuit allows the removal of the passive snubbers which are required otherwise in order to control the turn-off of the diode. The turn-off loss of the main switch was reduced 89% compared to hard-switching, and the voltage overshoot at turn-off was eliminated. The IGCT and ETO are particularly well suited for this type of circuit, as they have excellent surge current capabilities and very low conduction loss. The readily available GTO snubber capacitors are suitable for application as resonant capacitors, and the resonant inductor is easily fabricated with an air-core construction. The main issue regarding the proposed ZCT circuit is that there is no inductor in series with the DC-link, so successful commutation of the main diodes requires proper operation of the auxiliary circuit. The  $di/dt$  reactor which is found in hard-switching converters also helps to limit fault currents in the event of an output fault in the inverter, so the removal of this reactor requires additional work in the protection of the system. Overall, the ZCT circuit tested provided all of the benefits that were predicted, although the reverse recovery problem could only be reduced instead of eliminated as hoped. The turn-off loss was also not completely eliminated as the theoretical waveforms predicted, but it was dramatically reduced.

The reverse recovery problem was found to reduce the amount of current which could be soft-switched with the resonant tank, as the recovery energy reduced the energy stored in the resonant tank significantly. Overall, the ZCT circuit seems to be beneficial for high-power devices if a reduction in the switching loss is required. The ZCT circuit is used in place of the conventional RLD turn-on  $di/dt$  snubber, so the power loss associated with that snubber is eliminated as well. Due to the duty cycle loss to the resonant time, this circuit may be more appropriate for increasing the RMS current capacity of a system rather than for increasing the switching frequency beyond a few kilohertz.

## Conclusions

With the new device technology recently developed, the performance of high-power converters can be improved dramatically in terms of dynamics, efficiency, size, and protection, due to the improved switching speed and the removal of the turn-off snubber. The new device technology consists primarily of IGBTs being carried to higher power levels and GTO-derived devices, such as the ETO and the IGCT. The IGBTs are very convenient to use and have very simple gate drive requirements. However, these IGBTs are still much lower in power than the GTO-derived devices. The ETO and the IGCT have switching performance that is almost as good as that of an IGBT, although they have much higher blocking voltage ratings and have much less conduction loss, even compared to an IGBT with a lower voltage rating. The drawbacks for these devices are higher gate drive requirements and slightly worse switching.

The application of the new generation devices generates new problems when they are installed into a practical power converter. The higher  $di/dt$  and  $dV/dt$  that exists in these applications is an EMI concern, and is difficult to address. When the turn-off snubber is removed from the main power switch, the stress on the diode increases as well, since that diode now must withstand the full bus voltage reapplied during reverse recovery, where the switch's  $dV/dt$  snubber conventionally used would protect the diode as well. A new failure mode relating to the parasitic diode of the ETO was found and a solution was proposed and implemented. Additionally, a potential problem relating to a current circulating between an IGCT's driver and its antiparallel diode was identified.

The operation of a practical power converter was demonstrated using the ETO device. This system, a three-phase inverter, demonstrated good quality of the output current waveforms due to its high frequency operation as compared to the traditional GTO-based systems. The efficiency of the ETO-based converter was very high, as is typical with this type of state-of-the-art device. The ETO proved capable of operating without any turn-off snubbers at a high frequency, as predicted.

## Conclusions

When higher frequency operation or higher currents are required, soft switching may be helpful, as it can reduce the switching loss. A Zero Current Transition circuit was evaluated for application with high-power devices, and returned promising results. The turn-off loss was reduced 89% compared to hard switching, although some of the loss was transferred to the auxiliary circuit. All semiconductor devices (switches and diodes) achieved soft turn-off so the stress was not high. Although reliability concerns may limit the application of soft switching in high power systems, specialized applications such as some military uses may benefit from soft switching.

The HVIGBT, ETO, and IGCT offer the possibility for greatly enhanced future high-power converters. The switching times they offer are almost as low as some low voltage IGBTs, and the actual  $dI/dt$  and  $dV/dt$  levels that can exist are even higher than those of typical low-voltage MOSFETs. With the new devices new problems have been identified and solved.

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