HIGH VOLTAGE RESONANT SELF-TRACKING

CURRENT-FED CONVERTER

A Thesis

presented to

the Faculty of California Polytechnic State University,

San Luis Obispo

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

by

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March 2010

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TITLE:	HIGH VOLTAGE RESONANT SELF-TRACKING
	CURRENT-FED CONVERTER

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ABSTRACT

HIGH VOLTAGE RESONANT SELF-TRACKING CURRENT-FED CONVERTER Scott Logan McClusky

High voltage power supply design presents unique requirements, combining safety, controllability, high performance, and high efficiencies. A new Resonant Self-Tracking Current-Fed Converter (RST-CFC) is investigated as a proof-of-concept of a high voltage power supply particularly for an X-ray system. These systems require fast voltage rise times and low ripple to yield a clear image.

The proposed converter implements high-frequency resonance among discrete components and transformer parasitics to achieve high voltage gain, and the self-tracking nature ensures operation at maximum gain while power switches achieve zero-voltage switching across the full load range. This converter exhibits an inherent indefinite short-circuit capability. Theoretical results were obtained through simulations and verified by experimental results through a complete test configuration. Converter topology viability was confirmed through hardware testing and characterization.

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ACKNOWLEDGMENTS

Dr. Taufik,

It has been a pleasure to learn from you about the field of power electronics, and I surely would not be as heavily involved in this field without your encouragement and shared knowledge. Thank you for all your time and effort you have fed into my education.

Jonathan Paolucci,

You will always be an inspiration to me, and this thesis would doubtlessly be different and less exciting without your influence and advice. No words can express my appreciation for your friendship and support. The results of this thesis are shared between us.

My Parents,

Your support over the years has allowed me to arrive where I am, and I would not be here without your love, support, and everything you have done for me. Thank you so much.

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CHAPTER 1: INTRODUCTION

1.1 Power Electronics

As power levels rise, system sizes fall, and efficiency demands increase, power conversion necessitates advancements beyond conventional means. The field of power electronics refers to advanced conversion of energy through the use of solid-state switches. Conventionally, power conversion requires large components that provide relatively poor efficiency. Power electronics aims to minimize the size and maximize the efficiency through the use of solid-state switches and generally, high-frequency operation.

Though advanced topologies provide many advantages, the control of the system becomes more complicated. Most power electronics systems are controlled by an analog system with feedback, providing the required output. Recently, digital controls have trickled into power electronics for more advanced control or monitoring, though many digital systems still have significant limitations over analog systems [1-4].

1.2 Magnetics Miniaturization

Magnetic components are often the largest electrical component in an electrical system. Power transfer ability of magnetics is significantly affected by frequency; lower frequency requires larger magnetics for an equal power transfer. The AC system of power generation, distribution, and transmission was chosen to facilitate easily increasing or decreasing voltages for transmission.

Some countries such as the USA use a 60Hz system, while others run a 50Hz system. Either system have advantages and disadvantages, but they both require large transformers (with large magnetizing inductances) to convert power.

One major contribution of power electronics is that it allows increased frequency input into a transformer. Commonly, a transformer designed for power electronics may be run in the 20kHz-2MHz range. This further implies transformers or inductors that are a fraction of the size of a 60Hz transformer. With the largest components' size significantly reduced, the whole system can be miniaturized. Designing a quality power electronics system to operate at high frequency requires tedious attention to details and hours of design work associated with both the magnetic components and the surrounding circuitry. As seen in Figure 1-1, the high-frequency transformer is smaller, and has a power density of about 15W/cm³, while the 60Hz transformer's power density is a measly 0.15W/cm³ [5].



Figure 1-1: Transformer Size Comparison, Left: High-frequency, Right: 60Hz

1.3 Hard Switching

Hard switching is the practice of either turning on a solid-state switch with the full voltage across it, or turning it off with the voltage returning to the full voltage immediately. This is the most common way, and easiest to understand and control, of operating a switch. It is just like turning a switch on and off on a flashlight. Unfortunately, it has some serious disadvantages explained below.

Power loss due to hard-switching (switching loss) is often a major source of loss. Considering a MOSFET, the inherent device characteristics cause loss at switching. During turn-on, the current increases to its max value before the voltage decreases, and during turn-off, the voltage increases to its final value before the current decreases. Figure 1-2 shows an example of a switching transitions and power dissipation in a MOSFET. Though the switching loss appears very high, it is only for a fraction of a second which makes the average loss practical to dissipate.



Figure 1-2: I-V crossover and power loss in a MOSFET Let us assume we are using a MOSFET (metal-oxide semiconductor field effect transistor) rated for 14A 500V with an output capacitance (Drain-Source) of

300pF, such as the IRFP450. Imagine we are operating at 400V drain voltage when the gate is off, and 0V when the gate is on. The output capacitance must be discharged and charged every cycle. Picking a moderate frequency of 100kHz, the equation for power loss from capacitance is:

$$P = \frac{1}{2} \cdot C \cdot V^2 \cdot f = \frac{1}{2} \cdot 300 p F \cdot 400 V^2 \cdot 100 k Hz = 2.4W$$
(1-1)

Where P is power dissipated, C is capacitance, and V is volts, thus 2.4 watts are dissipated simply from hard-switching the output capacitance, neglecting all other losses such as the I-V crossover discussed above.

Consider switching an IGBT (insulated gate bipolar transistor), which is basically a very large BJT (bipolar junction transistor) that is voltage controlled like a MOSFET, rather than current controlled like a BJT. During turn-off, there is a phenomenon called "tail current," a result of the device being a minority carrier device. Though the gate is turned off, a smaller current still flows for some defined period, which is hole recombination within the device [6]. During this time the voltage has already returned to its initial state, so there is significant loss, since power dissipated is that tail current times the full voltage. IGBTs in hard switching applications usually operate below 50kHz due to this limitation. Figure 1-3 shows tail current in a commercial IGBT.



Figure 1-3: IGBT Tail Current During Turn-off [6]

Another issue related to hard switching deals with regulations around the world to limit the amount of electrical noise which can be emitted from a device. The noise is called EMI (Electromagnetic Interference), and can be conducted through wires, or radiated through the air. A major source of EMI is hard switching because large amounts of EMI are created from any large change in current over a short time (high di/dt). Hard switching applications distinctively chop the current, thus creating a plethora of noise that must be dealt with to meet standards.

Yet another concern that may be raised from hard switching relates to transformers. If isolation is required, a transformer must be used. When hard switching a transformer, a stray component in all transformers called leakage inductance becomes a problem. This is the inductance of the primary winding that is not coupled to the secondary winding, thus appearing as an inductance in series with the primary winding. When current through leakage inductance is

interrupted, "peaking" or "voltage spikes" appears on many topologies at the drains of the MOSFETs connected to the transformer. To alleviate this issue a snubber circuit is often used at the cost of wasting the extra energy in the leakage inductance.

In Figure 1-4, a push-pull converter is shown to demonstrate. The leakage is modeled as discrete inductors, and a common configuration for an RCD snubber is shown.



Figure 1-4: Push-Pull Converter

When one switch (MOSFET) is on, current ramps up through that leg of the transformer and leakage inductance. When the switch turns off, there remains energy in the leakage inductance, namely:

$$\mathbf{E} = \frac{1}{2} \cdot \mathbf{L} \cdot \mathbf{I}^2 \tag{1-2}$$

where E is energy (J), L is leakage inductance, and I is current at turn-off. Assuming there is no snubber, the energy in the leakage inductance transfers to the inherent drain-source capacitance of the MOSFET, similar to a series resonant circuit, and a voltage peak occurs. Since the voltage peak is often not added to the normal stress of the switch in design, it could therefore easily break the device. Thus, the RCD snubber is used to dissipate the energy. The main disadvantage is just that – it dissipates the energy rather than recycling it. Thus power loss increases with frequency, and can be roughly calculated for a welldesigned snubber as:

$$P = \frac{1}{2} \cdot L \cdot I^2 \cdot f \tag{1-3}$$

Where P is power (W), L is leakage inductance, I is current at turn-off, and f is frequency (Hz).

1.4 Soft Switching

As opposed to hard switching, soft switching is the practice of turning on and turning off a solid-state switch with either zero voltage across it or zero current through it. The converter topologies that create this are more complicated, and the control is often more difficult. Despite the complications, these converters are used in high-efficiency designs since they drastically reduce switching losses associated with hard-switching [7].

One type of soft-switching is called Zero Voltage Switching (ZVS) which refers to turning on and off the switch while there is very little voltage across it, meaning a very small voltage relative to hard switching. This is almost always achieved by some sort of resonance inherent in the topology. If no voltage is across the switch, regardless of current flow, there can be no power dissipation at the switching time. MOSFETs benefit from this greatly since the current rise and fall is so fast. IGBTs, on the other hand, do benefit, though not as much. The tail currents discussed previously still persist, allowing a small current flow as the voltage on the switch raises. Depending on the ZVS topology, IGBT switching loss must still be considered, and will be greatly affected by tail current length, switching frequency, and mode of ZVS operation.

Soft-switching topologies inherently generate less EMI than comparable hard-switching topologies. The voltages on the switch nodes change much slower, preventing any leakage spikes or ringing that are indicative of a highfrequency current sloshing among capacitances and inductances, assuredly creating unwanted EMI. Conducted EMI (through the wires back to the power source) is also strongly regulated, and filtering on the input often consumes a significant portion of board space. Reducing the EMI from switching allows reduction of the size of these components.

Yet another benefit of soft switching relates to rectifier recovery. All minority carrier diodes (most diodes, except low-voltage schottky and expensive silicon carbide) have a reverse recovery time associated with their turn-off. This is a time after the voltage has reversed across the diode (i.e. it should be off) where current continues to flow until all minority carriers have recombined. Reverse recovery of some ultrafast and schottky diodes can be seen in Figure 1-5. As demonstrated, not all ultrafast diodes are the same, and the recovery time should be noted on the datasheet. Standard recovery diodes may have recovery times in the µs range, where ultrafast are in the 10's of ns.



Figure 1-5: Reverse Recovery of Ultrafast Diodes

Diodes are commonly used on the output of a power electronics converter to rectify the output voltage. Beyond conduction losses, the reverse recovery acts as another source of power loss in the diode. The amount of reverse current during recovery depends on the di/dt of the current during turn-off. The negative current slope during turn-off continues linearly as seen in the figure until the diode begins to recover. Hard-switching configurations often have the full voltage across the diode immediately, which causes losses, especially at high voltages. Reverse recovery causes significantly less loss in soft-switching configurations due to the slow-moving voltages on the switching nodes. This also creates less EMI.

1.5 High Voltage

High voltage is any voltage over 600V, as defined by the 2005 National Electrical Code (NEC) in article 490.2. Systems employing high voltages require special considerations and precautions which normally do not plague electronics. As such, high voltage systems are a specialty area where detailed design information is not freely available.

Safety in high voltage (HV) systems cannot be stressed enough! The voltages present can easily provide lethal shocks. When the equipment is energized, all high-voltage areas should be avoided, and the whole work-space should be sectioned off from people who do not understand the dangers, and have some signage indicating the danger. Even after powering down the system, all capacitors connected to high voltage are potential dangers, as they could easily remain charged. Care must be taken to discharge these capacitors safely prior to any contact with the high-voltage circuit. All wires exposed must have voltage ratings high enough to safely insulate the voltage, as standard wire voltage ratings are usually 300-600V.

High-frequency high voltage (HFHV) presents dangers of radio frequency (RF) burns. HFHV will breakdown standard insulation more easily than DC, requiring a derating of the insulation voltage specified at DC on cabling and wires. Since the human body is a capacitance (Human Body Model is 100pF, defined by ESDA), if a part of the body is exposed to a HFHV wire, even on the outside of the insulation, the capacitance of the insulation of the wire and the human body can make a capacitive voltage divider with voltages high enough to

pass current through the body, even through an arc. These currents are at such a high frequency that the nerves do not respond to the electricity such as the pain and contractions that happen with DC, so the burn may not be noticed initially. At the entrance point on the body the thermal heating from the electricity breaking down the air and the skin at that point and will cause small point-like surface burns, which can become serious if the burn is high-energy or continues for a lengthy time. RF burns are simply another danger of high-voltage systems, and another reason to stay away from any part of the high-voltage system that is energized.

Breakdown or corona in a high voltage system indicates a problem in any well-designed high voltage system (except a few rare cases such as Marx generators). Breakdown references the failure of insulation that creates an electrically conductive path where it should not exist. The most commonplace breakdown is that of air in a thunderstorm, when the voltage in the clouds becomes enough to breakdown the air. Breakdown in air is dependent on many factors such as pressure, humidity, and temperature. Table 1-1 shows distances in air where breakdown occurs.

Vpeak		diameter [cm]				Vpeak	diameter [cm]		
[kV]	Needle	2.5	5	10	25	[kV]	50	75	100
5	0.42	0.13	0.15	0.15	0.16	140	5.15		
10	0.85	0.27	0.29	0.3	0.32	160	5.95		
15	1.3	0.42	0.44	0.46	0.48	200	7.6	7.5	7.5
20	1.75	0.58	0.6	0.62	0.64	240	9.2	9.1	
25	2.2	0.76	0.77	0.78	0.81	250			9.55
30	2.69	0.95	0.94	0.95	0.98	260	10	9.95	
35	2.69	1.17	1.12	1.12	1.15	300	11.8	11.6	11.5
40	3.81	1.41	1.3	1.29	1.32	340	13.7	13.2	
45	4.49	1.68	1.5	1.47	1.49	350			13.5
50	5.2	2	1.71	1.65	1.66	360	14.7	14.1	
60	6.81	2.82	2.17	2.02	2.02	400	16.8	15.9	15.5
70	8.8	4.05	2.68	2.42	2.37	440	19.2	17.9	
80	11.1		3.26	2.84	2.74	450			17.7
90	13.3		3.94	3.28	3.11	460	20.6	18.9	
100	15.5		4.77	3.75	3.49	500	23.6	20.9	19.9
110	17.7		5.79	4.25	3.88	450	26.8	23.1	
120	19.8		7.07	4.78	4.28	550			22.2
130	22			5.35	4.69	560	28.5	24.2	
140	24.1			5.97	5.1	600	33	26.7	24.7
150	26.1			6.64	5.52	640		29.3	
160	28.1			7.37	5.95	650			29.3
170	30.1			8.16	6.39	660		30.5	
180	32			9.03	6.84	700		33.4	30
190	33.9			10	7.3	740		36.8	
200	35.7			11.1	7.76	750			32.8
210	37.6			12.3	8.24	760		38.5	
220	39.5			13.7	8.73	800		42.2	36
230	41.4			15.3	9.24	840		46.5	
240	43.4				9.76	850			39.3
250	45.2				10.3	860		49	
300	54.7				13.3	900		53.7	43

Table 1-1: Standard Breakdown Distances in Air [8] [9]

Non-uniformity of an electric field causes breakdown to occur with lower voltages, which is why as the sphere diameter becomes smaller (or a needle point), which causes a more non-uniform field, the breakdown distance increases [10]. This complete breakdown is similar to an avalanche breakdown in a silicon device, where the entire channel breaks down at once. Breakdown also can occur in solid insulation if the dielectric breakdown strength is exceeded. Common high-voltage insulating materials have breakdowns ranging from 500V/mil to as high as 7000V/mil (1 mil = 0.001").

Corona is a phenomenon seen only where high voltage is present. It is a derivative of breakdown, but appears as a bluish glow near a conductor with a slight hissing sound, often directional, but does not travel all the way from one conductor to another. In a non-uniform electrical field (as caused by any two metal surfaces which are not large spheres), it is possible to breakdown the air where the highest electrical field exists (such as near a metal point), yet as the breakdown attempts to continue to the other conductor, the field strength decreases significantly enough to fail to breakdown the air [10]. Thus the breakdown ceases, and the corona is seen only near the conductor. Contrarily, in a uniform field, the onset of ionization leads to complete breakdown. Corona is destructive because it creates ozone, which is effective at breaking down many insulators over long periods of time, causing delayed failure. Corona, however, is a handy indication of a high-stress point accompanied by a hissing sound indicating that something is ready to completely breakdown at higher voltages,

and by turning off the lights, you'll know where to adjust the wiring or apply highbreakdown strength Corona Dope.

Breakdown and corona clarify the need for adequate insulation in a highvoltage system. Insulation methods vary, but the most common are either air or oil. Power transmission systems use air insulation in overhead lines, hence the larger distance in higher-tension lines. Switch gear such as circuit breakers or transformers for power systems utilizes air, special gasses (such as SF₆), or oil. Air insulation simply uses large amounts of air between conductors to prevent breakdown and corona by having a low electric field. This is a maintenance-free method, but requires large spaces. Gasses, or a vacuum, require air-tight enclosures for the high voltage equipment, plus the gas and equipment to evacuate and fill the chamber. This makes any necessary circuit changes very difficult to make after implementing the insulation.

Oil insulation is the most common among high-voltage equipment because it is fairly cheap, has a high dielectric strength (~700V/mil, or 28kV/mm vs 3kV/mm in air), readily displaces air, and acts as a good heat exchanger compared to air. It is, however, susceptible to contaminates and moisture lowering the breakdown, so is usually used in a sealed container. Also, the relative permittivity of oil is generally 2.2, thus all stray capacitances in an oilfilled device increases by that factor [10]. Circuitry changes can be made, though it is more difficult since it must be removed from the oil. The oil is a mineral oil designed for high-voltage insulation, such as Shell Diala AX (often called transformer oil), and is purified of contaminants, has a low viscosity, and is

characterized by the data sheet. Most oils have an additive which is an oxidation inhibitor. Some oils even have a negative off-gassing tendency, which is excellent considering gasses in the oil (bubbles) can be a cause of breakdown if they occur in high electric fields.

Some systems may have special needs of extremely close spacing and high voltages in either air or oil. In such cases, special materials may be used, such as high voltage potting compound, high voltage putty, corona dope, or Kapton tape. These materials have very high dielectric strengths, and certain mechanical properties as well, which may be suited to the particular application.

Measuring multiple kV is not a menial task, since most lab test equipment is designed to measure lower voltages. Hooking a multimeter straight to a highvoltage line will doubtlessly result in some nice arcing sounds followed by a bit of smoke and a blank readout. Specialized equipment is designed to measure high voltages or interface with existing multimeters or oscilloscopes. As with all specialized equipment, price becomes prohibitively high as the requirements deviate from the standard 300V or 1000V max. Some high-voltage probes are designed for DC - 60Hz operation, such as the Fluke 80K-40 High Voltage Probe, as can be seen by the bandwidth shown in Figure 1-6.



Figure 1-6: Fluke 80K-40 Probe Bandwidth

This probe is great for DC measurements, but high-frequency measurements require a probe with MHz or at least kHz of bandwidth.

One alternative to measuring DC – MHz range, since this task becomes surprisingly tricky with stray capacitances, is to have an AC voltage measurement device. This can be achieved through a capacitive voltage divider, and can have great high-frequency bandwidth with a simpler construction. Common to all measurement techniques, loading becomes a significant problem with high-frequency high voltage if the voltage swing is very large. Assuming the capacitive voltage divider only adds 3pF on the node being investigated, which contains a 50kHz signal, with 20kVpp, a reactive current of 7mA flows through the probe itself, which is 47 VA! Most systems would be affected by this additional load, and may even cause system failure simply by adding the 3pF probe. As probe capacitance is decreased, susceptibility to noise significantly increases due to the high impedance. High voltage high frequency measurement is difficult and thus direct measurement is often avoided.

Alternative measurement methods include "sniffing" the voltage by bringing a scope probe tip near (but not too near) a HVHF wire or node, and viewing the scope waveform. Absolute voltages will not be correct, but the waveform will be representative of the voltage waveform on the wire or node. If peak voltage is desired, a rectifier of appropriate voltage can rectify the voltage into a series RC node and be measured as DC there, or if average is desired simply a series RC can be attached and measured (considering loading, of course). The resistors, though, must have voltage ratings appropriate to the voltages or else they could change resistance or breakdown internally. For measuring high DC voltages, strands of high voltage resistors can be attached to a multimeter (on the ground side) to measure current through the strand. Though power will be dissipated, most multimeters can accurately measure in the uA or nA range, allowing relatively little power loss.

Due to its danger and cost, high voltage is usually limited to industrial uses, though a few consumer uses have become common such as in TVs and ignition systems. Here, some industrial uses and requirements will be discussed.

X-ray systems require high voltages. X-rays are generated from a vacuum tube that generally requires voltages ranging from 20kV to 150kV, depending on the tube and necessary energy ranges [11]. Medical uses of x-rays were discovered in 1895 and have since been the most common way of imaging a body's bone structure [12]. As advancements have been made, requirements for

the high voltage have become more demanding. The most important factors for the power supply are the need for a fast rise time (preferably <0.5ms), and low voltage ripple (<3%) [13]. Large ripple and/or slow rise time produce lower resolution or grainy images. Since an X-ray is a still image, power supply on time is very short. Medical CT scanners, from a power supply perspective, are basically long-duration X-ray machines, still requiring low ripple, but able to run for relatively lengthy times (several minutes). Power ranges on X-ray equipment are from hundreds of watts up to 180kW [14].

Another use of high voltage is in pasteurization. This is a process, which has been around for many decades, used to slow the growth of bacteria in food, though recently high voltage has been used to this effect on liquids. The process is called PEF (Pulsed Electric Field), and has been shown to be effective in some pasteurizations while changing the taste less than conventional methods [15]. Commercial systems generally run at 20-80kV, with 10s of amps, and pulsed with a duration from single to hundreds of µs at variable frequency depending on liquid flow. Waveforms can be square waves, exponentially decaying, or oscillatory.

The most stereotypical application of high voltage is that of scientific experimentation. Our most notable historical example is Nikola Tesla himself, master of obscure inventions. His most science-fiction invention is the Tesla coil, producing millions of volts. Nonetheless, present-day scientific experimentation often requires high voltages, such as in particle accelerators and pulse discharge

systems. Requirements here are application-specific, but voltages up to the MV are sometimes utilized.

1.6 High Voltage Transformers

Transformers are essential to power conversion, and high voltage transformers are a specialty subset of all transformers, requiring unique design practices. The nature of high voltage in these transformers requires special isolation, insulation, and winding techniques, and thus information is fairly inaccessible to all aside from the companies who hold their trade secrets. It would not be far from the truth to say that "those who speak don't know, and those who know don't speak." [16]

Most transformers are designed with some amount of isolation from the primary to the secondary windings. Certain regulations determine the test procedures and requirements, but typically isolation of a few thousand volts is common. In high voltage applications, isolation may still be required, but in this case it includes the high voltage output, thus isolation must be more carefully considered. To aid in isolation, many HV transformers utilize a U-core construction, with the primary on one leg, and the secondary on the other. Though this significantly eases isolation and winding, it yields high leakage inductance.

A major challenge in HVHF (High Voltage High Frequency) transformers is insulating thousands of volts from each other within extremely close proximity. The wires may be enamel coated, but their breakdown strength usually ranges

around 200V. The foremost failure mechanism for high voltage transformers is breakdown of the insulation and internal arcing, which is usually caused slowly by corona within the high voltage winding, eating away at the insulation until complete breakdown occurs.

Virtually all high voltage transformers have some sort of material in the secondary to replace the air, since corona occurs in air. The most common is potting compound or transformer oil. When impregnating the transformer with such, it is necessary that the liquid fills *all* gaps and spaces in the secondary side, since one small void can cause complete failure. This prevents the use of liquid-impermeable materials in areas of high voltage. Since the secondary will doubtlessly be multiple layers stacked upon each other, with high potentials between them, using conventional mylar transformer tape or Kapton tape is tempting, but may not be used in between layers because it would trap and seal air in the transformer secondary. Paper is the common alternative. Though its breakdown voltage is not high, the insulation is created by added oil or potting, and relying on its breakdown strength (though lower than tape). Thus, the paper thickness and/or number of layers of paper must allow enough oil or potting to insulate from one layer to another. To complicate things, paper has voids and capillaries which love to trap air, or moisture, even if submerged in oil or potting [17]. The electric field will mercilessly create corona in these microscopic air pockets until, once again, failure occurs.

The solution to this problem lies in pulling a strong vacuum for some time prior to encapsulating the transformer. Thus, the transformer must be prepared,

placed into a vacuum chamber with, but aside from, the encapsulation material, a vacuum pulled for generally 10 – 60 min (depending on paper thickness and pump speed), and then encapsulated in the vacuum. The vacuum draws out all the air from the chamber and paper, and it removes moisture from the oil and the transformer (which would reduce breakdown strength) since water boils below room temperature under a strong enough vacuum. Once the transformer is in the encapsulation material, a quick release of the vacuum helps force oil or potting into the capillaries of the paper [18]. This is the general method of providing adequate long-term insulation for a high voltage transformer. Unlike potting, oil has the desirable property of being self-healing. If a small void does exist, or a conductive particle, the transformer secondary may internally arc at that point. In potting, this would lead to a full and permanent breakdown channel. In oil, the breakdown basically vaporizes the impurity, and oil rushes in, providing its dielectric strength and quenching the arc.

A few pF here or there is no bother to a 60Hz HV transformer, but to a 50kHz HV transformer, stray capacitances can cause real issues with selfresonance frequencies (SRF) and circulating currents, similar to the high voltage measurement probe discussed earlier [19]. Since two conductors near each other create a capacitance, there is no way to remove the capacitance from the windings, but a few techniques can minimize the capacitance [20]. Most of the distributed capacitance, as it is called when it is capacitance within one winding, comes from the overlay of one layer of windings on top of the other due to the large voltage differential and close spacing.

The main technique used to reduce distributed capacitance is called sectionalizing the windings. This consists of breaking the secondary into multiple sections of layers, as shown in Figure 1-7.



Figure 1-7: Example of a Sectionalized Transformer and Bobbin The layers are still connected in series, and each section is connected in series. The reduction in capacitance is dependent on the number of sections, and the equation to calculate capacitance is:

$$C_{\rm S} = C_{\rm Orig} \cdot \frac{1}{n^2}$$
(1-4)

Where n is the number of sections, C_s is the distributed secondary capacitance, and C_{Orig} is what the secondary distributed capacitance would be if there were only one section (no sectionalization).

Another notable technique is to start each layer on the same side (which requires a crossover on each layer, called a flyback winding configuration) rather than winding back and forth. This reduces the capacitance by 25% [19]. Though this reduction is small, given the sensitivity to capacitance, it may be worthwhile.

Capacitance can be adversely affected by the dielectric between the windings. Since potting or oil is usually used as an insulator, the dielectric

constant must be considered. Air is 1.0, oil is generally 2.2, and potting can range from about 2 to 8 [10]. Since capacitance (as measured in free air) is multiplied by this constant, the increase after encapsulating the transformer must be designed for accordingly.

Calculating distributed capacitance of the secondary can be very difficult to obtain accurate results. Many different models can be used to model the layers, and even the offset of one layer to another becomes important. Though FEA (Finite Element Analysis) can determine the capacitance within an order of magnitude, errors can easily range from 10% to 500% (about as accurate as an experienced engineer's guess), proving difficult to fully design without building the transformer [19].

Another issue related to transformer design is leakage inductance. This is the inductance which is not coupled from one winding to the other, usually thought of as the primary to the secondary. High leakage is generally thought of as a negative property since it often impedes efficient power transfer, but can be utilized advantageously in some converter topologies. The coupling coefficient is the measure used in a transformer to explain the amount of leakage, and is defined as:

$$k = \sqrt{1 - \frac{L_{lk}}{L_{pri}}}$$
(1-5)

where k is the coupling coefficient, L_{lk} is the leakage inductance (measured by shorting the secondary winding and measuring the inductance of the primary), and L_{pri} is the primary inductance. Compact designs with closely-wound windings

generally have high coupling coefficients (indicating low leakage), while many layers of windings, especially if they do not cover the entire bobbin (such as sectionalized windings), increase the leakage. Thus, high voltage transformers tend to have higher leakage inductances, and lower coupling coefficients, than transformers with fewer windings [14].
CHAPTER 2: RESONANT CONVERTERS

2.1 Efficiency

Resonant converters are the class of power converters which use some sort of L-C resonance to achieve soft-switching. These converters tend to be more complicated, have additional components, and be more difficult to control. That being said, their power loss can be fractions of the loss of a comparable hard-switching topology. The main advantage of resonant converters is the high efficiency, though reduced EMI may be another significant benefit.

Efficiency is extremely important to advancing power electronics. Miniaturization, or increasing the power density, is important, but extraction of heat from the converter can become a difficult issue to deal with at smaller sizes. Lowering the power loss, thus increasing efficiency, enables higher power densities without extensive heat extraction systems.

2.2 Current-fed Push-Pull Converter

Push-pull converters are a fairly common hard-switching topology. Generally, they require an output inductor similar to a buck converter. As output voltages increase, an acceptable output inductor becomes more complicated and costly due to an increase in the required inductance and voltage standoff capability. A derivative of the push-pull, the current-fed push-pull, has essentially translated the output inductor to the primary side, as shown in Figure 2-1.



Figure 2-1: Current-fed Push-pull Converter

Adding the inductor to the primary side alters the control a bit. In a conventional push-pull, the switches operate 180° out of phase at variable duty cycle (though less than 50%) to regulate the output. In the current-fed push-pull, the two switches, SW1 and SW2, operate at 50% duty cycle each out of phase, so that one of the two switches is on at all times. The output regulation comes from varying the duty cycle of SW3, which is essentially a buck converter configuration without the output capacitor. The transformer steps up or down appropriately for the output voltage, and a control loop regulates the duty cycle of SW3 to maintain the output. Using this configuration, power must be transferred through two switches, creating more conduction losses. More importantly, there are three switches involved in hard-switching, creating considerable switching losses. Transformer leakage affects SW1 and SW2 regarding switching losses as discussed in chapter 1. Despite disadvantages related to power loss, this topology has been widely used reliably.

2.3 L-C Oscillation

To understand resonant converters and soft-switching, the L-C oscillation must be understood. The two main types of L-C oscillators consist of components in series or components in parallel, though there are many variations on these.

The series L-C oscillation circuit and waveforms are shown in Figure 2-2, associated with the circuit in Figure 2-3. Vin is a square wave, and the oscillation occurs between the inductor and capacitor, and is damped by the resistor.



Figure 2-2: Series RLC Response



Figure 2-3: Series RLC Circuit

Noting the input (Vin) and output (V_osc), the output has a superimposed decaying sine wave added to the input waveform. Its angular frequency is:

$$\omega = \frac{1}{\sqrt{L \cdot C}}$$
(2-1)

where ω is the angular frequency, L is the inductance, and C is the capacitance. Thus its real frequency is:

$$f = \frac{\omega}{2 \cdot \pi} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}}$$
(2-2)

where f is the frequency in Hz. Noting the output, the voltage of the sine wave yields a higher voltage than the input waveform. This voltage is directly proportional to the frequency and current in the circuit, since:

$$I_{\rm C} = C \cdot \frac{dv_{\rm c}}{dt}$$
(2-3)

and

$$V_{\rm L} = L \cdot \frac{di_{\rm L}}{dt}$$
(2-4)

where I_C is capacitor current, C is capacitance, dv_C/dt is the rate of change of voltage (V/s) across the capacitor, V_L is the inductor voltage, L is the inductance, and di_L/dt is the rate of change of the current (A/s) through the inductor.

In layman's terms, the resonant circuit, or "tank" can be thought of as "sloshing" energy around, between the L and C. The energy is stored as a current in the inductor, and stored as a voltage in the capacitor. When resonating, the full energy is in the inductor when the capacitor is completely discharged (V_c=0V), and the full energy is in the capacitor when the inductor is completely discharged (I_L =0A). The component energy equations are:

$$E_{L} = \frac{1}{2} \cdot L \cdot \left(I_{L}\right)^{2}$$
(2-5)

$$E_{\rm C} = \frac{1}{2} \cdot C \cdot \left(V_{\rm C} \right)^2 \tag{2-6}$$

where energy E is in joules. These components continue trading the energy back and forth at the resonant frequency until the energy is completely consumed by the circuit losses (called damping).

The series resistance damps the oscillation, creating the exponential decay. This component is not necessarily a discrete component. Since all nonideal components have some series resistance, this must be modeled in simulation. The resistance is a combination of the capacitor's ESR (equivalent series resistance) at the particular frequency, and the inductor's ESR, which potentially consists of DC winding resistance and AC losses (such as eddy currents, skin effect, and proximity losses). It is impossible to have no resistance in a real L-C circuit. Lower resistance is regarded as a higher quality circuit. Thus, the "quality factor" was created to explain how lossy the resonant circuit is. Q is defined as the ratio of power stored to power dissipated, and can be expressed as:

$$Q = \frac{X}{R}$$
(2-7)

where Q is the quality factor (unitless), X is the reactance of the capacitor or inductor at resonance, and R is the resistance. The equation is identical for

series or parallel resonant circuits, as long as the resistance in the parallel circuit is directly in series with the inductor or capacitor.

Parallel resonance is based on the same principles of series resonance, though with a different component configuration. The inductor and capacitor are in parallel, and the parasitic resistance is effectively in series with the inductor. Just like the series resonance, the resonance occurs when the component reactances are equal. In the series case, the impedance of the circuit to an AC waveform becomes zero (if Q is infinite), but in the parallel case, the impedance of the circuit to an AC waveform becomes infinite (if Q is infinite). As such, the circuit appears as an open circuit to an AC current source at resonance.

Magnitude of the current resonating in a parallel resonance circuit can be determined by the voltage across the capacitor (and/or inductor). A basic analysis by transforming into the frequency domain follows:

$$V = I \cdot Z \tag{2-8}$$

$$Z = R + j \cdot X \tag{2-9}$$

$$X_{C} = \frac{1}{\omega \cdot C}$$
(2-10)

$$X_{C} = \frac{1}{\frac{1}{\sqrt{L \cdot C}} \cdot C}$$
(2-11)

$$X_{C} = \frac{1}{\sqrt{\frac{C}{L}}}$$
(2-12)

$$X_{C} = \sqrt{\frac{L}{C}}$$
(2-13)

Assuming resistance R is negligible,

$$V = j \cdot I \cdot \sqrt{\frac{L}{C}}$$
(2-14)

$$|\mathbf{I}| = \left| \mathbf{j} \cdot \mathbf{V} \sqrt{\frac{\mathbf{C}}{\mathbf{L}}} \right| \tag{2-15}$$

$$I = V \cdot \sqrt{\frac{C}{L}}$$
(2-16)

Thus, the magnitude of the current can be found from the voltage and the resonant components. Alternatively, if the current is known, the voltage can be determined by a simple rearrangement:

$$V = I \cdot \sqrt{\frac{L}{C}}$$
(2-17)

2.4 Capacitively-Loaded Parallel Resonant Push-Pull

As shown above, resonant currents can become quite large depending on the resonant components, even if the DC sustaining input current is reasonable. Though resonant converters benefit from the lowered switching loss, often the conduction losses are significantly higher due to having to pass a large resonant current through the switches. One topology that mitigates some of this problem is the converter proposed by Daniel Edry and Sam Ben-Yaakov of the Ben-Gurion University called the Capacitively-Loaded Push-Pull Parallel Resonant Converter (CL-PPRC) [21]. Shown in Figure 2-4, the converter is a relative to the currentfed push-pull discussed earlier.



Figure 2-4: Capacitively-Loaded Push-Pull Converter (CL-PPRC)

The resonant section of this converter relies on the resonance between the capacitor C1, and the effective parallel inductance (that of the split inductor L1 and L2 in parallel with the transformer's apparent inductance, which could be load-related). Since the input inductor is large enough to act as a current source, the resonance experienced is the current-fed parallel resonance. During resonance, this "tank circuit" experiences the high resonant currents discussed earlier. Since the converter is aimed at efficiency, the L and C components will doubtlessly have a low ESR, yielding a high Q in the resonant circuit.

Control of this circuit occurs by frequency modulation. That is, the gates each have a 50% duty cycle 180° out of phase, but the period is altered by the control scheme. The switching frequency is required to be below the resonant frequency. The converter transfer function is:

Vout = Vin
$$\pi \cdot n \cdot \left(\frac{f_r}{f_s}\right)$$
 (2-18)

Where Vout is the output voltage, Vin is the input voltage, N is the transformer turns ratio, f_r is the resonant tank frequency, and f_s is the switching frequency. Noting:

$$\frac{f_r}{f_s} > 1 \tag{2-19}$$

indicates this converter operates in a boost configuration, and output cannot be reduced below a certain point.

Figure 2-5 shows the waveforms of SW1 voltages, and the currents in L, C, and SW1. SW1 and SW2 have identical voltage and current waveforms, just 180° out of phase. The component values, which are shown in Figure 2-4, and gate timing were chosen within the suggested criteria from [21].



Figure 2-5: PPRC Operating Waveforms

Based on the drain waveform, it is clear that ZVS is achieved by this topology. However, investigating the drain current should raise some concerns. In this configuration, the output power is only around 17W, with a 24V input, yet we see drain currents in excess of 5A. In this case, drain RMS current is 2.5A, while the average is 0.4A. When the circuit is not resonating, the resonant current flows through the switches, hence the high currents. This converter is an improvement over many resonant converters, as the resonant current often flows through a switch the entire period, but the switch requirements (and thus cost) and conduction losses will still be higher due to this current. As the frequency

approaches the resonant frequency, the switch RMS current will decrease, but the converter will have less margin for control. The suggested ratio of f_s to f_r is 0.7-0.8 (as simulated) to allow sufficient room for component tolerance as well as headroom for line or load changes [21]. Inherently, this converter will have excessive drain currents since resonant currents flow through the switches.

The controllable voltage range is limited in this converter, similarly to a boost converter. It must be used in an application whose voltage need not range drastically. If the converter needs to be used over a wide range, the operational frequency range must be wide. Since resonant current flows through the switches, as the operating frequency decreases (higher output voltages), more current flows through the switches, thus creating significantly more loss. This limitation becomes prohibitive at some point, limiting the useful range. Another disadvantage is the wide frequency range required, which prevents use from systems requiring a fairly fixed operation frequency to prevent any kind of aliasing or intermodulation distortion among other signals.

During start-up, there is no easy soft-start mechanism. If the converter is operated at its maximum frequency at the resonant frequency, which yields the lowest output voltage, the overshoot could still be devastating. Figure 2-6 shows startup overshoot of the converter from Figure 2-6 run at maximum frequency, with a light load.



Figure 2-6: Startup Waveforms of CL-PPRC

Drain voltages reach double the operating voltage, and the output voltage is almost double the steady-state value. Also, the input current has a very large spike that could trip a fault from the power source supplying the PPRC. These conditions do change with output load, so with a specific load, the converter may not cause an issue, but the startup definitely requires special consideration.

This converter has no inherent short-circuit protection. If a short on the output occurred, or in a high voltage system a breakdown that acts similar to a short, the converter would self-destruct without aid from external protection circuitry. When a short is applied, all of the transformer's coupled inductance is immediately shunted. All that is left for the PPRC is the leakage inductance. In all but the rarest cases, the leakage inductance will be significantly smaller than the resonant inductor (L1 and L2). This will cause the natural resonant frequency, f_r to increase drastically since the effective resonant inductance is no longer based

on the discrete inductor, but is based on the leakage inductance. Likely, the control loop will detect the output voltage drop, and lower its frequency to the lower limit to compensate, compounding the problem. Even if the converter were operating at its maximum frequency, which was the original f_r, the resonance is now at a higher frequency, so the converter still operates in a strong boost condition, drawing more current from the input inductor. This causes extremely high resonant currents which must be conducted through the switches for the majority of the period. Stress on all components is extremely high, and failure is likely. Unless short-circuit protection is deemed unimportant, some external circuitry must be implemented to solve this problem.

Though the CL-PPRC successfully implements resonance and ZVS, it suffers from excessive resonant currents flowing through the switches. If it were run exactly at resonance, this problem would not be an issue. However, operating the converter at perfect resonance would be very difficult with the configuration of controlled gates presented in [21]. The resonant components have relatively large tolerances, not due to poor design or manufacturing, but from the inherent properties of materials involved – specifically the magnetic material such as ferrite. It is not uncommon to have a 10% or 20% tolerance over the operating range. Following a wandering resonant frequency can be achieved through conventional controls, but there is an easier way.

2.5 Self-Resonance and Royer Oscillator

Edwin Armstrong, Ralph Hartley, and Edwin Colpitts were some of the early inventors of self-resonating circuits in the 1910's. These circuits were very important in wireless transmissions of the time, hence the three circuits named after them. All these circuits required a positive feedback method with a gain above one in order to sustain oscillation. Their original circuits, of course, used tubes, as the transistor was discovered in 1947. Jumping ahead to the 1950's, George Royer described the Royer oscillator, which is a self-resonating circuit that is still often used today, commonly as a CCFL (cold-cathode florescent lamp) driver for portable electronics LCD backlights. The basic Royer Oscillator is depicted in Figure 2-7.



Figure 2-7: Royer Oscillator

Similarly to the PPRC, the Royer Oscillator uses an L-C resonant tank. In this case, the L is the inductance of the transformer, and C is a discrete capacitor on the collectors of the NPN transistors. The excellent design in this circuit is because of the third winding on the primary side of the transformer which is

connected to the bases of the transistors. This winding ensures when one transistor is on, the other transistor is off, and as the sinusoidal resonance passes through the zero crossing, the active transistor is turned off and the other turned on. Due to the third winding coupled directly to the resonant tank, this topology absolutely tracks the resonant frequency even across wide component ranges and tolerances. Due to its zero-voltage switching, it is also an efficient circuit.

Another self-oscillating design is the cross-coupled L-C MOS oscillator depicted in Figure 2-8, based on MOSFETs rather than BJTs. The cross-coupling of the gates to the opposite drains yields a negative impedance at the drains.



Figure 2-8: Cross-coupled LC MOS Oscillator

Q of the circuit is defined as:

$$Q = \frac{2 \cdot \pi \cdot f \cdot L}{R_L}$$

(2-20)

And g_m is:

$$g_{m} = \frac{I_{D}}{V_{GS} - V_{t}}$$
(2-21)

For a stable oscillation,

$$\frac{1}{g_{m}} \ge \frac{2 \cdot \pi \cdot f \cdot L}{Q}$$
(2-22)

Where R_L is the series resistance of the inductor, g_m is the gain, I_D is the drain current, V_{GS} is the gate-source voltage, and V_t is the MOSFET threshold voltage. Increasing the drain current increases the gain which helps start-up and keeps a more stable oscillation [22]. Just like the Royer Oscillator, this topology directly follows the resonant frequency of the circuit regardless of any component variations.

2.6 Mazzilli Converter

The Mazzilli converter was ideated by Vladimiro Mazzilli, and is a derivative of the L-C MOS oscillator and Royer Oscillator [23]. As such, it self-oscillates at the L-C oscillation frequency. Figure 2-9 shows the basic schematic of the converter.



Figure 2-9: Mazzilli Converter Topology

The main difference in this converter comes in the gate drive circuitry. The Royer Oscillator requires a resistor from Vin, and a tertiary primary winding to drive the switching transistors, and the L-C MOS oscillator uses the opposing drains. One severe limitation of the L-C MOS cross-coupling is the fact that few MOSFET gate voltages can withstand above 20V, severely limiting the input voltage. The Mazzilli uses a combination, pulling power from Vin, yet cross-coupling the gates through a diode to the opposing drain. This overcomes the voltage limitations of the L-C MOSFETs instead of the Royer's BJTs, since MOSFETs are generally faster in full switching conditions. Also of note is the input inductor L1. Some Royer Oscillators also use this component. It increases efficiency by acting as a current source (the inductance is at least 4 times the magnetizing inductance of the transformer).

2.6.1 Modes of Operation

This converter has four modes of operation. The first mode is as the drains of both SW1 and SW2 approach zero, shown in Figure 2-10. The cross-coupling nature assures that SW2 turns on as SW1 turns off.



Figure 2-10: Mazzilli Operation Mode 1

During this operation, the resonant capacitor is completely discharged. The entirety of the resonant energy is stored in the inductor current, which is at a peak. No voltage is across the inductor/transformer, thus there is no output voltage or power transfer. Since the switch oscillation follows the L-C oscillation, no resonant current will flow through the switches.

After SW1 turns off and SW2 on, the resonant current proceeds to resonate, seen as a rise and fall of Drain1 voltage, transferring energy from the inductor to capacitor and back to inductor. This is mode 2.



Figure 2-11: Mazzilli Operation Mode 2

During this time, the transformer, which is also the resonant inductor, transfers power to the load. The load is reflected to the primary as shown in Figure 2-12. Note the leakage inductances from the transformer are shown discretely.



Figure 2-12: Mazzilli Operation Mode 2 Equivalent

Examining the effective circuit, it is clear the effective resonant inductance could be changed by the load resistance, since the magnetizing inductance could be shunted by the load resistor. This will be explored later.

As the Drain1 voltage resonates back down to zero, SW1 turns on and SW2 turns off, moving into the third operating mode of Figure 2-13.



Figure 2-13: Mazzilli Operation Mode 3

Just like the first operating mode, the capacitor is completely discharged, and the resonant inductor carries the full current, though in the opposite direction.

The final operating mode is as Drain2 exhibits the resonant rise and fall, similarly to mode 2.



Figure 2-14: Mazzilli Operation Mode 4

Power is transferred to the load again, though the polarity of the output voltage has reversed, similar to a push-pull. At the completion of mode 4, mode 1 once again occurs. Note the voltage across the inductor/transformer naturally

averages to zero. This inherently avoids a problem in push-pull converters called flux imbalance where the transformer is driven slightly into saturation due to a non-zero average voltage.

Voltage on the switching nodes is significantly higher than the input voltage. The voltage can be found based on the fact that the input inductor's average voltage is zero. On the inductor, one node is Vin, and the other is split between the drains, yielding a waveform similar to a full-wave rectification, though at half the voltage of each drain. Thus, we can derive the drain voltages as such:

$$V_{ind} = \frac{2}{T} \cdot \int_{0}^{\frac{T}{2}} \frac{V_{pk} \cdot \sin\left(\frac{2 \cdot \pi}{T}\right)}{2} dt = \frac{V_{pk}}{\pi} = V_{in}$$
(2-23)

$$V_{pk} = \pi \cdot V_{in} \tag{2-24}$$

where V_{ind} is the inductor voltage, T is the period, and V_{pk} is the peak drain voltage. Equation 2-24 presents an easy calculation of the drain voltage at steady-state. Input transients and load transients require further considerations.

2.6.2 Drawbacks and Limitations

This converter has the distinct advantage of locking the resonant currents within the resonant tank due to its self-tracking nature. Component tolerances and variations during operation do not cause any problems regarding the control since it self-oscillates. Despite these advantages, some serious conditions occur that present some possibly detrimental disadvantages.

During power transfer, the load is reflected across the transformer and appears in parallel with the transformer primary magnetizing inductance. As load changes, the impedance of the primary winding can be affected (worst case short circuit, shunting the entire magnetizing inductance). Since we know the resonant frequency, and thus operating frequency, is dependent on the primary's inductance:

$$f_{r} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}}$$
(2-25)

then it follows that if the primary's magnetizing inductance is shunted by the load, the operating frequency will be load-dependent. Within a range, this may be fine, but under heavy load, the only resonant circuit remaining may be the capacitor resonating with the leakage inductances. While this will not prevent oscillation, leakages in modern high density transformers tend to be very low (typical coupling coefficients above 0.9) [24], and thus the resonant frequency and currents could skyrocket easily an order of magnitude. This could result in significant loss and possible failure since the currents will be higher and the frequency will also be higher, potentially yielding significantly more AC losses.

Gate drive power is supplied from Vin through a resistor. Since the gate is a capacitance, this yields an R-C time constant to charge the gates. If the operating frequency is low, this is not an issue. At high frequencies, the gate drive becomes a problem, as seen in Figure 2-15. Note the gate and drain

voltages shown are for the *opposing* switches. Considering switching loss in a MOSFET when fast switching is desired, a fast gate signal is required.



Figure 2-15: Mazzilli Gate Operation

Higher voltages present another problem with the gate drive circuitry. The minor problem of overvoltaging the gates from a Vin too high can easily be mitigated by placing a zener in parallel with the gate-to-source below the gate breakdown voltage, though this will create higher losses in the gate resistors. The larger problem comes from diode device capacitance. Since the diodes are connected to the opposing drain, any diode capacitance acts to transfer current to the opposing drain during the resonant cycle. Though a few pF sounds menial, it can have serious effects on the gate voltage, shown in Figure 2-16.



Figure 2-16: HV Mazzilli Gate Operation

The falling drain voltage pulls current from the opposing gate through the diode capacitance, which can even pull the switch out of conduction. If this happens, losses could reach such high levels that the switches would be destroyed. To mitigate this problem, the gate resistors can be lowered in value, but this adds more power loss. From a high Vin, the power loss of these resistors becomes higher than any other component in the topology which is clearly unacceptable.

When the gate is low causing the switch to be off, the gate does not fall to zero volts. The voltage is the opposing drain voltage plus a diode drop. For low-voltage power MOSFETs with threshold voltages of around 5 volts, this is generally acceptable. Unfortunately, this becomes very problematic at higher currents and higher voltages, as the R_{DS_on} of high-voltage MOSFETs increases rapidly, and high currents will cause a significant voltage on the drain during the on-state. In this case, the "low" voltage on the gate may be very near, or even above, the threshold voltage. If this occurs, both MOSFETs can latch on. This is a disastrous condition, as the current in the input inductor ramps up indefinitely (since it has the full Vin across it) until some component erupts in a fury of fire and smoke. Such case is one strong limiting factor in attempting high input voltage high powers with this converter.

During resonant modes 2 and 4, the entire resonant current is flowing through the transformer primary. As such, the primary must be designed for much higher currents at high frequency than simply designing to the desired power transfer of the transformer. The transformer will, therefore, be of larger

size and likely larger leakage than other transformers with comparable power ratings.

Start-up conditions in this converter are unfavorable. The input inductor has no current flowing through it. During start-up, the input inductor adds a resonance to the system. The problem is almost identical to that of the CL-PPRC described in 2.4 and in Figure 2-6. If the output is loaded "properly," overshoot does not exist, but the converter is much more versatile if it can start up under any condition.

Load transients can also cause a latch-up condition. Since latch-up is detrimental, this condition must be avoided. A slow change in the load may change the operating frequency, but will not cause a latch-up. A latch-up condition is shown in Figure 2-17 due to a heavy load transient.



Figure 2-17: Mazzilli Load Transient Latch-up Operation

Certain design constraints can avert this problem, but come at a cost. One such modification is that the leakage inductance can be increased, but this reduces power throughput capability of the transformer. If sharp load transients or short circuits are an impossibility, this will not be an issue.

This converter's largest drawback is that it is unregulated. No control scheme to self-correct the output voltage results in output voltages being affected by any changes or glitches in the input voltage, as well as varying with a variable load. Practically all modern converters require some sort of regulation, so although this converter is a shining star regarding resonance and ZVS, its limitations severely limit its practical utility.

2.7 Resonance and High Voltage

High voltage, once again, presents some unique characteristics. Traditional hard switching using PWM (pulse-width modulation) inverters with high voltage transformers is insultingly problematic. Requirements of high turns ratios and large voltage isolations exacerbate the transformer parasitics and nonidealities, as discussed in Section 1.6. Leakage inductance causes undesirable potentially damaging voltage spikes, and the distributed capacitance slows rise times and causes current spikes. Both efficiency and performance are adversely affected, and system reliability decreases with increased component stress [25].

Rather than fighting the transformer parasitics, which are guaranteed to be high, it seems to make sense to embrace and utilize the non-idealities. Resonance can do just this. Many high voltage power supplies utilize resonance to achieve higher reliability, efficiency, and performance [26]. Leakage inductance and distributed capacitance must be considered, and both can be

used to assist the power conversion. Careful attention must be paid, however, as misuse of the parasitics can seriously degrade the converter performance or efficiency.

Inductors possess what is called a self-resonant frequency (SRF). This is the frequency of the parallel resonance of the inductance with the distributed capacitance of the inductor. Generally for standard inductors, it is well within the MHz region, and is distinctively avoided. Approaching the SRF, the impedance will be much higher than the inductor at lower frequencies, and above the SRF, the inductor will act capacitive. Transformers have a similar measure, though it is more complicated. Multiple windings cause interactions of distributed capacitances and interwinding capacitances, creating a complex interaction that is dependent on the external winding connections. The transformer will have a SRF, or possibly multiple SRF's for different windings, but similar to the parallel resonant circuit, the impedance will be higher approaching the SRF. This causes an increase in output voltage, but also induces large circulating currents within the transformer that contribute to loss through heat. Though SRF's must be carefully considered, they are difficult to determine prior to constructing and connecting the transformer. Even advanced FEA (finite element analysis) accuracy is inconsistent and can easily have errors of 500% [19].

Rectifiers have reverse recovery, discussed in section 1.4. Utilizing resonance in high voltage provides sinusoidal voltage waveforms rather than the square waveforms seen in PWM inverters. These diodes are generally the only semiconductor devices directly on the secondary of a HV system. Since high

voltage rectifiers have such a high voltage across them, any reverse current causes significant power loss, and reverse recovery losses can both degrade efficiency and lower the output voltage. Since reverse recovery time is not extremely dependent on waveform, a sinusoidal voltage across the diode causes much less loss than a square wave. In this way, utilizing resonance and softswitching boosts efficiency and performance, and significantly eases stresses on the secondary semiconductors.

2.8 Voltage Multipliers

Higher voltage specifications necessitate tougher construction requirements for HV transformers and introduce increasing parasitics. As such, it is attractive to use a lower turns ratio to ease the HV transformer, and use a voltage multiplier following the transformer to achieve the desired voltage [26].

A standard 2-stage half-wave Cockcroft-Walton (CW) cascade voltage multiplier operation will be described below, seen in Figure 2-18. All other DC voltage multiplier configurations can be understood by the same principles [26].



Figure 2-18: 2-stage Half-wave CW Voltage Multiplier

The input voltage, Vin, is some AC waveform; let's assume a sinusoidal waveform. The operational modes discount component values and focus on the concepts. Four modes occur:

- As Vin approaches its negative peak value, C1 charges through D1 to the waveform's peak value, Vin_{pk}.
- As Vin approaches its positive peak value, Vin_{pk} from Vin adds to the V_{pk} on C1, charging C2 to 2*Vin_{pk} through D2.
- Swinging to negative peak again, C3 charges through D3 to Vin_{pk}. C1 is recharged through D1 again.
- Swinging to the positive peak, C4 charges through D4 to 2*Vin_{pk}. C2 is recharged through D2 again.

Thus, after a few cycles, Vout is 2 times the input peak-peak voltage, or 4 times Vin_{pk}.

Voltage multipliers inherently have near-equivalent stresses across each stage, allowing for identical component selection and ease of analysis. They are also scalable with as many stages as desired for multiplication. This allows for a much lower input voltage than the desired output voltage. Most multipliers operate at high frequencies to allow for smaller capacitors.

The disadvantages come in ripple, regulation, and protection. The regulation and ripple can be easily determined by the equations in Table 2-1, and is highly frequency-dependent. This analysis assumes all capacitor values are equal.

	Output Voltage	Voltage Drop	Ripple
	(Vout)	(ΔV)	(δV)
Half-wave CW	$2 \cdot n \cdot V_{pk}$	$\frac{i_L}{f \cdot c} \cdot \left(\frac{2}{3} \cdot n^3 + \frac{1}{2} \cdot n^2 + \frac{1}{3} \cdot n\right)$	$\frac{{}^{i}L}{f \cdot c} \cdot \frac{n \cdot (n+1)}{2}$
Full-wave CW	$2 \cdot n \cdot V_{pk}$	$\frac{i_{L}}{f \cdot c} \cdot \left(\frac{1}{6} \cdot n^{3} + \frac{1}{4} \cdot n^{2} + \frac{1}{3} \cdot n\right)$	$\frac{{}^{i}L}{f \cdot c} \cdot \frac{n}{2}$

Table 2-1: CW Voltage Multiplier Equations [26]

Where n is the number of stages, c is the capacitance, f is the input frequency, V_{pk} is the peak input voltage, and I_L is the load current. The full-wave CW multiplier is a basic derivative of the half-wave CW, and a 2-stage version is shown in Figure 2-19.



Figure 2-19: 2-stage Full-wave CW Voltage Multiplier

The full-wave CW, also called symmetric CW, provides much lower ripple and better regulation, as described by Table 2-1, but comes at the cost of extra components. To achieve even better performance, capacitors may be chosen with unequal voltages. It has been found, though, that given a fixed total capacitance, the multiplier's output resistance will be no less than 75% the value if using all equal capacitors [27]. Considering the capacitor size differences and acquisition issues, it seems reasonable to use all equal capacitance values. The described voltage multipliers achieve a positive voltage multiplication, but a negative output voltage is just as easy to achieve. Reversing the polarity of the diodes will result in a negative output. In this way, a positive and negative voltage of equal magnitude can be derived from the same AC source.

CHAPTER 3: RESONANT SELF-TRACKING CURRENT-FED CONVERTER

3.1 Proposed Converter Topology

The proposed topology in Figure 3-1 on the next page is a high voltage high-power multi-stage converter, called a Resonant Self-Tracking Current-Fed Converter (RST-CFC). Stages consist of a pseudo-buck converter feeding a Mazzilli-based self-resonating ZVS converter, which outputs high voltage high frequency AC and is fed into positive and negative voltage multipliers that boost the output voltages. The transformer is integrated into the resonant tank circuitry, though does not carry the resonant current. A unique converter-specific gate drive architecture provides the continuing self-oscillation within the resonant section. Converter-specific protection circuitry ensures that a fault in the circuitry will shut down the converter rather than destroy any further components.



Figure 3-1: Proposed RST-CFC Converter Topology

3.2 Application Conditions

This converter topology is suited best to high-power high-voltage designs needing fair power density and relatively high efficiency. The high voltage output is split into a positive and negative in order to reduce insulation requirements between the output terminals and the load. High voltage resistors in the voltage multipliers ensure safety of the diodes in the case of a high voltage breakdown (or "sparkdown") on the output, which is a significant concern at high voltages. Inherent characteristics of the resonant circuitry protect the switching components from damage during a short circuit condition (such as a sustained sparkdown).

Though processing power through multiple stages generally reduces efficiency, high per-stage efficiency still yields a converter whose efficiency is reasonably high. Buck converters can easily achieve efficiencies in the 90% range. The self-oscillating resonant soft-switching circuitry can achieve efficiencies in the high 90%'s, as well as the voltage multiplication stage. Combined, efficiencies in the 80%'s are reasonable expectations from a welldesigned converter.

Input may be a rectified mains line. The use of IGBTs as the resonant switches allows for high input voltages such as a 480V 3Φ line, which also allows for scalability up to higher powers. The pseudo-buck input MOSFET could be substituted for an IGBT if currents or voltages deem it necessary.

The high voltage transformer is driven at high frequency by a resonant tank providing a sinusoidal drive. HVHF (High Voltage High Frequency)

transformers are plagued by high parasitics that cause problems with hard switching, so the use of the ZVS sinusoid enables looser requirements for the transformer, and thus a cheaper component.

The converter is controllable through adjustment of the pseudo-buck input stage. The entire transfer function acts similarly to a buck, so a wide output range can be reasonably achieved and controlled. High-voltage systems that require an easily and remotely controllable voltage will benefit from this feature.

Protection circuitry detects the voltages on the drains of the IGBTs to detect a fault condition. If the converter breaks out of oscillation, latches up, or draws excessive current that pulls the IGBTs out of saturation, the protection circuitry disables the gate drive circuitry on both switches. Varistors on each collector (not shown) absorb any voltage spike caused by the input inductor when the protection circuitry shuts down the switches.

3.3 Resonant Tank

The essential components of the resonant tank circuitry are isolated in Figure 3-2. Operation is almost identical to the Mazzilli operation described in detail in Section 2.6, so operating modes will not be described here. The largest difference, however, is the addition of the resonant inductor, L4.

The resonant tank consists of the capacitance C5 and the inductance L4 in parallel with T1's primary inductance. Thus, the operating frequency can be found as:

$$f_{r} = \frac{1}{2 \cdot \pi \cdot \sqrt{C \cdot L_{eq}}}$$
(3-1)

where L_{eq} is:

$$L_{eq} = \frac{L_{ind} \cdot L_{mag}}{L_{ind} + L_{mag}}$$
(3-2)

where L_{ind} is L4's inductance and L_{mag} is T1's entire primary inductance seen from the resonant tank. L_{mag} is the combination of the two coils on the HV transformer primary. Since they are magnetically coupled, adding them in series yields a four-fold increase in inductance from each individual coil. Thus, if L_{mag} is 4 times L_{ind} , the majority of the resonant inductance comes from L4, indicating the majority of the resonant current will flow through L4. If the primary inductance of each individual coil is equal to L4, the change in resonant frequency by adding the transformer to the circuit will be an increase of 11.8% to the operating frequency [23].


Figure 3-2: Resonant Tank Circuitry

As load changes the frequency is more stable than the Mazzilli design. Since the reflected load is shunt to the magnetizing inductance, and the magnetizing inductance is larger than L4, a change in the load in the normal operating range will have little effect on the frequency since L4 is the primary factor in determining frequency. This precludes complete shunt of the magnetizing inductance during a short circuit.

Without L4, latch-up during a load transient is a possibility because the resonant tank energy required to maintain oscillation flows through the transformer, and a step change in load could draw that energy through the transformer out of the resonant tank as described in section 2.6.2. L4 provides isolation of some of the resonant energy required to maintain oscillation from the

output, such that even during severe output load transients or sparkdowns, oscillation will continue correctly.

3.4 Converter-Specific Gate Drive Circuitry

Given the limitations on the Mazzilli gate drive circuitry, a new method of driving the gates had to be developed specifically for driving IGBTs with high collector voltages. The following requirements make available gate drive chips impractical for this application. The gate drive must cross-couple to the other high-voltage drain and be dv/dt resistant. It needs to have virtually no delay time. It must have a high-current drive to switch large IGBT gate charges. It must latch off for a short period during turn-off. These requirements led to the development of the gate drive circuitry found in Figure 3-3.



Figure 3-3: Gate Drive Circuitry

To maintain self-oscillation, the gates must be cross-coupled to the opposite collector to turn on and off at the appropriate commuting times. The collectors of the IGBTs are connected to the resonant tank. Gate 1 must turn on

as gate 2 turns off, which is when drain 1 resonant cycle approaches zero volts. Thus, gate 1 is on when the collector of SW2 is at a high voltage, and gate 2 is off when the collector of SW1 is at a low voltage.

When collector 2 is at high voltage, gate 1 must transition high. Collector 2 high turns off the cross-coupled diode. The current source feeding Vgi1 pulls up Vgi1, since the current sink below the level shifters sinks less current than the source provides. As Vgi1 is rising, the voltage follower sources a large current into node Vg1 to charge the gate capacitance of the IGBT. Since the voltage follower's current gain is β^2 (>10,000) due to the darlington transistor pairs, the current drawn from the Vgi1 node is negligible, thus the voltage is unaffected.

When collector 2 is a low voltage, meaning gate 2 is on, then gate 1 must transition low. The low voltage on collector 2 turns on the cross-conducting diode and pulls Vgi1 down to a diode drop above collector 2, since collector 2 is a lowimpedance node. The low Vgi1 voltage translates to a lower voltage input on the voltage follower, due to the level shifter and current sink, causing the follower to pull a large current and discharge the IGBT gate. VEE is a negative voltage, thus the gate will be pulled to a slightly negative voltage, aiding in switch turn-off.

As the gate voltage is pulled low, the gate turn-off latch circuitry activates. The gate latch-off circuitry is only necessary due to circuit parasitics, particularly inductances, that can cause ground-bounce and false-trigger the gate drive circuitry to reactivate and oscillate at very high frequencies, drawing excessive power and even possibly collapsing the resonant oscillation. While the gate of the IGBT is high, the R-C connected to the MOSFET gate is charged to a high

voltage, but the gate-source voltage remains negative or zero, ensuring the MOSFET is off. As the IGBT gate falls, the R-C begins to discharge. For a finite time (much less than the period of the resonant oscillation), the gate-source voltage (across the resistor) is above the threshold voltage and turns on the MOSFET. This, in turn, pulls node Vgi1 down through the resistor, and the gate drive circuitry is latched in a low state until the R-C on the MOSFET is discharged. In this way, positive feedback ensures once the circuitry triggers the negative transition, it remains there long enough for the opposing gate circuitry to reach a high state.

During the circuitry's entire operation, all BJT's remain off or in linear mode, ensuring the extremely fast circuit response times necessary. The resistors from base to emitter in the darlington pairs allow the second transistor to turn off faster by creating a path for base charge to be swept out of the BJT during turn-off. This is crucial, or unacceptable amounts of shoot-through would occur and the transistors would overheat. The darlington pairs ensure enough current is available to drive very large gate charges of larger IGBTs quickly. The current source provides enough current to maintain a high voltage on Vgi1 even as the parasitic capacitance in the cross-coupled diode pulls current from Vgi1 as the opposing collector voltage falls. All of these special considerations make this custom gate drive circuitry not only well suited, but essential, for this application.

3.5 Converter-Specific Protection Circuitry

The protection circuitry designed for this converter in theory should be unnecessary, similarly to a reserve parachute. In practice, the fault light is a nice reminder that the protection circuitry just prevented compounded failures and a crater in the circuit board.



Figure 3-4: Converter Protection Circuitry

Protection is implemented to protect the main IGBTs connected to the resonant tank. As switch voltages and currents increase, so do cost and size, as well as consequence in the case of a fault. To prevent switch breakage due to overcurrent, most high-power IGBTs have dedicated protection circuitry integrated into the gate drive circuitry on each switch. The approach taken in this converter achieves the same protection, but adds more preventative protection for this topology.

Operation of this circuitry is simply analog small-signal analysis, though operation will be described functionally. The non-inverting input of the comparators is connected to the Trip Level Set, which is simply a DC voltage divider (from the regulated rail) with a parallel cap to reduce noise. This level is set based on the particular IGBTs chosen, and should be set at least a diode drop above the IGBT's desaturation voltage. IGBT desaturation occurs when the current through the device exceeds its specifications and the collector-emitter voltage raises even with a fully-applied gate voltage. The diodes connected to collector 1 & 2 are high-voltage diodes that pull down the comparator inverting input when the collector voltage is low. The resistor from VCC to the inverting input is a pull-up resistor for this node so it defaults high unless pulled down by the collector. The diodes from the inverting inputs to ground and VCC are simply protection to ensure the node is never forced to dangerous voltages for the comparator inputs.

The comparator needs to be a high-speed comparator. During normal operation, either collector 1 or collector 2 will be at a low voltage, below the trip

level set on the non-inverting inputs of the comparators. This will cause one of the two comparators to pull down the output, which has a pull-up resistor attached. The comparator pulling down the output will switch every half-cycle, as the conduction IGBT switches. It is possible to have small glitches on the output during the switching transitions, due to practical operation of the switching transitions. Thus, the comparator output node will be high if *both* collectors are above the trip voltage. This can be caused by either desaturation of one of the IGBTs (or both) due to overcurrent, or it can be caused by both IGBTs being in an off state, thus both collector voltages rising to a high voltage. If the latter condition exists, this indicates an issue with either falling out of oscillation or a gate drive issue, either of which could be detrimental and warrant a converter fault condition and shutdown.

Since IGBTs are fairly robust devices, usually having a SCSOA (Short Circuit Safe Operating Area), which is a safe amount of time the device can be fully on with the full voltage across it (huge power dissipation), in the 10's of µs range, a short overcurrent condition will not destroy the device. In order to ignore glitches in the fault circuitry, the output of the comparators is integrated by sourcing current into a capacitor in the Fault Integrator section. If the voltage on the Fault node reaches a high enough level, indicating a fault on the collectors for a significant time, the protection latches on. In the Fault Latch section, the NMOS will turn on when its threshold voltage is reached. Since this is a voltage divider from the Fault node, this transistor turn-on sets the voltage at which the fault activates. Considering the poor regulation over this transistor parameter, the

voltage level can only be estimated. In this application, that was deemed reasonable to accept this tolerance.

As the NMOS in the Fault Latch section turns on, it pulls down the gate of the PMOS, turning it on, which pulls up the Fault node to the VCC rail, latching it on. Pulling down the PMOS gate also pulls current through the LED, activating the Fault Indicator Light. The latched Fault node, at a high voltage, turns on the NMOS transistors in the Gate Drive Disable section. The drains of these transistors connect to the gate drive circuitry, at the Vgi1 node seen in Figure 3-3 (and Vgi2 for SW2). Pulling down the Vgi node immediately pulls the IGBT gates low, forcing them off.

Forcing turn-off has a few consequences in a resonant circuit that is current fed. Since the IGBTs are the only DC current path to ground, disabling both switches cuts off the only path for converter current flow from the input inductor (in the buck stage in Figure 3-1). Since this current cannot immediately stop, the inductor immediately spikes the voltage on its output (input to the transformer), and thus the collectors of both switches. The voltage would rise to one switch's V_{CE} breakdown voltage and avalanche the switch. With correct design, this could be acceptable. To prevent this, a varistor can be placed across each IGBT collector to emitter. The varistor acts similar to a high-voltage highcurrent zener diode, and as long as its breakdown voltage is below the IGBTs, all current flow is directed into the varistors. These devices do add capacitance to the collector nodes, but considering use of resonance, this has no significant negative effect.

3.6 High Voltage Transformer

An integral part of the system, and arguably one of the most mysterious, an HV transformer must step up the voltage from the resonant tank to the input to the voltage multipliers. HV transformers and their associated challenges are discussed in detail in section 1.6, and section 2.7 discusses SRF (Self-Resonating Frequency) and using resonance with these transformers.

Since distributed capacitance cannot be eliminated, it must be considered for this topology. The main concern is the SRF of the transformer, which acts as a parallel resonant circuit on the secondary. Depending on the application, it may be wise to avoid this frequency, or prudent to operate at this condition. Operating the transformer at the secondary's SRF will cause high circulating currents as well as high voltages, effectively boosting the turns ratio. The circulating currents at the SRF will simply be the output voltage divided by the capacitor's reactance. Loss in the secondary near the SRF will be high, likely dominated by secondary I²R losses. If used in pulsed applications, the high loss for a short time may be acceptable, but a steady-state condition would likely overheat the transformer.

Leakage inductance also must be considered for this topology. As the reflected load begins to shunt a significant portion of the magnetizing inductance, the leakage inductance begins to affect operation. The peak voltage in the resonant tank will not change (though frequency may), but the output voltage will decrease due to voltage division between the leakage inductance and the impedance of the magnetizing inductance with the reflected load. A larger leakage inductance will make the onset of this condition earlier, and thus a lesser

possible power transfer. To compound this, the frequency will increase at extremely heavy loads, which will adjust the frequency with regards to the SRF, and will likely create operation above SRF, further reducing the output voltage and power transfer. Thus, as leakage inductance increases, power transfer decreases. High leakage does not invalidate efficiency in this topology, but it must be considered to achieve the desired voltage gain and power transfer capability.

The HV transformer must be designed to output a voltage high enough to support the output voltage under full load after the voltage multiplier. Considering loading and SRF conditions, as well as the voltage multiplier's reflected impedance, this becomes an extremely complex system that is difficult to analyze through conventional methods. The most effective and efficient modeling of the system is through iterative computer SPICE simulations to confirm system parameters are adequate for the design. Due to the complexity of HV transformer design and difficulty in predicting all parasitics, the most practical approach may be to build the transformer, test all parameters, and then adjust other circuit components to compensate for deviations found in the transformer.

3.7 Voltage Multipliers

To ease requirements on the HV transformer, a voltage multiplier is used on the output of the transformer. Detailed operation of a voltage multiplier is described in section 2.8. A four-stage full-wave CW multiplier was chosen in this

topology to provide a significantly high voltage while allowing for a reasonable HV transformer.

Voltage multipliers do increase the voltage, but come at the cost of slower rise and response time, load-induced voltage sag, higher ripple, and increased component count. Despite these disadvantages, they are fairly simple, cheap, easy to design, and simplify the already complex transformer. The converter topology may be modified to include greater or fewer stages of voltage multiplication, depending on the requirements. Whichever the case, Table 2-1 describes the equations used to analyze voltage multipliers, assuming a stiff voltage source. Since the transformer output may be affected by the load of the voltage multiplier, once again, SPICE simulation should be used to verify the operation of the complete converter.

An important consideration for voltage multipliers is the short-circuit condition, whether it be an actual short, or a complete or partial sparkdown on the output. Since a sparkdown condition must be tolerated and survived, the addition of series resistors to the diodes must be made. If the diode peak current is exceeded, all diodes are likely to fail. Addition of correct current-limiting high voltage resistors in series with the diodes prevents excessive diode current in the event of a sparkdown. These resistors do increase power loss and cost, but are a reasonable addition to increase power supply reliability.

3.8 Buck Input Stage

The buck input stage in Figure 3-1 resembles a buck converter, but lacks the output capacitor normally connected to the output of the inductor. A normal buck converter's transfer function is:

$$V_{out} = D \cdot V_{in}$$
(3-3)

Since this pseudo-buck stage is being used as a current source, the current from this stage can be compared to the current that would occur at 100% duty cycle, I_{nom} , assuming constant load:

$$I_{out} = D \cdot I_{nom}$$
(3-4)

And thus the input power, and output power, can be controlled by the duty cycle of this stage. Since it is a buck configuration, the output can be adjusted from full output down to near zero. In practice, there is a lower limit imposed by the necessity of a real oscillation in the tank circuit. If the tank voltage falls too low, the gate drive circuitry fails to operate correctly, and the protection circuitry will activate and the converter will shut down.

The inductor in this stage must be large enough to act as a current source for the resonant tank circuit, requiring an inductance at least two times the resonant tank inductance for a reasonable operation. Depending on the operating frequency of the buck stage, the inductor may need to be larger to prevent excessive current ripple, and thus output voltage ripple. A buck frequency above the resonant tank frequency is desirable to reduce ripple, but may be impractical if the switch needs to be an IGBT rather than a MOSFET.

Operating near the resonant frequency is not recommended due to intermodulation of the resonant and buck frequencies. If they are within 20kHz, the resulting intermodulation frequencies will be within the audible range, and likely the circuit will emit an unacceptable audible tone. Operating below the resonant frequency may be the most practical, as the switching losses will be decreased especially for an IGBT, but the required inductor will be larger and there will be a noticeable output ripple at the operating frequency.

3.9 Converter Design

The general converter operation was described above. What follows is the design of the converter tested in this document, made for the specific application outlined. The converter may be extended to many differing application requiring significant design alterations.

3.9.1 Requirements

Defining power supply requirements involves definition of the converter's use. This converter's main function is to power an X-ray tube. Section 1.5.5 describes a bit about the desirable properties, but the most notable are the fast rise time (<0.5ms) and the low ripple (<3%) required to produce sharp images. X-ray imaging is essentially a very low duty cycle application, requiring only a few milliseconds of on time per image, generally minutes apart. As such, instantaneous power dissipation may not be sustainable for continuous periods.

The converter investigated in this paper is a proof-of-concept converter rather than a complete production-ready converter. As such, the power levels are significantly reduced, size of the prototype is not a primary consideration, and the control loop is not fully implemented. The main objective is therefore to demonstrate operation principles of the proposed converter topology, along with demonstration of the viability of extending this converter to a practical use. This is emphasized over meeting hard design requirements.

Input voltage was chosen to be line-level in the United States, running from 120VAC 60Hz single-phase. Power factor was not a consideration. Input power was limited to below 1500W, considering the normal 15A circuit breaker on standard 120V circuits.

Output voltage was determined to be variable from 20kV to 120kV, differential. Thus, ±10kV up to ±60kV should be obtained in order to power the Xray tube. The maximum output current at 120kV is 8mA, which is 960 watts. Goals are summarized in Table 3-1.

Parameter	Goal
Input Voltage	120VAC, 60Hz
Input Current Maximum	15A
Power Factor	N/A
Maximum Instantaneous Power	960W
Maximum Output Voltages	+60kV, -60kV
Maximum Output Current	+8mA, -8mA
Output Rise Time	<1ms
Output Ripple	<3%
Efficiency	>80%

Table 3-1:	Prototype	Converter	Goals
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3.9.2 Operating Frequency

Converter operating frequency affects the design of every component, so an operating range must be determined prior to final component selection or design. This converter's resonant tank will operate in the range of 50-100kHz. Though this may seem like a wide range, testing of the actual HV transformer will reveal the actual parasitics of the transformer, which are important in deciding operating frequency. The buck input frequency will be adjusted accordingly, to be at least 20kHz below the resonant frequency to avoid intermodulation into the audible frequency range.

Operating near 100kHz necessitates careful consideration of high-speed and high-frequency effects. Semiconductor devices and drive circuitry must be fast enough to ensure switching loss is reasonably low, including fast rise and fall times, low parasitic capacitances, and fast reverse recoveries. Trace and wire inductances must be low to prevent ringing and voltage spikes during highcurrent transitions. All high-frequency high-current paths must have a low AC ESR at the operating frequency to prevent excessive power loss. Design is detailed in the following sections.

3.9.3 High Voltage Transformer

Designing the entire high voltage transformer is an iterative process. The simplest approach, and quite probably the most cost-effective, would be to purchase an available HV transformer that meets the major requirements. If the design must be more custom, it is suggested to work with a specialty transformer

house equipped to work with high-voltage transformers. Designing the entire transformer requires careful consideration of many elements, described in section 1.6.

The transformer was designed specifically for this converter, shown schematically in Figure 3-5.



Figure 3-5: High Voltage Transformer Schematic

The inductance of each primary coil was chosen to be equivalent to the resonant inductor, 200 μ H, making the entire primary 4 times the resonant inductor, thus omitting the majority of the resonant current from the primary. Turns ratio was chosen at 40:1, yielding a voltage gain of 40 if all parasitics are disregarded. Thus, the secondary inductance of each coil should be about 320mH. With a maximum input voltage of 1070 V_{pp}, this yields a maximum output voltage of 42.7kV_{pp}. The center-grounded secondary limits this voltage to two anti-phase 21.3kV_{pp} outputs.

To ensure adequate winding area and power handling capability, a UR64/40/20 Ferroxcube 3C81 core was chosen. To reduce high-frequency loss while maintaining low DC resistance ($2.9\Omega/ft$), Type 2 Litz wire (composed of 7 bunches of 22 strands of 36 AWG) was used on the primary. The split primary consisted of 15+15 turns, and the core had a gap of 0.015 inches. Core power

loss can be calculated based on AC peak flux density, core area, and frequency, and is specified in the datasheet.

$$P_{core} = \frac{P_{per_cm}^{3}}{Volume(cm^{3})}$$

$$\Delta B = \frac{V \cdot s}{V \cdot s}$$
(3-5)

$$B = \frac{1}{2 \cdot A_{\rm C} \cdot N \cdot 10^{-4}}$$
(3-6)

Thus, the peak flux density is about 1000 gauss at full rectified input voltage at 50kHz (highest volt-second stress conditions). This yields a power loss of 70mW/cm³, and a total core loss of 4.3W [28] [29].

Primary RMS currents peaking near 15A with two $45m\Omega$ primaries yield about 20W primary power loss. Secondary RMS currents including circulating currents estimated at 200mA with 110Ω windings yield 9W secondary power loss. At full power the complete transformer is expected to dissipate 39W of power. From the estimated total loss, we can then compute the expected temperature rise of the transformer. Based on the commonly accepted transformer formula for temperature rise based on natural convection:

$$\Delta T = \left(\frac{P_{tot}}{A_T}\right)^{0.833}$$
(3-7)

where ΔT is temperature rise in °C, P_{tot} is total transformer power loss in mW, and A_T is surface area in cm². With a 600cm² surface area of the oil container, the temp rise is about 32°C above ambient in a steady-state condition which is acceptable.

The transformer insulation design requires the use of transformer oil, and was vacuum encapsulated to ensure removal of air. The primary was wound on one leg of the UR core, and the secondary was wound on the other leg, providing insulation through distance. The secondary was carefully wound by hand with 37AWG wire, with each of the two secondaries consisting of 600 turns. Each secondary was sectionalized into 3 sections of 4 layers of 50 turns each to reduce distributed capacitance. The first secondary was wound closest to the core, and the second secondary was wound on top of the first primary (with significant insulation). Minimal Kapton was used, so layers of Kraft paper with oil served as insulation. All wires were routed with care and consideration of high voltage clearance in all directions. Once assembled and a custom leadframe constructed, a custom vacuum chamber was used to lower the transformer into Shell Diala AX transformer oil after a vacuum was pulled for 30 minutes with a 75 micron 2.5 CFM vacuum pump. Figure 3-6 shows the transformer prior to oil submersion.



Figure 3-6: High Voltage Transformer in Air

The resulting transformer was parameterized before and after oil

immersion. As expected, capacitances increased by a factor slightly above 2,

since the dielectric constant of the transformer oil is 2.2. Parameters for the final

transformer are summarized in Table 3-2.

Parameter		Value	Test Condition
Turns	Pri 1 + Pri 2	15 + 15	
	Sec 1 + Sec 2	600 + 593	
	Ratio	40:1	
Core	Туре	UR64/40/20	
	Material	3C81	
	Gap Length	15.0 mils	±0.25 mils
Inductance	Pri 1	203.6uH	10kHz, 0.1Vrms
	Pri 2	205.8uH	10kHz, 0.1Vrms
	Sec 1	371.0mH	10kHz, 0.1Vrms
	Sec 2	377.0mH	10kHz, 0.1Vrms
Q	Pri 1	49.9	10kHz, 0.1Vrms
	Pri 2	51.1	10kHz, 0.1Vrms
	Sec 1	170	10kHz, 0.1Vrms
	Sec 2	160	10kHz, 0.1Vrms
ESR	Pri 1 + Pri 2	90mΩ	DC
	Sec 1 + Sec 2	220Ω	DC
SRF	Sec 1	58.5kHz	Sec1 & Sec2 disconnected
	Sec 2	58.0kHz	Sec1 & Sec2 disconnected
	Sec 1	28.5kHz	Sec1 & Sec2 GND connected
	Sec 2	27.5kHz	Sec1 & Sec2 GND connected
Parasitics	Sec 1 Cap	84pF	Sec1 & Sec2 GND connected
	Sec 2 Cap	88pF	Sec1 & Sec2 GND connected
	Pri 1 Leakage	43.6uH	10kHz - Sec1, Sec2, GND, shorted
	Pri 2 Leakage	46.0uH	10kHz - Sec1, Sec2, GND, shorted
Coupling	Coefficient K	0.89	

Table 3-2: Transformer Parameters

3.9.4 Resonant Components

The complexity of all the resonant interactions required the use of SPICE and hardware testing to choose the final resonant tank values after completion of the transformer. Figure 3-7 has the final values used in the hardware.



Figure 3-7: Resonant Tank Configuration

A Bode plot in Figure 3-8 shows output voltage magnitude (scaled) versus operating frequency for the chosen resonant components. There are distinctively a number of resonant peaks and dips, which occur from interactions of the resonant tank inductance and capacitance, magnetizing inductance, primary and secondary leakage inductances, secondary distributed capacitance, and the reflected voltage multiplier capacitive loading. Simply calculating the resonant frequency of the L and C in the resonant tank will unfortunately provide a resonant frequency far from actual operation, which is why SPICE and hardware testing is necessary to determine operating frequency.



Figure 3-8: Bode Plot of Resonant Stage Output Voltage

Since the resonant components pass a significant high-frequency current, they must be low-loss components. Two capacitors were connected in parallel to achieve 0.090μ F capacitance, with an effective ESR of $10m\Omega$. They are Cornell-Dubilier 940C series metalized polypropylene capacitors designed for large highfrequency currents.

The inductor was a custom-wound inductor similar to the transformer. Using a UR64/40/20 3C81 core gapped 0.025", 7x22x36 Type 2 Litz wire with 19 turns. This yielded a 211.7µH inductor (measured at 10kHz, 0.1Vrms) with 55mΩ ESR at DC. Due to a single-layer construction and Litz wire, AC resistance should be negligibly higher, yielding 0.9W copper loss. Based on equations 3-5 and 3-6, the peak flux density is about 1100 gauss at full rectified input voltage at 70kHz (operation conditions). This yields a power loss of 100mW/cm³, and a total core loss of 6.1W, and total L loss of 7W. Using equation 3-7, with a surface area of 300cm², temperature rise is 14°C which is definitely acceptable [28] [29].

The IGBTs chosen for this application are part number IRGB5B120KD made by International Rectifier. They provide extremely fast rise and fall times for

IGBTs, near 20ns even at a high junction temperature [30]. The NPT (non-punch through) technology allows for easy device paralleling due to a positive $V_{CE(sat)}$ temperature coefficient. Though the device current is low for an IGBT (10A continuous), the advantages of speed and small tail current, along with ability to parallel multiple devices, make this IGBT a good choice.

3.9.5 Voltage Multipliers

Output voltage multipliers to step up the transformer output voltage were designed based on equations in Table 2-1 and availability of components. The maximum transformer output voltage based on turns ratio needs to be multiplied 3 times. A 4-stage full-wave CW multiplier provides ample headroom for voltage sag and various losses as shown in Figure 3-9.



Figure 3-9: 4-Stage Full-Wave CW Voltage Multiplier

470pF 20kV capacitors were chosen, which yields 5.5kV voltage sag at 50kHz or 2.7kV voltage sag at 100kHz. Voltage ripple will be $680V_{pp}$ at 50kHz or $340V_{pp}$ at 100kHz, neglecting any additional output capacitance.

Resistors are each 2Kohm resistors, limiting the maximum current during a sparkdown from the full 60kV to less than 4A through each diode. Datasheet specifications indicate a 3A surge for 8.3ms is acceptable, so a 4A pulse that will decay with the time constant less than 1µs will not damage the diodes. Though average currents in all resistors are equal, the RMS varies depending on location in the multiplier due to the current pulse shape. Power loss from the average current of 15mA is 0.5W per resistor, totaling 16W for both multiplier stacks. Despite this rather large power loss, the reliability benefits in this case outweigh the cost of this extra power.

Diode specifications indicate a maximum forward voltage drop of 35V at 25mA. Estimated power loss from an average of 4mA per diode forward current is 0.14W each, thus 2.2W per stack. Each diode maximum leakage current at 25°C is 1µA, indicating only 60mW power loss due to leakage. At 100°C (significantly above operating temperature), maximum leakage is 25µA, yielding 1.5W loss. The capacitors are low-dissipation (DF<0.001 at 10kHz) doorknob-type capacitors, providing almost lossless operation.

The completed positive segment of the multiplier is shown in Figure 3-10. Due to the high voltages and high frequencies, it is submerged in an oil bath. From the above calculations total power loss for both multipliers at full load is estimated as 22W.



Figure 3-10: Experimental Positive Voltage Multiplier

3.9.6 Buck Input Stage

The buck converter described in section 3.8 is used as the controlling input to the converter. Optimization of the remainder of the converter took priority over this common building block, thus available components were used, which are far larger and more robust than necessary for an optimized design as shown in Figure 3-11. Off-line voltage was isolated through a high-power isolation transformer for safety, then rectified and filtered. A large MOSFET (IRFK2D450) was used and connected to an IR2125 high-side gate drive chip. The PWM input was manually controlled to adjust the output voltage. An ultrafast DSEI30-12A diode provided the freewheeling path. Since the input inductor L3 is effectively averaging the voltage on the switch node into the self-resonant stage of the converter, the steady-state output voltage should be directly proportional to the duty cycle. Inductance of L3 was chosen as 660µH to achieve a low enough ripple. Operating frequency of the buck converter is chosen to be near 40kHz to avoid audible intermodulation distortion.



Figure 3-11: Pseudo-Buck Input Stage

3.9.7 Gate Drive Circuitry

To achieve the desired high speeds the gate drive circuitry utilized extremely small packages such as the SOT-523F package requiring less than $3mm^2$ board area. Figure 3-12 identifies all device values and part numbers, and the circuit operation is described in detail in Section 3.4. Note U12 and U14, used for current sources are small co-packaged transistors to achieve low process variation and high thermal-coupling between the current-mirror transistors' V_{BE} to ensure stable current sources and sinks. Though the currents chosen may seem high, they were deemed reasonable to ensure noise immunity within such a highpower high-voltage converter. A picture of the populated board is shown in Figure 3-12 noting that the scale is in cm.



Figure 3-12: Gate Drive Circuitry Values



Figure 3-13: Populated Gate Drive and Protection Circuitry

3.9.8 Protection Circuitry

Similar to the gate drive circuitry, the protection circuitry's high-speed also necessitated the use of small components as seen in Figure 3-14. Operation is detailed in Section 3.5. The chosen IGBTs (IRGB5B120KD) have a maximum $V_{CE(sat)}$ of 3.7V, so the trip level is set at 4.8V. The integration section yields a response time to a fault of about 1.1µs, detailed in the simulation section. An important note is that the power-on state for the protection circuitry is latched in the protect state. The button across C7 is the protection reset, and acts as the manual startup for the converter after power is applied.



Figure 3-14: Protection Circuitry Values

3.9.9 Small-Signal Power

Gate drive and protection circuitry requires a positive 15V rail (VCC), and a negative 5V rail (VEE). Positive current will not exceed 200mA and negative

current will not exceed 100mA during normal operation. Figure 3-15 outlines the power circuitry implemented in the converter. Based on the respective regulator's datasheet, the positive input can range from 16.3V to 36V, and the negative input can range from -5.2V to -20V [31][32]. Both LT linear regulator chips have internal current limiting and indefinite short-circuit protection, as well as thermal shutdown. Though none of these features should be needed, they provide some protection in the case of an unexpected fault.



Figure 3-15: Small-Signal Power Conditioning

3.10 Design Implementation

A wide variety of techniques from small-signal high-speed analog to highcurrent high-voltage power conversion were utilized to realize this converter successfully. Gate drive and protection circuits were implemented on a dual-layer circuit board custom designed and ordered through ExpressPCB, and all components were surface-mount to ensure a high-speed design. Components were populated with a stereo microscope, precision hot-air gun, and solder paste. The buck input stage's few components utilized the dead bug approach to connect the circuitry. The resonant tank utilized 2oz copper-clad FR4 as its base for the large components and high-current paths. The transformer required custom bobbins and winding, as well as oil and an oil-filled container. To vacuum-submerse the transformer, a custom vacuum chamber was constructed and utilized. The voltage multiplier was submersed in oil due to the high voltages, though did not need to be submersed in a vacuum. A high-voltage cable connected the output to the oil-bathed load, which consisted of multiple highvoltage high-power resistors. This load required the oil bath for both cooling and to prevent corona or any sparkdowns.

CHAPTER 4: SIMULATION RESULTS

4.1 Simulation and Accuracy

Simulation proves to be an invaluable tool for the extremely complex and interdependent circuits common in modern electronics. Advanced modeling and fast computers allow viewing a circuit's operation that would be impossible in the past. Nonetheless, simulation should be used as a beneficial tool, and empirical hardware verification should be the only confirmation of actual circuit operation.

To model the proposed converter, LTSpice IV from Linear Technology was used. This SPICE (Simulation Program with Integrated Circuit Emphasis) software was chosen because of its optimization to efficiently simulate switching power supplies.

Most components could be accurately modeled with manufacturerprovided SPICE models. Some components, however, lack available SPICE models. For the proposed converter, the most notable components without SPICE models were the buck-stage MOSFET, buck-stage freewheeling diode, and the output diodes. Models similar to actual components were chosen to replace these. Circuit functionality will not be affected, but modeled power loss will be affected due to differences in switching loss associated with rise and fall times, forward voltage drops, and reverse recoveries. Inductor core loss was not modeled, nor was transformer core loss. Possibly the most functionally disturbing characteristic not modeled are the circuit parasitics. Lead and wire inductances, trace capacitances, and miscellaneous signal/wire coupling can wreak havoc on

small-signal analog or digital circuitry. High-frequency high-voltage nodes can be significantly affected by minute stray capacitances. Once again, these effects emphasize the requirement of verifying the simulation through empirical measurements and examining waveforms of the actual converter.

4.2 Resonant Stage

Multiple resonant responses in the system show the need for an AC analysis to identify probable operating frequency. Viewing voltage gain on the output (magnitude scaled) as a function of frequency in the input to the resonant tank in Figure 4-1, two peaks are near in magnitude as the largest peaks.





In an attempt to produce an accurate analysis, the AC analysis includes magnetizing inductances, primary leakage, secondary leakage, secondary distributed capacitance, resonant tank components, effective voltage multiplier stages, voltage multiplier sparkdown resistors, and ESR's of all components. Since many of these parameters are somewhat frequency dependent, and simplification was required due to inability to use diodes (in the voltage multiplier) in an AC analysis, error is expected. The effective AC analysis schematic is shown in Figure 4-2.



Figure 4-2: Resonant Stage AC Analysis Schematic

The location and relative magnitude of the resonant peaks indicates a strong resonant frequency near 24kHz and 70kHz, with two minor peaks at 40kHz and 160kHz. Most of these resonant peaks are an interaction of more than two of the reactive components, though that would be an easy calculation. The self-tracking nature of this converter will lock onto a resonance, given it has

a gain high enough to sustain oscillation. Transient analysis of this converter simulates with oscillation at 80kHz, near the higher peak. Oscillating near this peak instead of the equivalent-magnitude peak at 24kHz can be explained by the operation of the diodes in the voltage multiplier.

Without assistance from the diode operation, likely the converter would run at the lower frequency resonance with the higher resonance super-imposed on the waveform (this operation has been seen in both simulation and hardware). The diodes, however, transfer power non-linearly. Figure 4-3 shows current and voltage of the secondary at an operating point (scalable). Note that as the current is drawn abruptly, the slope of the voltage waveform decreases correspondingly.



Figure 4-3: Secondary Output Waveforms

As diodes conduct, they effectively connect additional capacitors in the voltage multiplier which modifies the oscillation. During conduction, the diodes transfer power from the resonant energy, lowering the open-circuit peak of the waveform. As the diodes turn off, the existing higher frequency resonance continues in the
negative direction, maintaining the higher frequency oscillation. The 4-stage voltage multiplier adds to this interaction; a single-stage multiplier would exhibit somewhat different behavior, though still similar.

Secondary current and all corresponding diode currents are shown in Figure 4-4. The addition of all diode currents together yields the secondary current. Lower multiplier stages near the secondary have softer current waveforms that start later, and diodes closer to the output have a harder and earlier turn-on. All diodes are not on at exactly the same time, and as such the resonance is affected. Including the higher stages in the converter causes an earlier and sharper onset to the current drawn through the secondary, as opposed to a single stage. In this way, the conduction-induced resonance modification is altered by the number of multiplier stages.



Figure 4-4: Secondary Winding and Diode Currents

The above discussion of complex interactions and non-linearities demonstrates the need for simulation in order to determine the actual operating frequency. A transient analysis results in an operating frequency ranging from 70kHz to 82kHz which is acceptable and within the desired 50-100kHz range. The frequency is also found to be only slightly load or buck duty cycle dependent.

4.3 Gate Drive

Special attention was paid to speed in the gate drive circuitry. Specifically, an extremely low delay time (propagation delay) was desired. Though many commercial chips are "high-speed," this usually refers to the rise and fall speeds instead of the propagation delay, which is often in the hundreds of nanoseconds. Simulation indicated the gate drive circuitry to be extremely fast. Figure 4-5 shows the turn-on and turn-off transitions given an input with a 2ns rise and fall time and driving a purely capacitive 1nF load.



Figure 4-5: Gate Drive Operation Speed

Rising propagation delay was noted at 2.4ns (6Vin to 6Vout) with a rise time (10% to 90%) of 2.1ns. NPN current peaked at 7.4A. Falling propagation delay was 4.7ns (6Vin to 6Vout) with a fall time (90% to 10%) of 5.7ns. PNP current peaked at 2.6A. The positive current slew is 3.7A/ns which would generate 10V across a 2.7nH trace inductance! Simulation did not include parasitics like these,

which will doubtlessly slow transitions, but the simulation proves the speed of the circuitry given proper layout.

Proper operation is shown in Figure 4-6, showing one IGBT's collector voltage and current under full load, and the corresponding gate voltage. Note the short notch of negative voltage as the gate turns off. This is the gate turn-off latch working as described in section 3.4. The gate drive circuitry simulation indicates flawless performance.



Figure 4-6: Gate Operation

4.4 Protection Circuitry

Protection of the IGBTs is implemented through pulling both gates low in the case of a fault as described in section 3.5. The simulation indicates the fault circuitry will latch in the protect state in response to any fault longer than a 1.1µs duration as shown in Figure 4-7.



Figure 4-7: Protection Circuitry Operation

Fault onset (of a 1.1µs fault) to latching of the fault node takes 4.1µs, and from fault onset to the gate drive's fall (fall time 4.0µs) takes 7.4µs. Delays in this system are due to the time constants of the input resistors and input capacitance on the associated MOSFETs. If the fault persists, fault onset to latching takes 3.2µs, and from fault onset to gate drive's fall takes 5.5µs. These response times are adequately fast to ensure protection in this topology for IGBTs.

4.5 Output Voltage

The converter's desired output characteristics of fast rise time and low output voltage ripple were simulated and are shown in Figure 4-8. Only the positive output voltage is shown because the negative output voltage is a mirror image.



Figure 4-8: Output Voltage Rise Time and Ripple

Rise time (0-90%) run open loop for a full load condition is 1.77ms. Simulations indicate a closed loop control would slightly increase this speed to about 1.5ms. A lighter load condition would allow for faster rise times. Output voltage ripple is $655V_{pp}$ or 1.09%. Note the ripple is at double the operating frequency due to the full wave voltage multiplier. The clear asymmetry of the ripple waveform is due to the slightly unequal secondary inductances and distributed capacitances which were included in the simulation. Additional output capacitance due to load

configuration and output connection parasitics could significantly affect the ripple and rise times.

A short circuit condition (200μ s, $1m\Omega$) from the positive output to ground is simulated in Figure 4-9. Since a sparkdown can be viewed as a momentary short circuit, operation in this condition is extendable from this demonstration. Parasitic inductances both in the voltage multiplier stage connections and the short path are included in the simulation assuming a short with the shortest physical path.



Figure 4-9: Simulation of a Short Circuit

Initial peak current rises to 790 amps and oscillates at 17MHz with a fast exponential decay. The short circuit creates a high-Q series resonant circuit that oscillates due to the step short circuit. The capacitors, which are high-surge capable, should not be damaged by a short circuit condition or sparkdown. The diodes on the contrary may suffer damage due to high pulse currents in the upper stages. Assuming the diodes do not fail from the surge, the converter continues operation with a DC output of 58mA short-circuit current. During a short circuit on both positive and negative outputs, the input power is simulated as 120W. Of that, 90W is dissipated in the voltage multipliers' sparkdown resistors. Though this power loss is undesirable, it is functionally acceptable considering all resistors are rated for over 5W and are bathed in oil. The uninterrupted primary resonant oscillation and rise of the output voltage after the short is released demonstrate the immunity of the primary circuitry to an output short.

4.6 Efficiency

Efficiency simulation results are tabulated in Table 4-1 and graphed in Figure 4-10. The efficiencies of the buck, resonant, and voltage multiplier stages were derived from simulation data and are shown separately to better characterize the sources of loss.

% Rated Power	Buck Duty Cycle	Output Voltage (kV)	Power Output (W)	Power Input (W)	Buck Efficiency	Resonant Efficiency	Multiplier Efficiency	Total Efficiency
100.3%	93.9%	60.101	963.2	1067.0	97.8%	93.8%	98.3%	90.3%
96.4%	92.0%	58.905	925.3	1024.4	97.9%	94.0%	98.2%	90.3%
88.2%	88.0%	56.335	846.3	938.7	97.9%	94.0%	98.0%	90.2%
80.4%	84.0%	53.796	771.7	857.6	97.9%	94.1%	97.7%	90.0%
70.9%	79.0%	50.537	681.1	756.8	97.9%	94.4%	97.4%	90.0%
62.2%	74.0%	47.314	597.0	664.7	97.9%	94.4%	97.2%	89.8%
50.8%	67.0%	42.757	487.5	544.1	97.7%	94.6%	97.0%	89.6%
42.0%	61.0%	38.896	403.5	451.1	97.7%	94.6%	96.8%	89.4%
31.5%	53.0%	33.684	302.6	340.1	97.5%	94.6%	96.5%	89.0%
21.5%	44.0%	27.806	206.2	233.6	97.2%	94.4%	96.2%	88.3%
12.5%	34.0%	21.234	120.2	138.4	96.1%	93.9%	96.2%	86.8%
4.0%	20.0%	12.030	38.6	47.1	92.7%	91.8%	96.3%	82.0%

Table 4-1: Converter Efficiency with Constant Resistive Load



Figure 4-10: Converter Efficiency Based on Simulation

Figure 4-10 shows that simulated efficiency is above 90% at rated power,

and does not dip below 85% efficiency until 10% power. This indicates a

relatively efficient converter. The resonant stage which includes the transformer, resonant tank components, and IGBTs, maintains near 94% efficiency across the range (η _Res). The buck stage which includes the buck MOSFET, freewheeling diode, and input inductor, simulates efficiencies nearing 98% across the range (η _Buck). The voltage multiplier stage, including the damping resistors, ranges from 96% to 98% efficiency (η _CW) and notably does not drop in efficiency at very light load.

Despite the optimistic simulation results, inadequacies of SPICE must be considered. Since the buck stage MOSFET and diode lacked a correct simulation model, likely their efficiencies will be lower than simulated, especially considering a buck achieving 98% efficiency is almost exclusively reserved for soft-switching rather than this stage's hard switching. Neither inductor power loss was included, nor was the transformer core power loss. Inclusion of all of these losses will likely decrease efficiency by approximately 3-7%.

CHAPTER 5: HARDWARE RESULTS

5.1 Hardware Test Setup

The proposed converter topology was implemented and tested entirely in the author's private laboratory with no use of equipment or financial assistance from the California Polytechnic State University, San Luis Obispo, or any other external organization. A photograph of the converter test setup is shown in Figure 5-1 with converter sections appropriately labeled. A United States dollar bill is also shown to indicate scale.

Small size was emphasized in the resonant stage and transformer, since these present the most difficulty in miniaturization. Other components did not receive the same detailed attention to size. The 60Hz input filter and buck inductors are completely functional but significantly larger than necessary. The voltage multiplier's size could be reduced with a redesign. Due to the short duration of testing and thermal masses, no components required forced-air cooling, though a fan was placed across the small-signal components and IGBTs for safety.

As a load rated for 60kV is not a common piece of equipment, highvoltage high-power Cableform CJF series 7.5 Meg Ω 3% resistors were obtained and implemented in an oil bath. The load was connected through a 10-foot 75kVrated X-ray cable for safety, attached to the voltage multiplier. The load consisted of four 7.5 Meg Ω resistors, with two parallel sets in series yielding a total load resistance of 7.5 Meg Ω rated for 250kV and over 400 watts continuous power.

Figure 5-2 is a picture of the load setup. As a scale, each resistor is 18.5" long and 2" diameter.



Figure 5-1: Experimental Setup



Figure 5-2: High-voltage Load in Oil Bath

Table 5-1 lists the equipment used for test setup and measurements.

Equipment	Manufacturer	Model #	Measurement Function
Multimeter	Fluke	8840A	Input Voltage
Multimeter	Hewlett Packard	3466A	Output Voltage
HV Probe	Fluke	80K-40	HV Output voltage
Multimeter	Fluke	8050A	Output Current
Multimeter	Craftsman	82022	Input Current
Power Supply	GoldStar	GP-303	Gate Voltage Positive
Power Supply	Power Designs	TP340	Gate Negative Voltage
Current Probe	Tektronix	A6302	Current Probe
Current Probe	Tektronix	AM 503	Current Probe Amplifier
Pulse Generator	Philips	PM 5712	Buck PWM Signal
Oscilloscope	Hewlett Packard	54602B	Viewing Waveforms
Oscilloscope	Tektronix	466	Viewing Waveforms
Oscilloscope	Tektronix	7904A	Viewing Waveforms, Mainframe
Oscilloscope Plug-in	Tektronix	7A26	200MHz Vertical Amp
Oscilloscope Plug-in	Tektronix	7B92A	Delaying Time Base

Table	5-1:	Test	Equi	pment	Utilized
rubic	0 1.	1000	Lyan	princin	Cunzoa

5.2 Hardware Troubleshooting

Simulation results were promising, but initial hardware tests did not instill the same hope as simulation. Parasitics causes significant issues with the highspeed gate drive circuitry. A high frequency oscillation on the gates and drains appeared at every switching transition, preventing operation above 5% load and creating higher switching losses. Figure 5-3 shows an experimental waveform with low input voltage and output power from the IGBT gates. Significant and calculable known parasitic were added in simulation and resulted in a similar waveform as depicted in Figure 5-4. Simulation oscillations were at 27MHz, while experimental oscillations were at 21MHz.



Figure 5-3: Gate Drive Oscillations at Low Input Voltage, 5V/div, 200ns/div



Figure 5-4: Gate Parasitic Oscillation Simulation

The oscillation was fixed by slowing down the response of the cross-coupled diode pull-down circuitry. A 100Ω resistor was added in series, and a 150pF capacitor to ground was added on the anode of the diode. Also, the resistor connected from the diode anode to the drain of the MOSFET in the gate turn-off latch section was changed from 75Ω to 51Ω to assist in faster pull-down.

The fault protection worked very well in preventing circuitry failure, as no primary side power components failed during testing. Unfortunately, cases of false positives presented bothersome interruptions. The cause was traced to variation in the pull-down diode drop, $V_{CE(sat)}$, and ground sag and bounce caused by higher currents and parasitic inductances. To overcome false triggering without sacrificing correct operation, the trip voltage was set to 7.3V which is 2.4V higher than originally set. Though this is well above the $V_{CE(sat)}$ voltage, if the IGBT is coming out of saturation, voltage rises very quickly with increasing current, and hence this voltage difference is not significant.

5.3 Hardware Testing

Testing followed a rigorous procedure before start-up to ensure safety with such a high-voltage system. The control, measurement systems, and shut-down switch were far from the high voltage output, as was the operator during operation.

Testing was performed primarily on the resonant stage and a single positive voltage multiplier. Failure of the high voltage transformer during testing, described later in section 5.10, prevented testing of a negative voltage multiplier and prevented full characterization of the buck stage. Though the buck stage was not characterized regarding efficiency or output voltage vs. duty cycle, viable operation was confirmed by testing it in the complete system. A buck stage is common and relatively simple, and implementing such a stage is nothing new, complex, or essential to proving the viability of the converter topology. No negative voltage multiplier was tested for the same reasons, though operation and stresses are almost identical to the positive multiplier stage. The positive stage's performance indicates a negative voltage multiplier would work just as well.

For characterization of the resonant stage, the output of the AC filter capacitor was connected directly to the input inductor that is connected to the center-tap of the transformer's primary. This effectively makes the buck duty cycle 100% and removes any losses associated with the buck converter. Thus, measured efficiencies will not include losses from the buck stage which would

reduce efficiency. Input voltage was controlled through the use of a fused autotransformer connected to the AC filter.

In connecting the input voltage to the power line, any variation in the power line transfers to the input and output voltages and will cause fluctuation in readings. To ensure accurate efficiency measurements, all voltage and current readings were taken simultaneously. Nevertheless, due to asynchronous instrument refresh rates, not all instruments will be reading the same interval. This will undoubtedly cause some small error in efficiency measurements.

Measuring high voltage proved difficult. A high-precision strand of 5 200MegΩ 2W 1% resistors was submerged in oil, and current was measured in the return path, but a combination of the leakage currents at that voltage, and difficulty in controlling oil surface effects yielded unacceptable error. The Fluke 80K-40 high voltage probe was used to calibrate the high voltage measurement, but is only rated for 40kVDC. The decided method to measure above 40kV was to measure the return current on the load resistors and calculate the voltage based on the resistance. Since this resulted in errors less than 0.5% up to 40kVDC when comparing to the probe measurement, this method was used up to the maximum 60kVDC. It is also safer because all high voltage leads can be submerged in oil, as opposed to the free-air probe.

5.4 Efficiency Results

Table 5-2 displays the tabulated efficiency results. As mentioned before, these measurements do not include the buck stage, and only reach 50% power due to the transformer failure described later in section 5.10. Only the positive voltage multiplier was investigated, thus maximum output power for this experiment was 50% of the simulated power. Due to measurement jitter from the power line, many measurements were made and are graphed in Figure 5-5 along with an actual expected efficiency line based on data.

The required input voltage to achieve an output voltage was lower than expected. Simulation required a 135V input to achieve 60kV with 50% load in the same configuration, but experimental results only require a 112V input. This is explained by slight differences in the resonant stage gain discussed previously in section 4.2.

Vin	lin	Vout	lout	P_in	P_out		
(V)	(A)	(kV)	(mA)	(W)	(W)	% Load	Efficiency
31.99	1.355	15.77	2.106	43.3	33.2	3.46%	76.62%
32.17	1.374	15.97	2.120	44.2	33.9	3.53%	76.60%
32.0	1.429	16.208	2.161	45.7	35.0	3.65%	76.59%
33.08	1.475	16.73	2.221	48.8	37.2	3.87%	76.15%
40.7	1.777	20.46	2.723	72.3	55.7	5.80%	77.03%
50.83	2.367	26.61	3.548	120.3	94.4	9.83%	78.47%
52.4	2.339	26.88	3.572	122.6	96.0	10.00%	78.34%
52.7	2.505	27.66	3.688	132.0	102.0	10.63%	77.27%
62.3	2.815	32.15	4.282	175.4	137.7	14.34%	78.50%
66.58	3.020	34.39	4.581	201.1	157.5	16.41%	78.35%
65.6	3.079	34.53	4.599	202.0	158.8	16.54%	78.62%
70.8	3.230	36.50	4.857	228.7	177.3	18.47%	77.52%
70.7	3.510	37.635	5.018	248.2	188.9	19.67%	76.10%
71.0	3.386	37.703	5.027	240.4	189.5	19.74%	78.84%
77.6	3.566	40.01	5.32	276.7	212.9	22.17%	76.92%
86.3	4.17	45.50	6.03	359.9	274.4	28.58%	76.24%
92.9	4.44	49.163	6.555	412.5	322.3	33.57%	78.13%
99.6	4.84	53.025	7.07	482.1	374.9	39.05%	77.77%
100	4.78	53.25	7.10	478.0	378.1	39.38%	79.10%
105	5.04	55.80	7.44	529.2	415.2	43.25%	78.45%
112	5.53	60.00	8.00	619.4	480.0	50.00%	77.50%
113.15	5.51	60.225	8.03	623.5	483.6	50.38%	77.57%
113.0 <u></u> 5	5.41	60.225	8.03	611.6	483.6	50.38%	79.07%

Table 5-2: Converter Efficiency Data Excluding the Buck Stage



Figure 5-5: Converter Efficiency Excluding the Buck Stage

Simulated results compiled excluding the buck stage are compared to

measured results in Figure 5-6.



Figure 5-6: Simulate and Measured Efficiencies Excluding the Buck Stage

It is clear the converter's efficiency fell far from the simulated efficiency, providing efficiencies around 78% when simulation showed near 92%. Though only tested to 50% load, based on the trend and similar simulation trends, converter efficiency is expected remain just below 80% from 50% load to 100%.

Investigating power loss, the converter was run continuously at 100 watts output to determine heat sources. At this power level, 30 watts were dissipated in the converter. Identifying and characterizing power loss from the transformer and voltage multiplier was difficult due to oil submersion. The IGBTs, on the other hand, dissipate heat through well-characterized heatsinks. Relying on natural convection and temperature rise after running steady-state, the total IGBT loss was estimated at 20-22 watts. This accounts for 70% of the converter's total loss which is much higher than expected. The collector voltages appeared as expected, but the current waveform of the emitter as shown in Figure 5-7 indicates a significant source of power loss.



Figure 5-7: Emitter Current, 2A/div, 5µs/div, 50% load

As a comparison the emitter current waveform in simulation is illustrated in Figure 5-8.



Figure 5-8: Simulated Emitter Current Waveform

Focusing on wave shape rather than magnitude, the current waveform shows a large tail current characteristic of IGBTs that is not apparent in simulation. IGBT models used in simulation were manufacturer-provided sub-circuits designed to model this particular IGBT, and do include a small tail current. These particular IGBTs were chosen for their fast switching times and expected low tail currents. The enormous tail current apparent in measurement definitely causes very high power losses compared with expected losses. This single issue accounts for the majority of the discrepancy in simulated vs. actual efficiency.

5.5 Collector Waveforms

The collector waveforms of this converter are one of its most distinct characteristics. Ideally, the waveform would be a clean half-sine wave peaking at π times the input voltage. Figure 5-9 shows the waveforms of both collectors at the full 60kV 8mA output with 113V input. The waveform appears at 69kHz as

expected except for a small glitch at the switching transition. Figure 5-10 shows the glitch, which is a spike to about 75V for about 50ns.



Figure 5-9: Collector Waveforms, 50V/div, 5µs/div, 113Vin, 50% Load



Figure 5-10: Collector Waveform Glitch, 50V/div, 100ns/div, 113Vin, 50% Load The glitch on both collectors is due to the slowed gate drive circuitry which was required due to circuit parasitics. Since the opposing gate's cross-coupling is slowed, a small delay is introduced where effectively both gates are low and both

IGBTs are off. This in turn causes the input current to the tank circuitry to raise both collector voltages equally until one IGBT begins to turn on and pull the voltage back down. A power loss will be associated with this delay, as the IGBTs are operating in a linear range as they rise and fall, but the loss is small compared to the loss from tail current described earlier.

5.6 Gate Waveforms

After the modification described in section 5.2, the gate drive circuitry behaved very well. Waveforms of both gates are shown in Figure 5-11.



Figure 5-11: Gate Waveforms, 5V/div, 2µs/div

The turn-on has a small plateau at the threshold voltage, characteristic of MOSFETs and IGBTs and accentuated by the slowed gate drive circuitry. The negative notch during turn-off is the proper operation of the gate turn-off latch holding the gate low.

5.7 Resonant Currents

All currents in the resonant tank and transformer should be sinusoidal. The transformer primary current and resonant inductor current are shown in Figure 5-12 and Figure 5-13, respectively.



Figure 5-12: Transformer Primary Current, 5.0A/div, 5µs/div, 40% load



Figure 5-13: Resonant Inductor Current, 2.0A/div, 5µs/div, 50% load

The transformer primary current was captured at 40% load rather than 50% load due to current probe limitations imposed by its specifications [33]. The transformer primary RMS current at 40% load is 6.7A. The resonant inductor RMS current at 50% load is 2.4A. Increasing load will increase transformer current, but resonant inductor current will only increase minimally.

5.8 Input Inductor Currents

Input inductor currents were measured in Figure 5-14 and Figure 5-15 with the buck stage bypassed, preventing any buck ripple. All ripple is due to the resonant circuitry at 50% load. Figure 5-15, which is AC coupled, indicates a peak-to-peak ripple of 0.3A superimposed on the 5.4ADC. The ripple is at 138kHz, and slightly asymmetrical. The slight ripple at 69kHz in the waveform is due to the differences in the two secondary windings causing slight differences in power transferred per half-cycle, and thus input current.



Figure 5-14: Buck Inductor Current with 100% Duty Cycle, 2A/div, 5µs/div, 50% Load



Figure 5-15: Buck Inductor Current at 100% Duty Cycle, 0.2A/div AC Coupled, 5µs/div, 50% Load
Figure 5-16 shows the input ripple due to the buck stage, as well as the
buck switch node. The resonant current ripple can be clearly seen superimposed
on a standard asymmetric triangle buck current waveform. Input voltage was only
38V and load was only 6% since the transformer failure prevented complete
testing, but the waveform shape can be extended to higher powers.



Figure 5-16: Input Inductor Current (top, 0.1A/div) and Buck Switch Node (bottom, 50V/div), 10µs/div, 38Vin, 6% load

5.9 Output Voltage Ripple & Rise Time

The output voltage ripple and rise time were not characterized due to the transformer failure's interruption of testing. Both of these characteristics will be affected by the output capacitance. Using an X-ray cable, which is coaxial high-voltage cable, additional capacitance appears on the output. 10ft of this cable was used whose capacitance was measured as 410pF. Considering the expected and simulated output capacitance of 120pF, this additional capacitance will significantly reduce output ripple and increase the rise time. Through a high-voltage capacitive voltage divider, the output voltage ripple was measured at 10.5kV and 1.4mA output to be $17V_{pp}$ or 0.16%. Calculations from this measurement indicate about 550pF of total output capacitance. Extending this to

full load, ripple can be calculated as $94V_{pp}$ or 0.16%. The added capacitance significantly improves ripple well within the 3% specification, but it doubtlessly slows rise times. Unfortunately, rise times were unable to be investigated due to transformer failure described below.

5.10 HV Transformer Failure

During testing of the positive voltage multiplier, the high voltage transformer failed catastrophically. Due to the critical nature of the transformer to the converter and the complexity of reconstructing the transformer, testing ceased. To recount the conditions, from a cold start the converter was run at full output voltage successfully, fully stressing the positive voltage multiplier, for about 20 seconds when the transformer failed. It immediately released smoke bubbles through the oil from its secondary winding, and ceased outputting voltage. A hasty glance before lunging for the turn-off switch noted no fault protection had been enabled, and the primary of the converter was still oscillating. After investigating the fault and reapplying power, the converter's primary effortlessly oscillated at 55kHz and drew only a hundreds of milliamps from the supply.

Investigating the transformer failure, the primary inductances measured only the leakage, indicating a shorted secondary. Secondary 1 had the expected leakage, but secondary 2's leakage was one third the expected value, indicating the failed winding. Black flecks of debris were floating in the oil from the failure. The point-of-failure is unknown, though a thorough transformer autopsy has not

been performed. Since the converter ran with a constant output voltage for 20 seconds, an internal breakdown due to overvoltage stress is not suspected, especially since the transformer oil's breakdown voltage temperature coefficient is positive. It is hypothesized that the circulating currents in the secondary caused I²R heating to the point of melting the enamel insulation on two adjacent windings. In that instant, the two adjacent windings shorted and the transformer's secondary became one turn of 37AWG wire rather than 600 turns. Now a step-down transformer with high current capability, the transformer forced immense currents through that one turn of fine wire. Catastrophic failure occurred as the wire melted itself and all wires adjacent, compounding the failure and likely causing arcing as some wires disconnected and others melted together. The result was smoke, a shorted output, and the need for the transformer and its operator to cool off.

Continuing oscillation at 55kHz with a shorted secondary indicates the self-tracking gate resonant stage is simply oscillating with the leakage inductance. Since there is no longer power throughput, the converter happily resonates with low quiescent power. Though transformer failure was an unfortunate incident through and through, it does indicate the inherent protection of the primary circuitry to an output short circuit on the transformer.

CHAPTER 6: CONCLUSION

6.1 Summary

The proposed Resonant Self-Tracking Current-Fed Converter (RST-CFC) operation principles were verified through simulation and hardware testing. During development, the topology underwent many iterative changes and simulations to optimize the design. The converter would not have been possible if the groundwork for the resonant stage had not been laid by J. Paolucci in [23]. Through countless tests and simulations, and just as many discounted ideas, this RST-CFC converter emerged to be investigated. Through hardware testing and troubleshooting, the operational theories of the proposed converter were successfully verified. Many unexpected complications and intricacies arose during verification of the hardware, but through untold hours the converter was brought to fervent life. The converter's operation was similar to expectations, but some significant quantitative discrepancies were identified and explained.

An output voltage of +60kV at 8mA (480W) was achieved, providing 50% load. The negative output voltage multiplier was never tested due to transformer failure, thus the converter was not tested beyond 50% load. Efficiency slipped by at 78% at 50% load, which is much lower than the simulated 92%. Efficiency this low is unacceptable for a high-efficiency commercial converter, but the main source of power loss was determined to be due to the resonant stage IGBTs' tail current. These losses did not appear in simulation despite using the IGBTs'

manufacturer-provided SPICE models. The buck stage was not included in the efficiency measurements or calculations due to transformer failure.

Output voltage ripple and rise time depend heavily on output capacitance. The X-ray cable safely connecting the output to the load added four times the expected output capacitance, and hence reduced output ripple voltage to 0.16%. The output rise time also suffers from this capacitance which was not included in simulation and was not experimentally verified.

The high voltage transformer failed catastrophically during testing. This prevented full converter characterization, such as inability to test the negative voltage multiplier, the buck input stage, output voltage ripple, or output rise time. Failure was due to extended operation (20 seconds) at 50% load, resulting in over temperature of the secondary winding and causing an internally shorted secondary. Prior to the failure, the hardware was verified and operated functionally as described in detail in Chapter 5.

As a proof-of-concept, this converter achieved the expected verification goal as described in section 3.9.1. The functionality and viability of the converter was confirmed by the experimental results that correlated with simulation. The positive outcome of this investigation warrants further improvement and investigation of this converter as described below.

6.2 Future Work

Viability of the converter was clearly demonstrated, but future work is needed to optimize the system. Most notably, efficiency improvements need to

be made. Then, this converter should be extended to higher input voltages and power throughput.

The transformer did not fail because it was designed poorly, but rather it was due to extended operation beyond its design. If operation will be a low duty cycle with pulse widths less than 1 second, the transformer as tested would work well. For continuous operation, a more suitable transformer is needed. To reduce power loss in the secondary, the distributed capacitance should be further reduced which will lower the secondary circulating currents and I²R losses and improve efficiency.

Proper operation of the negative voltage multiplier should be verified by connecting it to the output of the transformer and attaching it to another load. This allows reaching 100% load instead of the measured 50%. Larger stresses on the primary should not introduce any problems, but this should be tested thoroughly.

Complete implementation of the buck stage and control loop was not achieved, though should be investigated. A buck input stage is relatively simple and should be easily implemented and tested. The control loop, though, may be difficult. The complete converter transfer function has not been derived, but will be a compound transfer function based on the buck input, resonant stage, and voltage multiplier. A complete and accurate transfer function is likely to be elusive due to the extremely complex interactions of the components in the resonant stage. Nonetheless, a low-bandwidth control loop should be reasonable to implement using voltage-mode control.

Power loss in the IGBTs must be reduced. Too much power is wasted solely in these devices to achieve a high efficiency. Since tail currents dominate the cause of loss, and the tail current is a fairly unchangeable property of a particular IGBT, two main options exist: different IGBTs could be chosen which have lower tail currents, or the frequency of the resonant converter operation could be lowered. The former would require testing many different IGBT tail currents since datasheets do not include that information for a zero-voltage turnoff, and it could be difficult to find a device with lower tail currents. The latter would reduce the power from the IGBTs to some degree, but would require larger magnetics to support the increased volt-seconds caused by lower frequency.

Once the above issues are explored and work properly, application of this converter to higher powers should be investigated, since 960 watts will power only the smallest X-ray tubes. Though MOSFETs could be used at the input voltages tested, IGBTs were chosen to provide extension of their use in this converter at higher voltages, since MOSFETs lack high enough voltage capability. Utilizing a 480V 3Φ line input would allow for more power and require higher voltage IGBTs to support the collector voltages. All components of the system are scalable to higher power levels.

6.3 Conclusion

Advancements in power electronics continue to form the power conversion field and push the limits of efficiency and miniaturization. Rather than a single event, it is an expanding collection of information that signifies advancement in

this field. Investigating in detail the Resonant Self-Tracking Current-Fed Converter presented in this paper represents another small step forward for the field of power electronics.

Some quantitative goals set forth for the converter were met. However, some others faced several issues. For example, due to the high voltage transformer's breakdown, a negative output voltage was never investigated, rise time was not measured, full load not achieved, the buck stage not characterized, and efficiency was lower than desired. Despite these issues, the converter investigation and documentation is credited as a success.

All theoretical operating principles of the proposed converter topology were positively confirmed through proper operation and verification of the associated waveforms. Every condition, good or bad, seen in the converter was successfully simulated, reasonably explained, or both. The investigation and explanations demonstrate an understanding of each condition's causes, and such work lays the foundation for future improvements, modifications, and advances in the field of power electronics.

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APPENDIX

Gate Drive and Protection Circuitry PCB Layout:



Left: top layer. Right: bottom layer.

2 oz copper, no solder mask or silkscreen

Dimensions: 1.25" x 2.5"

All black circles indicate plated through-holes



IGBT daughter boards for heatsink mounting and IGBT paralleling:

Left: top layer. Right: bottom layer. 2 oz copper, no solder mask or silkscreen Dimensions: 0.75" x 1.25"

All black circles indicate plated through-holes

<u>Item</u> #	<u>Quan</u> tity	Price(ea) /per	Price:		Descr	iption	Supplier	Part #	Package
		 F 0/1	¢15.00		IC LDO REG ADJST		Disilian		0000
- 1	3	5.8/1	\$15.00	U	NEG 500MA	LIII/5CS8#PBF	Digikey	LT1175CS8#PBF-ND LT3080EST#TRPBFCT-	82010
2	3	4.2/1	\$15.00	U	IC REG LDO ADJ 1.1A	LT3080EST#TRPBF	Digikey	ND	SOT223
3	10	0.178/5	\$2.00	С	VS SMD	EEE-1VA220WR	Digikey	PCE3953CT-ND	5mmD
4	6	0.16/1	\$1.00	D	LED SMARTLED YELLOW 587NM	LY L29K-J1K2-26-Z	Digikey	475-2794-1-ND	0603
5	6	0.68/1	\$3.00	D	Dual TRANSISTOR NPN AF 45V	BC 847S E6327	Digikey	BC847SE6327INCT- ND	SOT-363
6	6	0.68/1	\$3.00	D	Dual TRANS PNP 60V 1A	PBSS5160DS	Digikev	568-4351-1-ND	SC-74
7	30	0 248/10	\$8.00	D	DIODE SW 75V 4NS	1N4148WT	Digikey	1N4148WTCT-ND	SOD- 523E
,	00	0.210/10	<i>\\</i> 0.00		TRANS HP NPN 50V		Digitey		0201
8	6	0.76/1	\$4.00	Q	2000MA TRANS SW PNP 40V	FMMT619TA	Digikey	FMMT619CT-ND	SOT23-3
9	6	0.6/1	\$3.00	Q		FMMT720TA	Digikey	FMMT720CT-ND	SOT23-3
10	10	0.38/1	\$4.00	Q	200MA	MMBT3904T	Digikey	MMBT3904TCT-ND	523F
11	10	0.38/1	\$4.00	Q	TRANS PNP 40V 200MA	MMBT3906T	Digikey	MMBT3906TCT-ND	SOT- 523F
12	6	0.3/10	\$2.00	D	DIODE SCHOTTKY 30V	BAT54WX-TP	Digikey	BAT54WX-TPCT-ND	SOD-523
13	0	0 248/10	\$0.00	D	DIODE SW 75V 4NS	1N4148WT	Digikey	1N4148WTCT-ND	SOD- 523E
14	10	0.215/10	\$2.00	0	MOSFET N-CH 50V		Digikov		6070.2
14	10	0.315/10	\$3.00	Q	MOSFET P-CH 50V	B33138W-7-F	Digikey	B22138W-FDICT-IND	3070-3
15	6	0.315/10	\$2.00	Q	130MA	BSS84W-7-F	Digikey	BSS84W-FDICT-ND	SC70-3
16	5	0.88/1	\$4.00	U		LM319DT	Digikey	497-1576-1-ND	14-SOL
17	10	0.133/10	\$1.00	D	630NM	LS L29K-H1J2-1-Z	Digikey	475-1195-1-ND	0603
18	4	0.61/1	\$2.00	R	SUR ABSORBER 10MM 910V	ERZ-V10D911	Digikey	P7213-ND	10mmAx
19	1	5.3/1	\$5.00	т	TWEEZER STLE 7 ORGE CRVD FNE PNT	18072EZ	Digikey	243-1055-ND	NA
20	10	0.638/10	\$6.00	D	DIODE ULTRA FAST 1200V 1A SMB	STTH112U	Digikey	497-2460-1-ND	SMB
20		01000/10	÷0100	5			Digitoj		0603
21	10	0.281/10	\$3.00	С	4.7uF 0805, 25V	GRM21BR61E475KA12L	Digikey	490-3335-1-ND	0603
22	20	0.079/10	\$1.00	С	1u	GRM188R61E105KA12D	Digikey	490-3897-1-ND	
22	30	0.010/10	\$0.50	C	100n		Digikov	490-1524-1-ND	0603
23	50	0.017/10	\$0.50	C	10011	UNITION TETO AND	Digikey	470-1324-1-ND	0603
24	20	0.044/10	\$1.00	С	10n	C1608X7R1E103J	Digikey	445-5099-1-ND	0402
25	20	0.032/10	\$0.50	С	1n	CC0603JRNPO8BN102	Digikey	311-1342-1-ND	0803
26	20	0.022/10	\$0.50	C	0.1p	C1608C0C1H1011	Digikov	445 1291 1 ND	0603
20	30	0.022/10	\$0.50	C	0.111	010000001111013	Digikey	445-1261-1-ND	0603
27	20	0.053/10	\$1.00	С	50p	GRM1885C1H510JA01D	Digikey	490-1420-1-ND	0603
28	10	0.27/10	\$3.00	R	1 OHM 1210		Digikey	P1.0VCT-ND	0003
29	10	0 27/10	\$3.00	R	3 3 -1210		Digikev	P3 3VCT-ND	0603
27	10	0.27710	<i>\$</i> 3.00	Ň	0.0 1210		Digitey		0603
30	10	0.27/10	\$3.00	R	7.5-1210		Digikey	P7.5VCT-ND	0602
31	10	0.14/10	\$2.00	R	1k 0805 0.25W		Digikey	RHM1.0KKCT-ND	0003

Bill of Materials for Gate Drive and Protection Circuitry

						_			0603
32	10	0.041/10	\$0.50	R	3k 0805		Digikey	RHM3.00KCCT-ND	0603
33	10	0.312/10	\$3.00	R	0.1		Digikey	P.10AHCT-ND	0000
34	20	0.025/10	\$0.50	R	10		Digikey	RMCF1/1610FRCT-ND	0603
54	20	0.023710	ψ0.50	IX.	10		Digitey	RMCF1/1624.9FRCT-	0603
35	40	0.025/10	\$1.00	R	24.9		Digikey	ND	0603
36	20	0.025/10	\$0.50	R	33		Digikey	RMCF1/1633FRCT-ND	
27	40	0.025/10	\$1.00	D	40.0		Digikov	RMCF1/1649.9FRCT-	0603
37	40	0.023/10	\$1.00	ĸ	47.7		Digikey	ND	0603
38	20	0.025/10	\$0.50	R	75		Digikey	RMCF1/1675FRCT-ND	0603
39	20	0.025/10	\$0.50	R	499		Digikey	RMCF1/16499FRC1- ND	0003
40	20	0.025/10	¢0 E0	D	750		Digilkov	RMCF1/16750FRCT-	0603
40	20	0.025/10	\$0.50	ĸ	750		Digikey	ND	0603
41	40	0.025/10	\$1.00	R	1k		Digikey	RMCF1/161KFRCT-ND	0(02
42	20	0.025/10	\$0.50	R	2.2k 1/10W		Digikey	RMCF1/162.2KFRCT- ND	0603
							<u> </u>	RMCF1/163.01KFRCT-	0603
43	20	0.025/10	\$0.50	R	3.01k		Digikey	ND PMCE1/163 32KEPCT	0603
44	10	0.025/10	\$0.50	R	3.32k		Digikey	ND	
45	10	0.025/10	\$0.50	R	4.75k		Digikey	RMCF1/164.75KFRCT- ND	0603
								RMCF1/164.99KFRCT-	0603
46	40	0.025/10	\$1.00	R	4.99k		Digikey	ND	0603
47	40	0.025/10	\$1.00	R	10k		Digikey	ND	
48	10	0.067/10	\$0.50	R	15k		Diaikev	311-15.0KHRCT-ND	0603
10	10	01007710	\$0100		1011		Digitoy	RMCF1/1633.2KFRCT-	0603
49	20	0.025/10	\$0.50	R	33k		Digikey	ND	0603
50	10	0.025/10	\$0.50	R	47.5k		Digikey	ND	
51	30	0.025/10	\$0.50	R	19 9k		Digikey	RMCF1/1649.9KFRCT-	0603
01	00	0.020710	<i>\</i> 0.00	IX.	17.78		Digitoy	RMCF1/1682.5KFRCT-	0603
52	20	0.025/10	\$0.50	R	82.5k		Digikey	ND	0603
53	30	0.025/10	\$0.50	R	100k		Digikey	ND	
54	10	0.025/10	\$0.50	R	150k		Digikey	RMCF1/16150KFRCT-	0603
54	10	0.023/10	ψ 0 .50	K	1300		Digitey	RMCF1/1620KFRCT-	0603
55	20	0.025/10	\$0.50	R	20.0k		Digikey	ND	0603
56	10	0.025/10	\$0.50	R	27.4k		Digikey	RMCF1/1627.4KFRC1- ND	0003
57	20	0.025/10	¢0 E0	D	// Fk		Digilkov	RMCF1/1666.5KFRCT-	0603
5/	20	0.025/10	Φ U.5U	к	Varactor SUR		ыдікеу		
58	4	0.5/1	\$2.00	R	ABSORBER 10MM 620V 2500A ZNR	ERZ-V10D621	Digikey	P7258-ND	10mmAx
59	4	0.5/1	\$2.00	R	SUR ABSORBER	FR7-V10D751	Digikey	P7260-ND	10mmAv
		0.0/1	\$2.00		SUR ABSORBER		Diati	D7212 ND	10
60	4	0.5/1	\$2.00	к	SUR ABSORBER	<u>ΕΚΖ-ΥΙΟΟ82Ι</u>	ыдікеу	r/212-NU	TUMMAX
61	4	0.61/1	\$2.00	R	10MM 1KV SUR ABSORB 10MM	ERZ-V10D102	Digikey	P7261-ND	10mmAx
62	3	1.33/1	\$4.00	R	1800V	ERZ-V10D182	Digikey	P7215-ND	10mmAx

63	20	0.212/10	\$5.00	TERMINAL DBL TURRET .109"L BRASS		Digikey	1502-2K-ND	NA
				IGBT W/DIODE				TO-
64	10	4.1/10	\$41.00	1200V 12A TO220AB	IRGB5B120KDPBF	Digikey	IRGB5B120KDPBF-ND	220AB
				SOLDER PASTE NO-				
65	1	12.75/1	\$13.00	CLEAN 63/37 5CC	SMD291AX	Digikey	SMD291AX-ND	NA
				HEATSINK TO-220				
66	2	1.88/1	\$4.00	POWER W/PINS BK	530002B02500G	Digikey	HS380-ND	NA