Analysis and design for interleaved ZCS buck DC–DC converter with low switching losses

Article *in* International Journal of Power Electronics · January 2017

DOI: 10.1504/IJPELEC.2017.10005253

3 authors:

Emad H. El-Zohri
Sohag University
27 PUBLICATIONS **92** CITATIONS
SEE PROFILE

Hedra Mahfouz
Sohag University
7 PUBLICATIONS **23** CITATIONS
SEE PROFILE

Khairy Sayed
Sohag University Faculty of Engineering
104 PUBLICATIONS **519** CITATIONS
SEE PROFILE

Analysis and design for interleaved ZCS buck DC-DC converter with low switching losses

Khairy Sayed

Department of Electrical Engineering,
Faculty of Engineering, Sohag University,
Sohag, Egypt
Email: khairy_fathy@yahoo.ca

Emad H. El-Zohri and Hedra Mahfouz*

Department of Electrical Engineering,
Faculty of Industrial Education,
Sohag University,
Sohag, Egypt
Email: emad.elzohri@yahoo.com
Email: hedra_saleeeeb@yahoo.com
*Corresponding author

Abstract: This paper presents an interleaved buck DC-DC converter using zero current switching (ZCS) resonant with additional inductor and capacitor that mainly used for battery charging applications. The proposed novel converter has advantages of its simplicity, low cost, high efficiency and behaviour of easy control under the (ZCS) condition so that reducing the switching losses. Therefore, the proposed converter offers lower switching losses with a higher power density. The performance of the converter system is improved using coupled inductors. These coupled inductors reduce the magnetic size and also improve the converter's transient performance without increasing the steady-state current ripple. The detailed study of operating principle and design considerations is presented. The effectiveness of the proposed control scheme is demonstrated through PSIM simulations. Calculated efficiency of the converter is ensured about 94%, which is substantially considered to be a satisfactory performance.

Keywords: coupled inductors; interleaved buck DC-DC converter; soft switching; zero current switching.

Reference to this paper should be made as follows: Sayed, K., El-Zohri, E. H. and Mahfouz, H. (2017) 'Analysis and design for interleaved ZCS buck DC-DC converter with low switching losses', *Int. J. Power Electronics*, Vol. 8, No. 3, pp.210–231.

Biographical notes: Khairy Sayed received his B.S. degree in electrical power and machines from the Assiut University, Assiut, Egypt, in 1997; his Master's degree from the Electrical Energy Saving Research Center, Graduate School of Electrical Engineering, Kyungnam University, Masan, Korea, in 2007 and his Ph.D. degree from the Assiut University, in 2013. He is working as an assistant professor in the Department of Electrical Engineering, Sohag University, Egypt. He is a member of IEEE. His research interests include soft switching DC-DC power converter topologies, high-frequency inverter applications, renewable energy related power conditioners and control schemes.

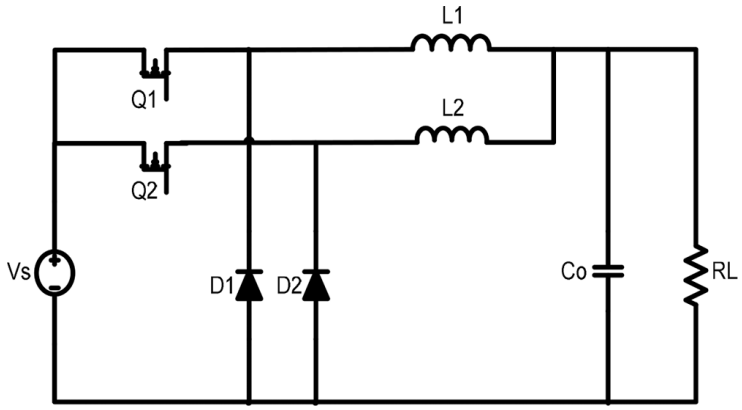
Emad H. El-Zohri received his B.S. degree in electrical power and machines in 1999, his Master's degree in 2003 and his Ph.D. degree in 2012, from the Assiut University, Assiut, Egypt. He is working as an assistant professor in the electrical department at the Faculty of Industrial Education, Sohag University, Egypt. His research interests include soft switching DC-DC power converter topologies, high-frequency inverter applications, renewable energy-related power conditioners and control schemes.

Hedra Mahfouz received his B.S. degree in electrical power and machines in 2010 and his Master's degree in power electronics in 2015 from the Sohag University, Sohag, Egypt. He is working as an assistant lecturer in the electrical department at the Faculty of Industrial Education, Sohag University, Sohag, Egypt. His research interests include power quality, power converters, energy storage devices and their applications to the power system.

1 Introduction

The buck converters were widely used in many DC power sources for microprocessor units, battery chargers and LED drivers and their derivatives (Sugumar et al., 2013). The interleaved buck converter has received a lot of attention due to its simple structure and low control complexity. Therefore, this converter is used in applications in which non-isolation, step-down conversion ratio and high output current with low ripple are required (Wong et al., 2001; Garcia et al., 2006; Lee et al., 2008; Selvaganesan et al., 2008; Lin et al., 2009; Laird et al., 2010; Chuang, 2010; Moo et al., 2011; Markakis et al., 2014). A basic buck converter converts a DC voltage to a step-down DC voltage. Interleaving technique leads to additional benefits such as reduced ripple currents in both the input and output circuits. Higher efficiency is realised by splitting the output current into two paths, substantially reducing losses and inductor AC losses. In the field of power electronics, application of interleaving technique can be traced back to very early days, especially in high power applications. The voltage and current stress can easily go beyond the range that one power device can handle. Multiple power devices connected in parallel and/or series could be one solution. However, voltage sharing and/or current sharing are still the concerns. Instead of paralleling power devices, paralleling power converters is another solution which could be more beneficial. These benefits include harmonic cancellation, better efficiency, better thermal performance and high power density (Lakshmi et al., 2014). Figure 1 shows the conventional interleaved buck converter in which all semiconductor devices suffer from the input voltage, and hence, high-voltage devices rated above the input voltage should be used. High-voltage rated devices have generally poor characteristics such as high cost, high on resistance, high forward voltage drop and severe reverse recovery. In addition, the converter operates under hard switching condition. For higher power density and better dynamics, it is required that the converter operates at higher switching frequencies (Du et al., 2009). However, higher switching frequencies increase the switching losses associated with turn-on, turn-off and reverse recovery. Consequently, the efficiency is further deteriorated. Also, it experiences an extremely short duty cycle in the case of high-input and low-output voltage applications.

Figure 1 Hard switching of the conventional interleaved buck converter



To overcome the aforementioned drawbacks of the interleaved buck converter, three-level buck converters are introduced (Jin and Ruan, 2007; Rodrigues et al., 2009; Ruan et al., 2008). The voltage stress is half of the input voltage in the converters. However, so many components are required for the use of interleaved buck converter. The interleaved buck converter with zero current transition (ZCT) is introduced to reduce diode reverse recovery losses in Ilic and Maksimovic (2007). The ZCT is implemented by only adding an inductor into the interleaved buck converter. However, in spite of these advantages, the converter suffers from high current stress, because the output current flows through each module in a complementary way. And it still has the drawbacks of the interleaved buck converter. The interleaved buck converter with a single capacitor turn-off snubber is demonstrated in Chen et al. (2004). Its advantages are that the switching loss associated with turn-off transition can be reduced, and single coupled inductor implements the converter as two output inductors. However, because it operates in discontinuous conduction mode (DCM), all elements suffer from high current stress, resulting in high conduction and core losses. In addition, the voltages across all semiconductor devices are still the input voltage. The interleaved buck converter with active clamp circuit is presented in Tsai and Shen (2009). In this converter, all active switches are turned ON with zero voltage switching (ZVS). In addition, a high step-down conversion ratio can be obtained, and the voltage stress across the freewheeling diodes can be reduced. However, to obtain the mentioned advantages, it requires additional active switches and passive elements, which increases the cost significantly at low or middle levels of power applications.

The Pulse Width Modulation (PWM) control is used in the converter circuits to get the desired shape of the output voltage or current. By using this technique, the following disadvantages occur:

1 The devices are turned on and off at the load current with a high di/dt value.

2 The switches are subjected to a high voltage stress.

3 The switching power loss also increases with the switching frequency.

4 The turn-on and turn-off losses could be a significant portion of the total power loss.

5 The electromagnetic interference is also produced due to high *di*/*dt* and *du*/*dt* in the converter waveforms.

The above disadvantages can be eliminated (or) minimised if the devices are turned 'ON' and 'OFF' using soft switching technique. These are zero current switching (ZCS). This paper aims to propose a novel interleaved buck DC-DC converterto save energy and losses as found in the form of heat and also to achieve high efficiency.

2 Circuit configuration of ZCS buck converter

2.1 Circuit configuration

The proposed interleaved buck DC-DC converter with (ZCS) resonant converter shown in Figure 2 is suitable for low-voltage and high-current applications. It is similar to the conventional interleaved buck converter, but two active switches are connected in parallel and coupled inductors. The buck (ZCS) resonant converters are used for resolving the high switching frequency losses, reducing the circuit volume and controlling the switches with ease. Therefore, they control the output voltage via switching frequency with duty ratio *K* which will be 50%. The switches of ZCS resonant converters turn ON and OFF at zero current due to the current produced by resonant inductor L_r and the resonant capacitor C_r that the resonance flows across the switch. The resonant circuit holds a switch S, resonant components inductor L_r and capacitor C_r. Figure 3 shows the circuit structure of a ZCS resonant converter.

Figure 2 Soft switching of the proposed interleaved buck converter using ZCS

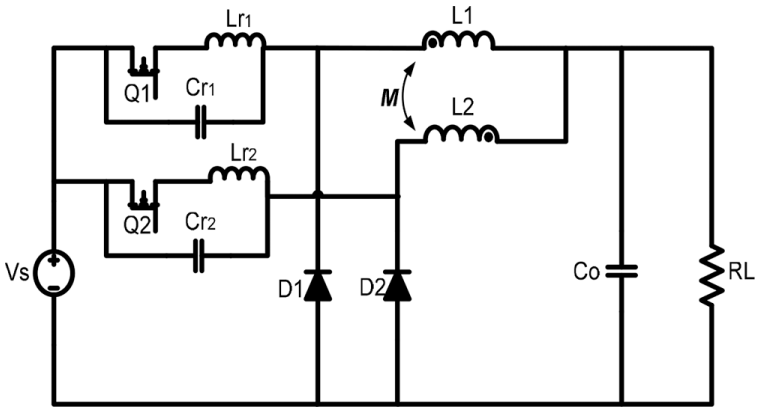
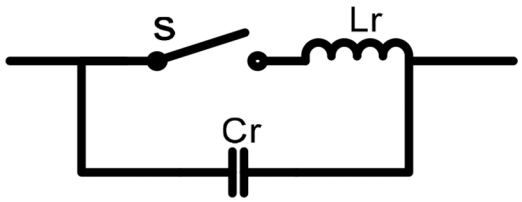


Figure 3 ZCS resonant converter



2.2 Steady state analysis of proposed work

Under continuous inductor current operation, eight major operating intervals are identified over one switching cycle. Figure 4 shows simulated voltage and current waveforms of its key components. The operating equivalent circuits of the proposed interleaved buck converter when $K \leq 0.5$ shown in Figure 5.

Figure 4 Relevant voltage and current waveforms of the proposed interleaved buck converter using ZCS (see online version for colours)

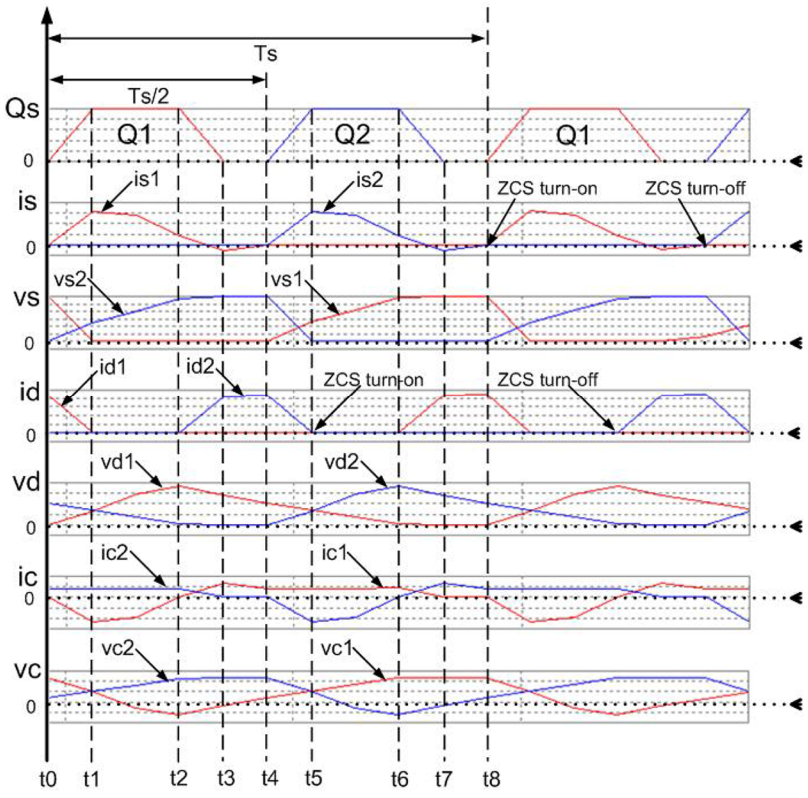
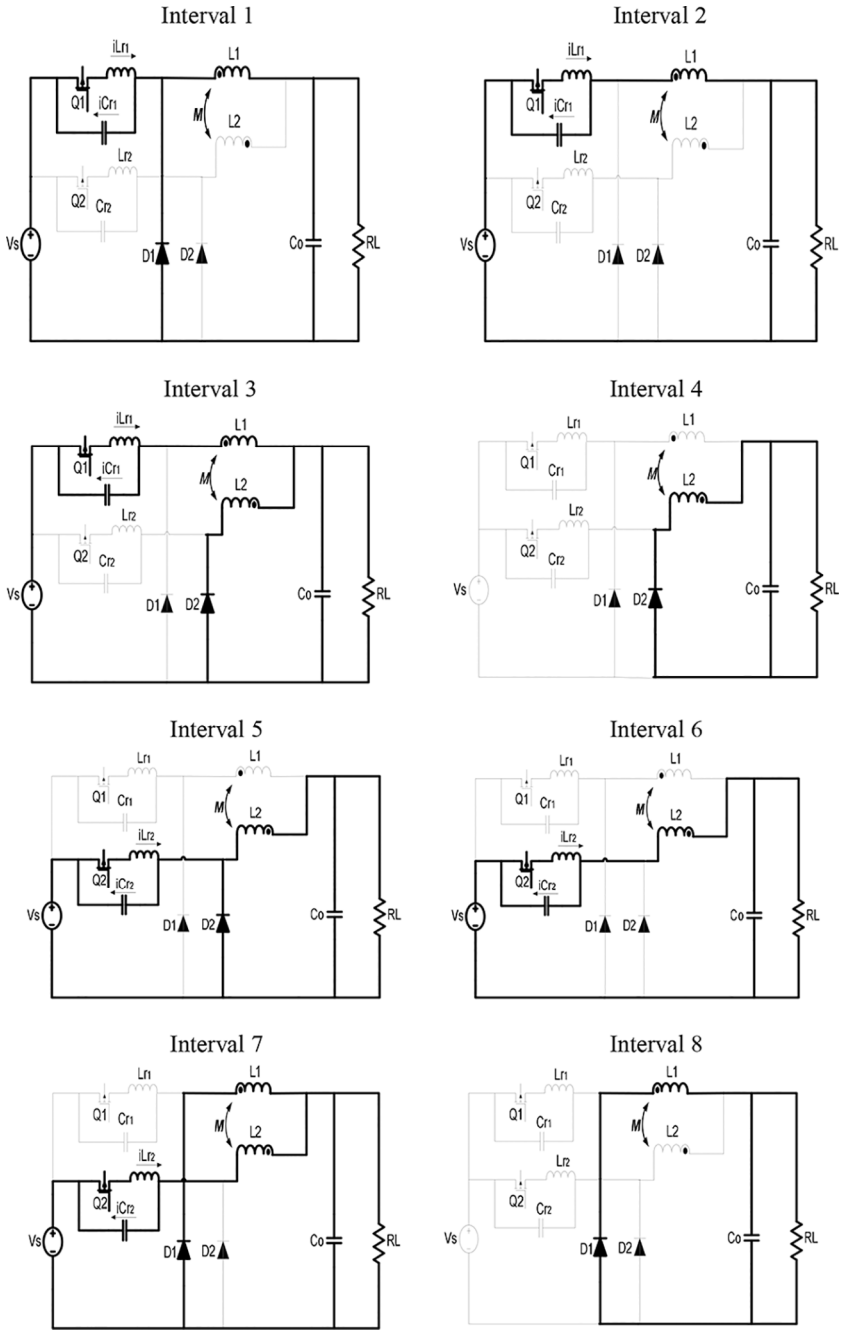


Figure 5 Operating circuits of the proposed interleaved buck converter when $K \leq 0.5$



Interval 1 ($t_0 \le t \le t_1$) begins when Q_1 is turned ON at t_0. Then, the current resonant inductor of Lr_1, $iLr_1(t)$, flows through Q_1, Cr_1 and L_1 to the load. Hence, $iLr_1(t)$ increases linearly from the initial value. At the same time, D_2 is turned OFF. Hence, the current of L_1, $iL_1(t)$ flows through D_1.

Interval 2 ($t_1 \le t \le t_2$) begins when Q_1 is turned ON at t_1. Then, the current resonant inductor of Lr_1, $iLr_1(t)$, flows through Q_1, Cr_1 and L_1 to the load. Hence, $iLr_1(t)$ increases linearly from the initial value. At the same time, D_1 and D_2 are turned OFF. Hence, the current of L_1, $iL_1(t)$, flows through the load.

Interval 3 ($t_2 \le t \le t_3$) begins when Q_1 is turned ON at t_2. Then, the current resonant inductor of Lr_1, $iLr_1(t)$, flows through Q_1, Cr_1 and L_1, to the load. Hence, $iLr_1(t)$ decrease linearly. At the same time, D_1 is turned OFF. Hence, the current of L_1 and L_2, $iL_1(t)$ and $iL_2(t)$, flows through D_2.

Interval 4 ($t_3 \le t \le t_4$) begins when Q_1 is turned OFF at t_3. Then, the current of L_2, $iL_2(t)$ flows through D_2. Hence, the current of L_2, $iL_2(t)$ decrease linearly, during this interval.

Interval 5 ($t_4 \le t \le t_5$) begins when Q_2 is turned ON at t_4. Then, the current resonant inductor of Lr_2, $iLr_2(t)$, flows through Q_2, Cr_2 and L_2, to the load. Hence, $iLr_2(t)$ increases linearly from the initial value. At the same time, D_1 is turned OFF. Hence, the current of L_1, $iL_1(t)$, flows through D_2.

Interval 6 ($t_5 \le t \le t_6$) begins when Q_2 is turned ON at t_5. Then, the current resonant inductor of Lr_2, $iLr_2(t)$ flows through Q_2, Cr_2 and L_2, to the load. Hence, $iLr_2(t)$ increases linearly from the initial value. At the same time, D_1 and D_2 are turned OFF. Hence, the current of L_2, $iL_2(t)$, flows through the load.

Interval 7 ($t_6 \le t \le t_7$) begins when Q_2 is turned ON at t_6. Then, the current resonant inductor of Lr_2, $iLr_2(t)$ flows through Q_2, Cr_2 and L_2, to the load. Hence, $iLr_2(t)$ decrease linearly. At the same time, D_2 is turned OFF. Hence, the current of L_1 and L_2, $iL_1(t)$ and $iL_2(t)$, flows through D_1.

Interval 8 ($t_7 \le t \le t_8$) begins when Q_2 is turned OFF at t_7. Then, the current of L_1, $iL_1(t)$ flows through D_1. Hence, the current of L_1, $iL_1(t)$ decrease linearly, during this interval.

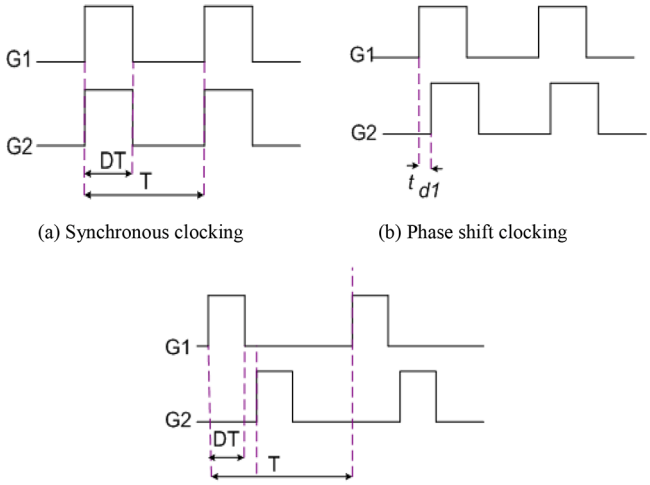
The steady-state operation of the proposed interleaved buck converter has been described in detail. Consequently, it can be known that the proposed interleaved buck converter has advantages in terms of efficiency and component stress in the case of $K \le 0.5$ only. Because of switches, Q_1 and Q_2 experience high current stress in the case of $K > 0.5$ in Lee et al. (2012). Thus, the proposed interleaved buck converter is recommended for the applications where the operating duty cycle is smaller than or equal to 0.5.

2.3 Gate pulse pattern

The gate pulse pattern for main switches Q_1 and Q_2 are shown schematically in Figure 6. The operation of an N-cell parallel converter system is considered. If all of the cells are clocked synchronously, as illustrated in Figure 6a for a two-cell system; then the system behaves exactly as a single large converter. However, it can be shown that if the cells are clocked independently (and hence operate at slightly different frequencies) as shown in Figure 6b, the RMS input and output current ripples will be reduced by a factor of due to the passive ripple cancellation that occurs among cells. The active method of interleaving

illustrated in Figure 6c is well known. Interleaving N parallel (or series) connected converter cells requires that the cells are operated at the same switching frequency but phase displaced with respect to one another by $2\pi/N$ radians.

Figure 6 Gate pulse pattern. (a) Synchronous clocking. (b) Phase shift clocking. (c) Interleaved clocking (see online version for colours)



(a) Synchronous clocking (b) Phase shift clocking

(c) Interleaved clocking

In the interleaving technique, cells are operated at the same switching frequency with their switching waveforms displaced in phase over a switching period. The benefits of this technique are due to harmonic cancellation among the cells and include low ripple amplitude and high ripple frequency in the aggregate input and output waveforms.

3 Design considerations of key components

This section details how the main components in the proposed topology were chosen. Important factors when choosing components were size, cost and impact on the efficiency of the circuit. All components were chosen to be surface mount to reduce the size and hence improve power density from the previous design.

3.1 Design of the coupled inductors

To find the value of the coupled inductors, we will use

$$V_L = L \times \frac{di}{dt} \tag{1}$$

For high switching frequency operation

$$V_L = L \times \frac{\Delta i}{\Delta t} \tag{2}$$

$$L = V_L \times \frac{\Delta t}{\Delta i} \tag{3}$$

There are two states of a buck converter. The first state occurs when the switch is on (closed), and the second stage occurs when the switch is off (open). Choosing the switch to be on, we can write the equation as

$$L = V_{L\text{-on}} \times \frac{t_{\text{on}}}{\Delta i} \tag{4}$$

When the switch is on, the voltage source is connected to the positive end of the inductor. The negative end of the inductor is connected to the output voltage. Therefore, assuming an ideal switch, the voltage across the inductor when the switch is on is equal to

$$V_{L\text{-on}} = V_I - V_O = 12 - 6 = 6 \text{ V} \tag{5}$$

The time the switch is on is equal to

$$T_{\text{on}} = KT \tag{6}$$

The period, T_s, is equal to the inverse of the switching frequency, which is given by the design requirement to be 100 kHz. Therefore, the period is equal to 10 μs. Based on volt-second balance concept, the average of the voltage across an inductor is equal to zero. Therefore, we can use the volt-second balance to find the duty cycle, K. The equation for volt-second balance is

$$V_{L\text{-on}} \times KT + V_{L\text{-off}} \times (1-K)T = 0 \tag{7}$$

The period will be dropped from this equation. To find the duty cycle

$$(V_I - V_O)K + (-V_O)(1-K) = 0 \tag{8}$$

$$K = \frac{V_o}{V_i} = \frac{6}{12} = 0.5 \tag{9}$$

The inductor is chosen to have a ripple of 0.1 A, which is 10% of the desired average current through the inductor. Plugging all the values in, the value of the inductor is equal to

$$V_{L\text{-on}} \times \frac{t_{\text{on}}}{\Delta i} = (V_I - V_O) \times \frac{KT}{\Delta i} = (12-6) \times \frac{0.5 \times 10 \times 10^{-6}}{0.1} = 300 \text{ μH} \tag{10}$$

3.2 Design of the output capacitor

To find the output capacitor, C_O, we will use the charge equation:

$$Q = CV \tag{11}$$

The average of the charge, Q, is equal to zero. Therefore, the charge when the switch is on is used to find the capacitor value. The voltage across the capacitor while the switch is on is equal to the output voltage ripple

$$C = \frac{Q_{\text{on}}}{\Delta V_o} \tag{12}$$

Therefore, the charge while one of the switches is ON is equal to

$$Q_{\text{on}} = \left[\frac{1}{2}\right]\left[\frac{T}{2}\right]\left[\frac{\Delta i}{2}\right] = \left[\frac{1}{2}\right]\left[\frac{2.5\times10^{-6}}{2}\right]\left[\frac{0.1}{2}\right] = 31.25 \text{ nC} \tag{13}$$

Therefore, the output capacitor value is equal to

$$C_o = \frac{Q_{\text{on}}}{\Delta V_o} = \frac{31.25\times10^{-9}}{0.05} = 0.625 \text{ μF} \tag{14}$$

as output voltage ripple ΔV_o < 50 mV.

3.3 Design of ZCS buck converter

The equivalent output impedance can be determined from the output voltage V_O and the output current I_O given as

$$R_o = \frac{V_o}{I_o} = \frac{6}{2} = 3\ \Omega \tag{15}$$

The characteristic impedance is computed as given

$$R_o = 3\ \Omega \text{ and } Q = 1 \text{ into } Z_o = \frac{R_o}{Q} = \frac{3}{1} = 3\ \Omega \tag{16}$$

The resonant frequency is calculated from switching frequency f_s, and normalised switching frequency f_{ns} = 0.5 was set based on the normalised voltage gain

$$f_o = \frac{f_s}{f_{ns}} = \frac{100 \text{ kHz}}{0.5} = 200 \text{ kHz} \tag{17}$$

The LC-resonant pair will be derived for which fatherly computing the LC-filter pairs of novel design parameters. The resonant inductor L_r *is* given by

$$L_r = \frac{Z_o}{\omega_o} = \frac{Z_o}{2\pi f_o} = \frac{3}{2\pi\times200\times10^3} = 2.4 \text{ μH} \tag{18}$$

The resonant capacitance C_r is given by

$$C_r = \frac{1}{\omega_o Z_o} = \frac{1}{2\pi\times200\times10^3\times3} = 0.265 \text{ μF} \tag{19}$$

3.4 Selection of power switches and diodes

The MOSFETs are *N*-type MOSFETs. When the selection of switching devices M_1 and M_2 MOSFETs, we must ensure that the MOSFETs can handle the 100-kHz switching frequency. Also, the MOSFETs must be able to handle the peak current of 7 A, which is the same as the phase inductors. By meeting these two parameters, the proposed topology

should work. To meet the 90% efficiency specification, more care must be taken in selecting the MOSFETs. The maximum voltage stresses imposed on both active switches M_1 and M_2 are

$$V_{\mathrm{DS\,(max)}} = V_I + V_O = 12 + 6 = 18 \text{ V} \tag{20}$$

When active switch M_1 or M_2 is turned ON, the maximum switch current $I_{\mathrm{DS\,(max)}}$ can be given as

$$I_{\mathrm{DS\,(max)}} \approx \frac{I_o}{4} + \frac{(V_i - V_o)K}{n^2 Lr\, Fo} = \frac{2}{4} + \frac{(12-6)0.5}{1^2 \times 2.4\times 10^{-6} \times 200 \times 10^3} = 6.75 \text{ A} \tag{21}$$

And both free-wheeling diodes D_1 and D_2 are

$$V_{D(\max)} = V_I = 12 \text{ V} \tag{22}$$

When free-wheeling diode D_1 or D_2 is conducting, the maximum diode current $I_{\mathrm{DS\ (max)}}$ can be given as

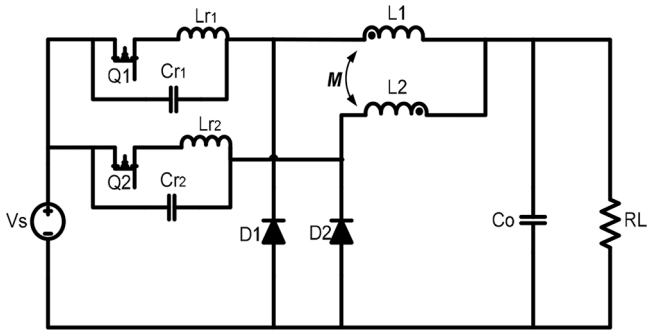
$$I_{D(\max)} \approx \frac{(V_i - V_o)K}{n\, Lr\, Fo} = \frac{(12-6)0.5}{2.4\times 10^{-6} \times 200 \times 10^3} = 6.25 \text{ A} \tag{23}$$

Selection of switching devices M_1 and M_2 involves a trade-off between conduction losses and switching losses. The selection of MOSFETs with low $R_{\mathrm{ds\text{-}on}}$ will reduce conduction loss, but it will result in high parasitic capacitance. Switches with lower $R_{\mathrm{ds\text{-}on}}$ also imply larger die size and higher cost. For this application, we can select the proper MOSFETs as the IRF540 which provide high enough safety margins with a drain-source breakdown voltage of 50 V. Several important parameters of the IRF540 are listed as follows: The on resistance is $R_{\mathrm{ds\text{-}on}} = 77$ mΩ, The total gate charge is $Q_{\mathrm{sw}} = 65$ nC.

4 Power loss calculations and efficiency

The following power losses of the proposed converter topology at full load for worst case scenario are estimated to verify the measured efficiency. The key component values of the experimental converter are shown in Figure 7, from which power losses are evaluated as follows.

Figure 7 Experimental circuit of the proposed interleaved buck converter using ZCS



4.1 Parameters

This section shows the entire given, component and calculated parameters in Tables 1–3, respectively. The component parameters come from the typical values listed in the component data sheets. Next, some calculated parameters will be shown, where K is the duty cycle, T_s is the switching period, I_{buck} is the average current through each phase and ΔI_{buck} is the current ripple through each phase.

Table 1 Given parameters

Item	*Symbol*	*Value*
DC input voltage	V_{in}	12 V
DC output voltage	V_{out}	6 V
Output current	I_o	2 A
Coupled inductors	L	300 μH
Output capacitor	C_o	0.625 μF
Switching frequency	f_s	100 kHz

Table 2 Component parameters

Item	*Symbol*	*Value*
Buck coupled inductors	DCR_{coup}	76 mΩ
Output capacitor	ESR_{out}	250 mΩ
Main switch	$R_{\text{ds-on}}$	77 mΩ
Main switch Qg	Q_{sw}	65 nC
Main switch rise time	$T_{r\text{-Time}}$	39 nS
Main switch fall time	$T_{f\text{-Time}}$	24 nS
Schottky diode forward voltage drop	V_f	0.3 V

Table 3 Calculated parameters

$$K = \frac{V_o}{V_i} = \frac{6}{12} = 0.5$$

$$T_s = \frac{1}{fs} = \frac{1}{100 \times 10^3} = 10\ \mu\text{s}$$

$$I_{\text{buck}} = \frac{I_o}{2} = \frac{2}{2} = 1\ \text{A}$$

$$\Delta I_{\text{buck}} = 10\% \times I_{\text{buck}} = 0.1 \times 1 = 0.1\ \text{A}$$

$$\Delta I_o = 10\% \times I_o = 0.1 \times 2 = 0.2\ \text{A}$$

4.2 Coupled inductors (L_1 and L_2) losses

The calculation assumes that core losses are negligible, and thus, only copper loss is taken into consideration. According to measurement, the winding resistance of the coupled inductors is $R_{\text{Coup}} = 76\ \text{m}\Omega$ and the copper losses can be estimated as

$$P_{\text{copper}} = \left[\frac{Io}{2}\right]^2 \times R_{\text{Coup}} = \left[\frac{2}{2}\right]^2 \times 76\times10^{-3} = 0.076\ \text{W} \tag{24}$$

Total power loss of the coupled inductors is therefore

$$P_{\text{total}} = 2\times P_{\text{copper}} = 2\times0.076 = 0.152\ \text{W} \tag{25}$$

4.3 Output capacitor losses

The power losses from the output capacitors are calculated

$$P_{\text{capa}} = \Delta I_o{}^2 \times \text{ESR}_{\text{out}} = (0.2)^2 \times 250\times10^{-3} = 0.01\ \text{W} \tag{26}$$

4.4 MOSFETs (M_1 and M_2) losses

The power loss in the MOSFET comes from conduction, gate charge and switching losses as

$$I_{\text{rms}} = I_{\text{buck}} \times \sqrt{K\times\left[1+\frac{(\Delta I_{\text{buck}})^2}{12\times(I_{\text{buck}})^2}\right]} = 1\times\sqrt{0.5\times\left[1+\frac{(0.1)^2}{12\times(1)^2}\right]} = 0.7074\ \text{A} \tag{27}$$

- *Conduction loss*

$$P_{\text{cond}} = I_{\text{rms}}{}^2 \times R_{\text{ds-on}} = (0.7074)^2 \times 77\times10^{-3} = 0.0385\ \text{W} \tag{28}$$

- *Switching loss*

$$\begin{aligned} P_{\text{Swit}} &= 0.5\times I_{\text{buck}} \times V_{\text{IN}} \times (T_{r-\text{time}} + T_{f-\text{time}}) \times f_s \\ &= 0.5\times1\times12\times\left(39\times10^{-9} + 24\times10^{-9}\right)\times100\times10^3 = 0.0378\ \text{W} \end{aligned} \tag{29}$$

- *Gate charge loss*

$$P_{\text{gate}} = Q_{\text{sw}} \times V_{\text{IN}} \times f_s = 65\times10^{-9}\times12\times100\times10^3 = 0.078\ \text{W} \tag{30}$$

Total power loss of the MOSFETs is therefore

$$P_{\text{total}} = 2\times(P_{\text{cond}} + P_{\text{Swit}} + P_{\text{off}}) = 2\times(0.0385 + 0.0378 + 0.078) = 0.309\ \text{W} \tag{31}$$

4.5 Free-wheeling diodes (D_1 and D_2) losses

Thus, the conduction loss of the free-wheeling diode can be determined as

$$P_{\text{diode}} = \frac{I_o}{2} \times V_F \times (1-K) = \frac{2}{2}\times0.3\times(1-0.5) = 0.15\ \text{W} \tag{32}$$

Total power loss of the Diodes is therefore

$$P_{\text{total}} = 2 \times P_{\text{diode}} = 2 \times 0.35 = 0.3 \text{ W} \tag{33}$$

4.6 Total power loss and efficiency

Finally, the total power loss and efficiency at full load can now be calculated

$$\begin{aligned} P_{\text{total}} &= P_{\text{CoupledInductors}} + P_{\text{Capacitor}} + P_{\text{Mosfet}} + P_{\text{diode}} \\ &= 0.152 + 0.01 + 0.309 + 0.3 = 0.771 \text{ W} \end{aligned} \tag{34}$$

Power losses under full load condition on the key components are summarised in Table 4. The estimated efficiency of the proposed converter with ZCS circuits at input voltage V_I =12 *Vdc*, and full-load condition is

$$P_{\text{out}} = V_O \times I_O = 6 \times 2 = 12 \text{ W} \tag{35}$$

$$\eta\% = \frac{P_{\text{out}}}{P_{\text{out}} + \text{total losses}} \times 100 = \frac{12}{12 + 0.771} \times 100 = 94\% \tag{36}$$

Table 4 Results of power losses analysis under full load and efficiency estimation of the proposed interleaved buck converter with ZCS circuits

Item		*Power loss calculation*	*Power losses*
Coupled inductor losses		$P_{\text{copper}} = 2 \times \left[\frac{I_o}{2}\right]^2 \times R_{\text{Coup}}$	0.152 W
Output capacitor losses		$P_{\text{capa}} = \Delta I_o^{\,2} \times \text{ESR}_{\text{out}}$	0.01 W
MOSFET losses	Conduction losses of Q1 and Q2	$P_{\text{cond}} = 2 \times I_{\text{rms}}^2 \times R_{\text{ds-on}}$	0.077 W
	Switching losses of Q1 and Q2	$P_{\text{Swit}} = 2 \times 0.5 \times I_{\text{buck}} \times V_{\text{in}} \times (T_{r\text{-time}} + T_{f\text{-time}}) \times f_s$	0.0756 W
	Gate charge losses of Q1 and Q2	$P_{\text{off}} = 2 \times Q_{\text{sw}} \times V_{\text{in}} \times f_s$	0.156 W
Diode losses	Conduction losses of D1 and D2	$P_{\text{diode}} = 2 \times \frac{Io}{2} \times V_F \times (1 - K)$	0.3 W
Total losses		$P_{\text{total}} = P_{\text{Coupled Inductors}} + P_{\text{Capacitor}} + P_{\text{Mosfet}} + P_{\text{diode}}$	0.771 W
Efficiency		$\eta\% = \frac{P_{\text{out}}}{P_{\text{out}} + \text{total losses}} \times 100$	94%

As shown in Eq. (36), the expected efficiency at full load is 94%.

Figures 8 and 9 show the graph for results of power loss analysis for the proposed interleaved buck converter at 100 kHz and calculated efficiency of soft switching interleaved buck converter versus hard switching, respectively.

Figure 8 Results of power loss analysis for the proposed interleaved buck converter at 100 kHz (see online version for colours)

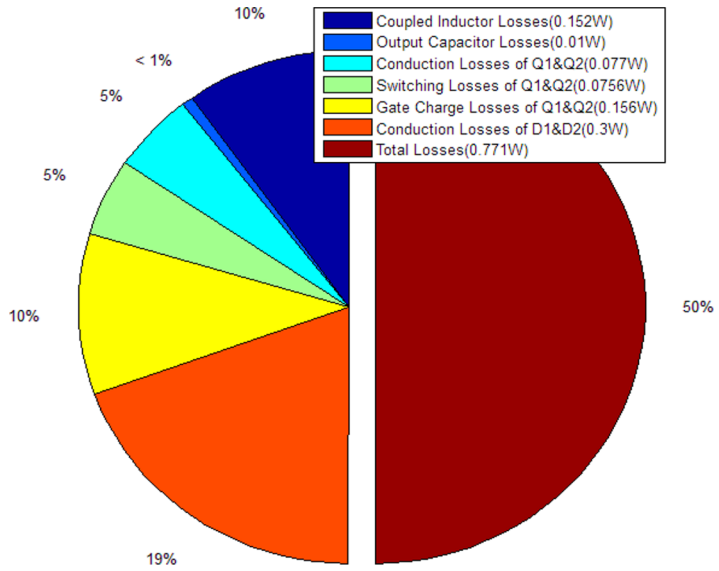
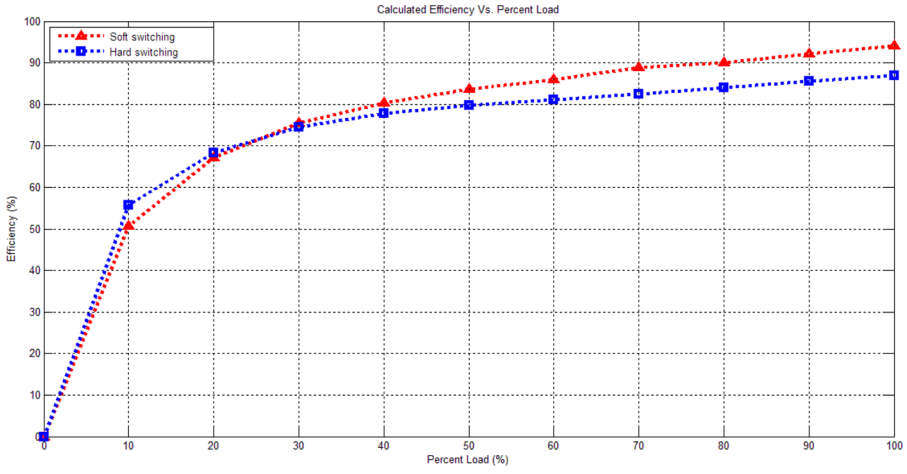


Figure 9 Efficiency of soft switching interleaved buck converter vs. hard switching (see online version for colours)

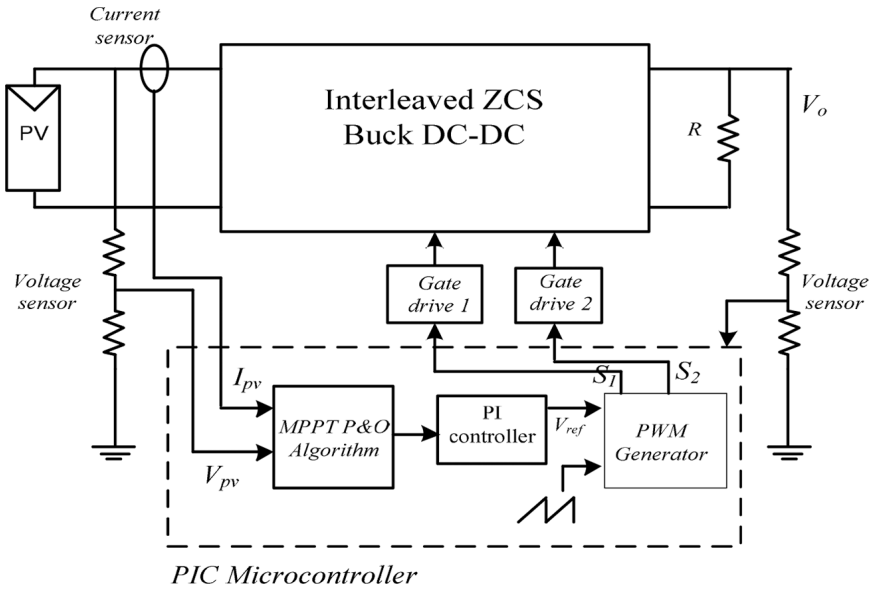


The two above figures reveal that the proposed converter can operate at higher switching frequencies without the penalty of a significant increase in the losses. Thus, it can be said that the proposed interleaved buck converter is more advantageous in terms of efficiency and power density.

5 Feedback control scheme

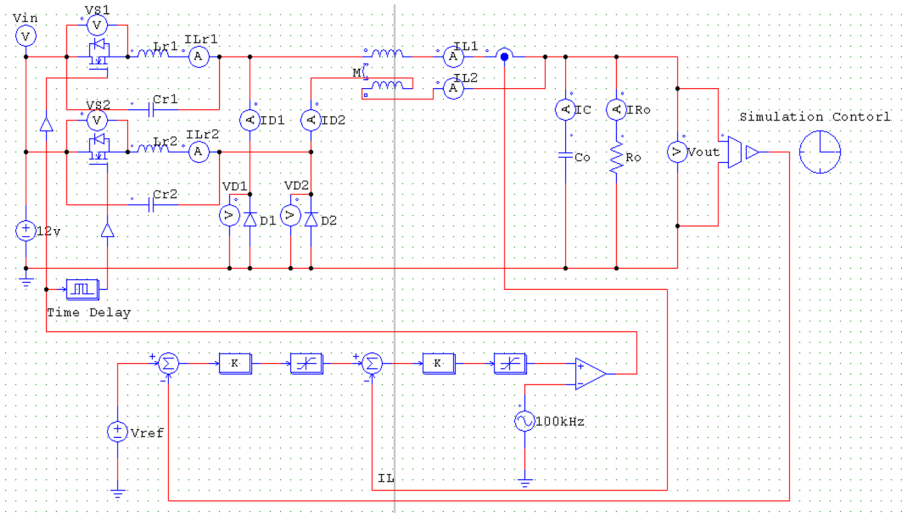
The perturb and observe (P&O) approach is used to track the Maximum Power Point Tracking (MPP and MPPT) of the array that is well suited to PIC microcontroller implementation (Sayed and Nakaoka, 2015; Sayed et al., 2012, 2014). To follow up the change of insolation level and temperature, the perturbation cycle is repeated and the algorithm continues in the same way. The Maximum Power Point Tracking (MPP and MPPT) algorithm is embedded in the logic block and produces a reference voltage to adjust the duty cycle to move the operating point on the P-V curve of the PV module. The reference voltage is compared with a sawtooth waveform using a comparator. Finally, a PWM switching signal is generated to drive the switches Q1 and Q2 of Figure 2. The output voltage is sensed to be controlled within the specified limits. The control system is given in a block diagram given in Figure 10. The adopted converter is controlled by PIC microcontroller, which is used to implement P&O MPPT algorithm.

Figure 10 Block diagram of the soft-switching buck converter



The proposed controller-based scheme is evaluated through PSIM simulations. The PSIM model which represents the system and control scheme is shown in Figure 11. The dual-loop average current mode control is a better solution. In the dual-loop structure, the outer loop is voltage loop, which provides the current reference for the inner loop. This control requires the sampling of two variables: output voltage and inductor current. Both the inner current loop and the outer voltage loop use a proportional controller as is shown in Figure 10.

Figure 11 Simulation model of a proposed circuit interleaved buck DC-DC converter using ZCS resonant (see online version for colours)



6 Simulation results

The proposed converter is simulated using PSIM software. The simulation diagram is shown in Figure 11 whereas the simulation parameters are shown in Table 5.

Table 5 Simulation parameters

Item	*Symbol*	*Value*
DC input voltage	V_{in}	12 V
DC output voltage	V_{out}	6 V
Output current	I_o	2 A
Resonant inductor	L_r	2.4 µH
Resonant capacitor	C_r	0.265 µF
Coupled inductors	L_{coup}	300 µH
Output capacitor	C_o	0.625 µF
Switching frequency	f_s	100 kHz
Resonant frequency	f_o	200 kHz
Load resistance	R_l	3 Ω

Figure 12 shows the input voltage, output voltage and current waveforms. For an input voltage of 12 V, the output voltage is 6 V at time 20 ms, and the output current is 2 A at time 20 ms. Table 6 gives the ripple of the two topologies for hard and soft switching, respectively. Table 6 shows clearly the superiority of soft switching that removes the ripple in output voltage and current.

Figure 12 The steady state and dynamic performance of hard and soft switching (see online version for colours)

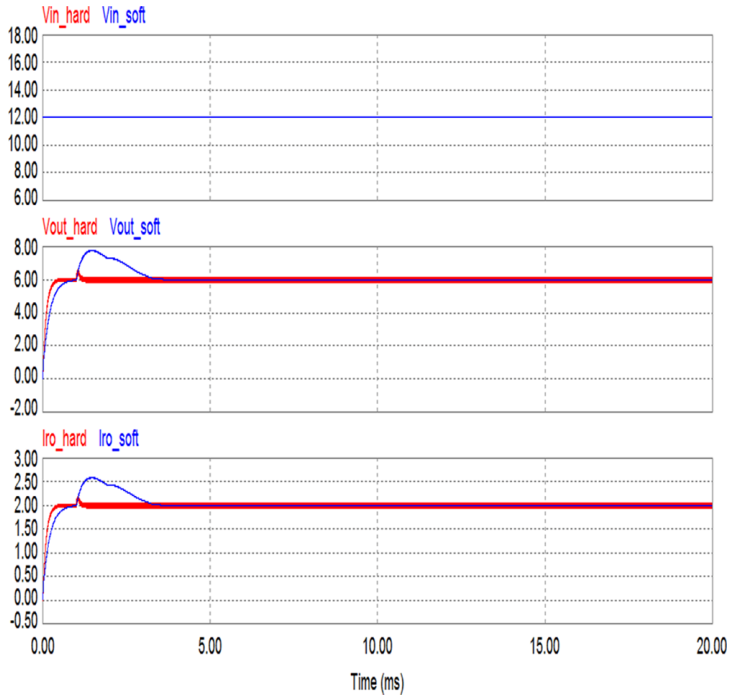


Table 6 Comparison between the two topologies

Item	*Output voltage ripple (mV)*	*Output current ripple (mA)*
Hard switching with feedback control	300	100
Soft switching with feedback control using ZCS resonant	0	0

7 Experimental results

Figure 13 shows a picture of lab setup whereas Figure 14 presents the experimental waveforms of switches signal (Q_1 or Q_2). Experimental voltage waveforms of switches (Q_1 or Q_2) are shown in Figure 15 whereas the current waveforms are given in Figure 16. Figure 17 shows the experimental output voltage. The figures show the superiority of the proposed converter in reducing the switching losses of the converter system.

Figure 13 Picture of lab setup (see online version for colours)

Figure 14 Waveforms of switches signal Q_1 or Q_2 (V_Q: 3 V/div; time: 5 µs/div) (see online version for colours)

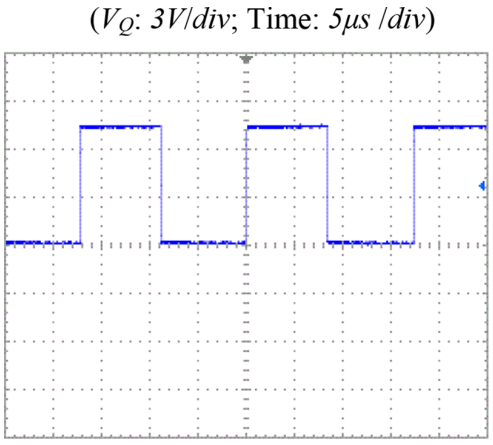


Figure 15 Voltage waveforms of switches Q_1 or Q_2 (V_Q: 3 V/div; time: 5 µs/div) (see online version for colours)

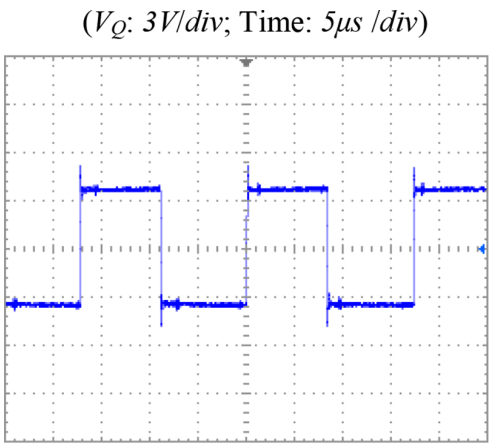


Figure 16 Current waveforms of switches Q_1 or Q_2 (i_Q: 1 A/div; time: 5 µs/div) (see online version for colours)

(i_Q: *1A/div*; Time: *5µs/div*)

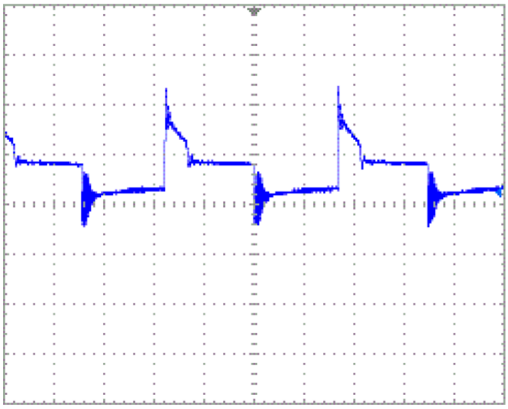
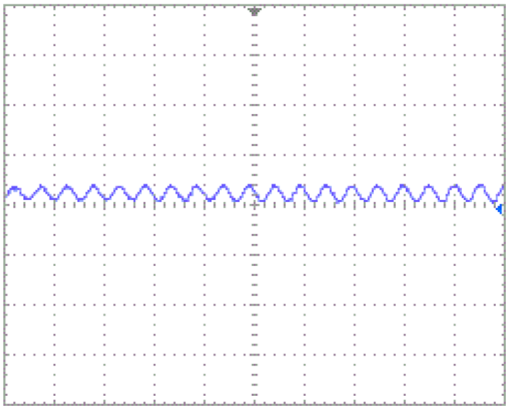


Figure 17 Waveforms of output voltage (V_O: 25 V/div; time: 100 ns/div) (see online version for colours)

(V_O: *25V/div*; Time: *100ns/div*)



8 Conclusion

This paper demonstrates the most important properties of the proposed interleaved buck DC-DC converter. The operation and different waveforms of this converter are described. The following conclusions can be drawn.

- The proposed interleaved buck DC-DC converter has a simple structure, giving high output current with low ripple, higher power density and low cost.
- Interleaved switching technique is advantageous because it will yield a smaller current ripple and higher frequency compared with non-interleaved switching.

- The use of coupled inductors could reduce the number of magnetic cores and magnetic material used, exhibits lower switch stress and lower conduction losses both in the switching device and filter capacitor on account of the smaller current ripple, and improves the converter efficiency compared with the non-coupled case. Also, using coupled inductors will reduce size and cost.
- Indirect coupling inductors were suitable for interleaved buck DC-DC converter. Increasing the coupling coefficient reduces the output current ripple which in turn reduces the inductor core losses.
- The use of interleaved clocking has the advantage of reducing the output ripple and increases the output voltage for the same circuit conditions. This enhances and improves the efficiency and performance considerably.
- The proposed converter can operate at higher switching frequencies without the penalty of a significant increase in the losses. Thus, it can be said that the proposed interleaved buck converter is more advantageous in terms of efficiency and power density.

References

Chen, Y.M., Tseng, S.Y., Tsai, C.T. and Wu, T.F. (2004) 'Interleaved buck converters with a single-capacitor turn-off snubber', *IEEE Transactions on Aerospace and Electronic Systems*, Vol. 40, No. 3, July, pp.954–967.

Chuang, Y.C. (2010) 'High-efficiency ZCS buck converter for rechargeable batteries', *IEEE Transactions on Industrial Electronics*, Vol. 57, No. 7, July, pp.2463–2472.

Du, X., Zhou, L., and Tai, H.M. (2009) 'Double-frequency buck converter', *IEEE Transactions on Industrial Electronics*, Vol. 56, No. 5, May, pp.1690–1698.

Garcia, O., Zumel, P., Castro, A.D. and Cobos, J.A. (2006) 'Automotive DC-DC bidirectional converter made with many interleaved buck stages', *IEEE Transactions on Power Electronics*, Vol. 21, No. 21, May, pp.578–586.

Ilic, M. and Maksimovic, D. (2007) 'Interleaved zero-current-transition buck converter', *IEEE Transactions on Industry Applications*, Vol. 43, No. 6, November, pp.1619–1627.

Jin, K. and Ruan, X. (2007) 'Zero-voltage-switching multi-resonant three-level converters', *IEEE Transactions on Industrial Electronics*, Vol. 54, No. 3, June, pp.1705–1715.

Laird, I., Lu, D.D-C. and Agelidis, V.G. (2010) 'Switched-coupled-inductor DC/DC converters with high voltage conversion ratio', *International Journal of Power Electronics*, Vol. 2, No. 4, January, pp.345–362.

Lakshmi, D., Zabiullah, S. and Venu Gopal, D. (2014) 'Improved stepdown conversion in interleaved buck converter and low switching losses', *International Journal of Engineering and Science*, Vol. 4, No. 3, March, pp.15–24.

Lee, J.H., Bae, H.S. and Cho, B.H. (2008) 'Resistive control for a photovoltaic battery charging system using a microcontroller', *IEEE Transactions on Industrial Electronics*, Vol. 55, No. 7, July, pp.2767–2775.

Lee, I-O., Cho, S-Y. and Moon, G-W. (2012) 'Interleaved buck converter having low switching losses and improved step-down conversion ratio', *IEEE Transactions on Power Electronics*, Vol. 27, No. 8, August, pp.3664–3675.

Lin, R.L., Hsu, C.C. and Changchien, S.K. (2009) 'Interleaved four-phase buck-based current source with an isolated energy-recovery scheme for electrical discharge machine', *IEEE Transactions on Power Electronics*, Vol. 24, No. 7, July, pp.2249–2258.

Markakis, A., Holderbaum, W. and Potter, B. (2014) 'Bond graph models of DC-DC converters operating for both CCM and DCM', *International Journal of Power Electronics*, Vol. 6, No. 1, January, pp.18–41.

Moo, C.S., Chen, Y.J., Cheng, H.L. and Hsieh, Y.C. (2011) 'Twin-buck converter with zero-voltage-transition', *IEEE Transactions on Industrial Electronics*, Vol. 58, No. 6, June, pp.2366–2371.

Rodrigues, J.P., Mussa, S.A., Heldwein, M.L. and Perin, A.J. (2009) 'Three-level ZVS active clamping PWM for the DC-DC buck converter', *IEEE Transactions on Power Electronics*, Vol. 24, No. 10, October, pp.2249–2258.

Ruan, X., Li, B., Chen, Q., Tan, S.C. and Tse, C.K. (2008) 'Fundamental considerations of three-level DC-DC converters: topologies, analysis, and control', *IEEE Transactions on Circuits and Systems*, Vol. 55, No. 11, December, pp.3733–3743.

Sayed, K., Abdel-Salam, M., Ahmed, A. and Ahmed, M. (2012) 'New high voltage gain dual-boost DC-DC converter for photovoltaic power systems', *Electric Power Components and Systems*, Vol. 40, No. 7, April, pp.711–728.

Sayed, K., Abdel-Salam, M., Ahmed, A. and Ahmed, M. (2014) 'A ripple current minimization based single phase PWM inverter', *International Journal of Power Electronics*, Vol. 6, No. 3, January, pp.201–223.

Sayed, K. and Nakaoka, M. (2015) 'Performance of induction heating power supply using dual control mode pulse-width modulation–pulse-density modulation high-frequency inverter', *Electric Power Components and Systems*, Vol. 43, No. 2, January, pp.157–166.

Selvaganesan, N., Sundaramurthy, R., Charline, G.D. and Paramasivam, S. (2008) 'Design and implementation of fuzzy logic controller for high performance coupled inductor DC-DC converter', *International Journal of Power Electronics*, Vol. 1, No. 1, January, pp.87–100.

Sugumar, S., Saravanan, E.M., Dinesh, E., Elangovan, D. and Saravanakumar, R. (2013) 'Interleaved buck converter using low voltage and high current application', *International Journal of Applied Engineering Research*, Vol. 8, No. 19, October, pp.2317–2319.

Tsai, C.T. and Shen, C.L. (2009) 'Interleaved soft-switching coupled buck converter with active clamp circuits', *Proc. IEEE International Conference on Power Electronics and Drive Systems (PEDS)*, 2-5 November, Taipei, Taiwan, pp.1113–1118.

Wong, P.L., Xu, P., Yang, B. and Lee, F.C. (2001) 'Performance improvements of interleaving VRMs with coupling inductors', *IEEE Transactions on Power Electronics*, Vol. 168, No. 4, July, pp.499–507.