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High-speed pixel circuits for large-sized 3-D AMOLED displays

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Abstract — Large-sized active-matrix organic light-emitting diode (AMOLED) displays require high-frame-rate driving technology to achieve high-quality 3-D images. However, higher-frame-rate driving decreases the time available for compensating V_{th} in the pixel circuit. Therefore, a new method needs to be developed to compensate the pixel circuit in a shorter time interval. In this work, image quality of a 14-in. quarter full-high-definition (qFHD) AMOLED driven at a frame rate of over 240 Hz was investigated. It was found that image degradation is related to the time available for compensation of the driving TFT threshold voltage. To solve this problem, novel AMOLED pixel circuits for high-speed operation are proposed to compensate threshold-voltage variation at frame rates above 240 Hz. When V_{th} is varied over ±1.0 V, conventional pixel circuits showed current deviations of 22.8 and 39.8% at 240 and 480 Hz, respectively, while the new pixel circuits showed deviations of only 2.6 and 5.4%.

Keywords — *AMOLED, pixel circuit, 3-D, large size, high frame rates.*

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1 Introduction

AMOLED panels use circuits to compensate for variation of threshold voltage (V_{th}) in low-temperature polysilicon thin-film transistors (LTPS TFTs). Although many pixel circuits using various V_{th} compensation methods have been developed,[1–5] there has to date been inadequate research on pixel circuits for large-sized three-dimensional (3-D) AMOLED displays. Recently, increasing attention has been given to the development of large-sized 3-D AMOLED panels.[6,7] In general, 3-D displays are classified into two types: (1) stereoscopic 3-D displays with special glasses[8] and (2) autostereoscopic 3-D displays without glasses.[9] Stereoscopic 3-D displays using glasses have several advantages, including preservation of resolution and zone-independent 3-D viewing. To implement 3-D images with glasses, the left and right images must be shown alternately at periodic intervals. Display driving in this manner requires frame rates of 120 Hz or higher. However, as the frame rate increases, scan time per pixel line decreases, which can create serious problems for proper operation of AMOLED pixel circuits. In particular, compensation for the variation of threshold voltage of LTPS TFTs will not work if the compensation period is too short. The problem gets worse in large-sized AMOLED panels as a result of increased rise and fall times due to large resistive–capacitive (RC) loads. Although there are some approaches to implement 3-D display schemes without increasing frame rates, basically, the development of a high-speed pixel circuit is necessary for achieving the best quality. Therefore, research and development has been under way to enable operation of panels at high frame rates such as 240 Hz. In this paper, we propose a method to implement 3-D AMOLED displays using high-speed driving with a practical pixel circuit. The proposed pixel circuit consists of five transistors and two capacitors. Its input signals are scan (SCAN), emission (EM), and emission bar (EMB). The effect of V_{th} compensation of the pixel circuit is verified in simulation results.

2 3-D display driving scheme

Figure 1 shows a comparison of 2-D and 3-D display driving schemes. Figure 1(a) illustrates a conventional 60-Hz 2-D display driving scheme. The x axis represents time and the y axis represents scan lines. At a frame rate of 60 Hz, the time for one frame is 16.67 msec. During this time, the AMOLED pixel circuit carries out initialization, V_{th} compensation, data writing, and emission.[1,10–12] Figure 1(b) shows a 240-Hz 3-D display driving scheme using shutter glasses. One frame time at 240 Hz is about 4.17 msec, which is 1/4 of the time compared to that for the 60-Hz case. To implement the 3-D display, left and black data are written during the first two frames, and right and black data are written for the following two frames. As described in the figure, the left shutter glass is opened (on) when the left image is emitted and the right shutter glass is on when the right image is emitted. However, it can be difficult to switch liquid-crystal-based shutter glasses on and off in such a short time because their response time is several milliseconds.[8] This may cause a cross-talk problem which is undesirable in 3-D displays. The problem can be solved by reducing the emission duty ratio to match the response time of the shutter glasses. However, reducing the emission time causes a loss of luminance, so that more current must be driven into the OLED to achieve a given luminance. Higher drive levels are not good for AMOLED displays in terms of life and image sticking. In order to avoid this problem, frame rates faster than 240 Hz can be used. As an example of faster operation, a 480-Hz 3-D driving scheme is described in Fig. 1(c). In this case, the black emission period

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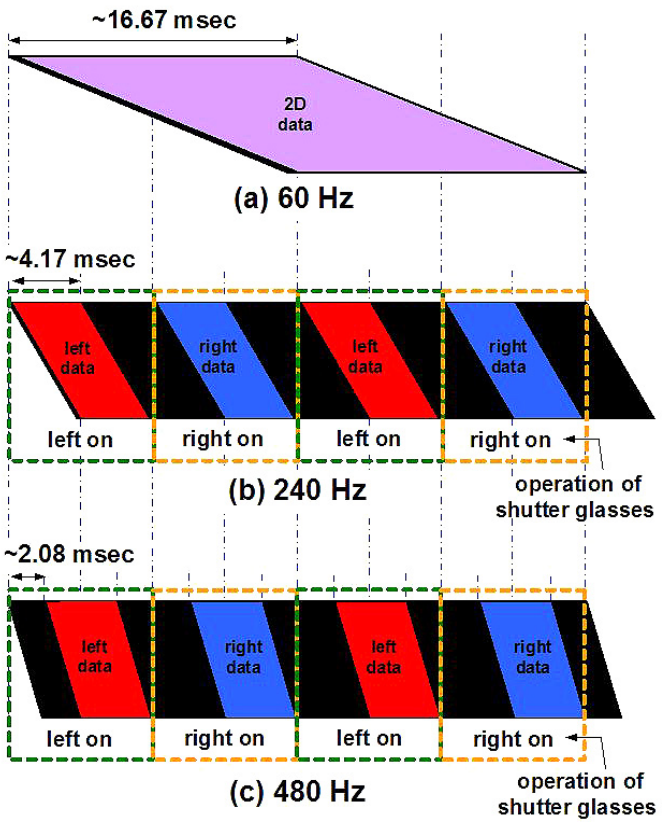

FIGURE 1 — 2-D and 3-D display driving schemes. (a) Conventional 60-Hz 2-D driving; (b) 240-Hz 3-D driving; (c) 480-Hz 3-D driving.

has been increased to be about 2.08 msec. This means that more on/off timing margin is provided for the shutter glasses in consideration of their response time. Accordingly, cross-talk can be reduced using this scheme.

3 High-speed pixel circuit

3.1 Problems at high-speed operation

In order to implement the 240-Hz 3-D and the 480-Hz 3-D driving schemes, it is necessary to design a high-speed pixel circuit capable of completing V_{th} compensation and data writing in a short time. Usually, V_{th} compensation is accomplished by using a diode connection method. In this method, V_{th} of the driving transistor has to be charged to the transistor's gate node before emission. However, most prior pixel circuits have been designed to have one horizontal line time (1H) for V_{th} charging. Therefore, as frame rates increase, less time is allocated to V_{th} compensation.

Figure 2 shows photographs of a 14-in. qFHD AMOLED panel at different 1H times. The pixel circuit consists of six transistors and one capacitor (6T-1C) as shown in Fig. 3. When 1H is 9.7 µsec, the image is uniform as shown in Fig. 2(a). However, when 1H is 0.91 µsec, image uniformity is lost as shown in Fig. 2(b). Specifically, the left and right sides of the image are relatively uniform, but the center of the image shows luminance variation, which is known as random mura. The non-uniform image is attributed to the different RC load. Since the scan and emission drivers are integrated into the left and right sides of the panel, the rise and fall times are longer in the central part of the display. As a result, the V_{th} compensation function does not work properly with a shorter V_{th} charging time. The same problem is expected in the conventional 5T-2C pixel circuit.[6,10,11] As V_{th} charging time is allocated according to the scan time, image quality will depend on operating speed. In addition, the effect will be more severe for higher-resolution panels because the 1H time will be shorter. In this paper, we focused on researching a new driving scheme to achieve better circuit operation for large-sized 3-D AMOLED displays. Detailed results are discussed with comparisons between conventional driving and the new proposed driving scheme.

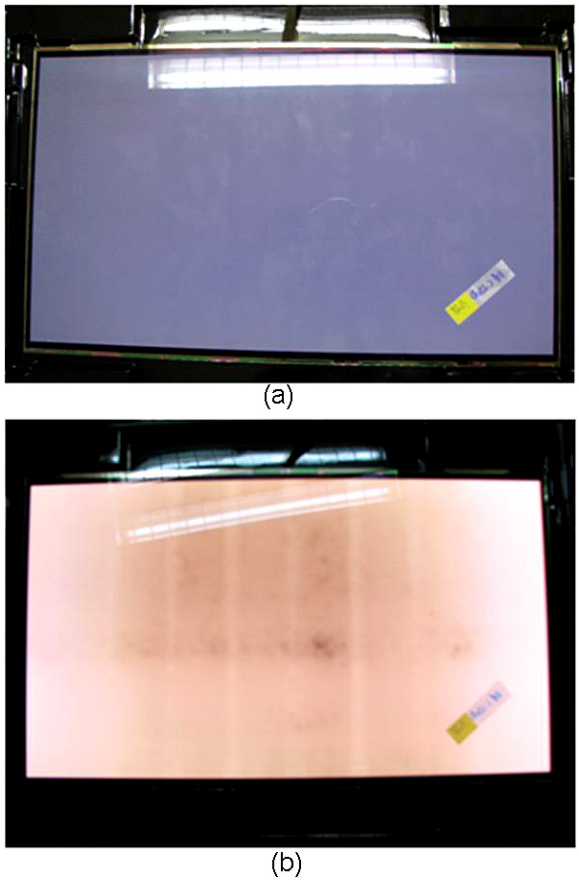

FIGURE 2 — 14-in. qFHD AMOLED panel driven at different speeds: (a) horizontal line time (1H) = 9.7 µsec; (b) horizontal line time (1H) of 0.91 µsec.

3.2 Effect of RC load

Because large-sized AMOLED panels have bigger RC loads, they have longer rise and fall times. In addition to the short 1H time mentioned above, larger distributed RC loads reduce the time available for compensation of V_{th}, resulting in non-uniform images. Therefore, an improved approach for V_{th} compensation is necessary for large panels driven at high frame rates. Most pixel circuits store the V_{th} term when the

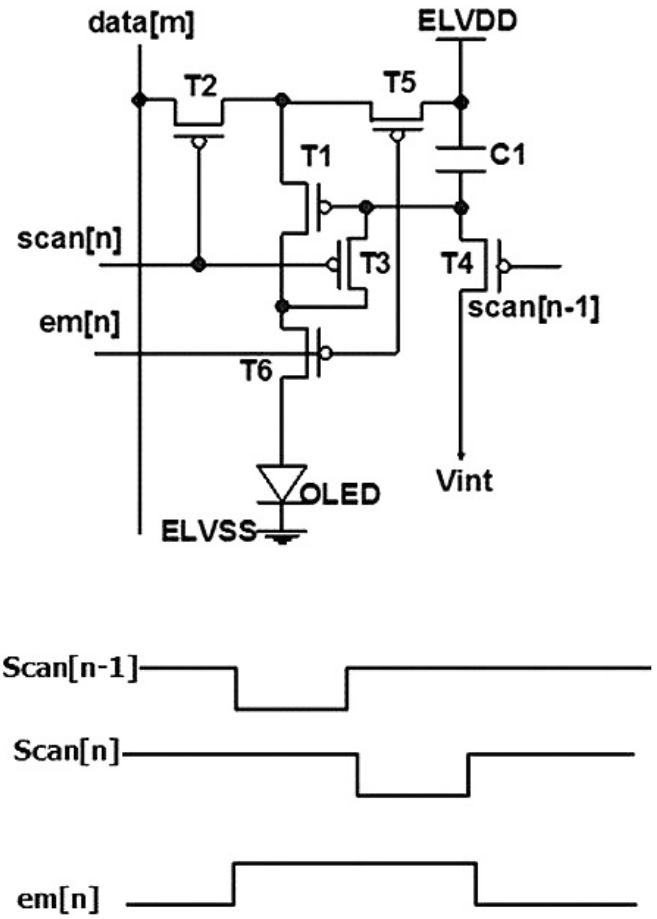

FIGURE 3 — Schematic and timing diagram of 6T-1C AMOLED pixel circuit.

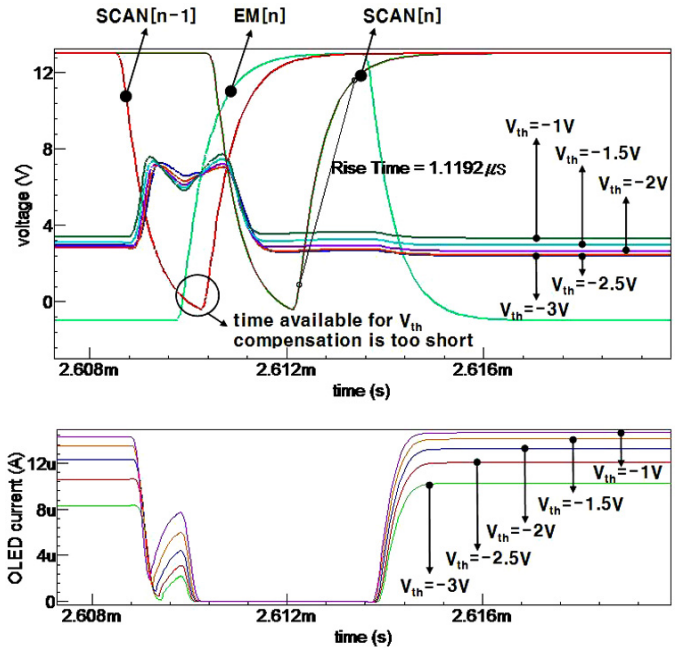

FIGURE 4 — Simulation result of RC load effect on large-sized and high-speed AMOLED panel. Rising time of more than 1 μsec is shown.

scan signal is low by using the diode connection method. Therefore, this low-voltage sustain time is critical for compensation of V_{th} variations. Operation of the conventional 5T-2C pixel circuit was simulated at a 480-Hz driving frequency, and the results are shown in Fig. 4. Scan line loads for a 40-in. AMOLED panel were used in this simulation. It is shown that the rise and fall time of more than 1 μsec significantly affects the period of the low scan voltage. Clearly, reduction in the time available for compensation of V_{th} reduces the circuit's ability to compensate V_{th} variations. To achieve better compensation, low-resistance metal and small parasitic capacitance need to be designed into the layout and process design. Low-resistance metal also reduces IR drops on power lines such as ELVDD, ELVSS, and V_{sus}, which also improves the long-range uniformity of the image.

3.3 New pixel circuit design and operation

A new pixel circuit and its driving scheme are proposed to secure proper operation regardless of 1H time and RC load. The circuit concept is that compensation time is independent of 1H scan time. By using the EMB[n – 1] signal or an extended Scan[n – 2] signal, the proposed pixel circuit has more than a 1H time for V_{th} compensation. The main operating mechanism is the same such that either signal can be used to improve image quality. The circuit operation using EMB[n – 1] is described next.

Figure 5 illustrates the proposed 5T-2C pixel circuit and its input signals. The critical point in this circuit design relates to the input signals. Unlike conventional 5T-2C pixel circuits,[6,10,11] the new circuit uses the EMB[n – 1] signal to

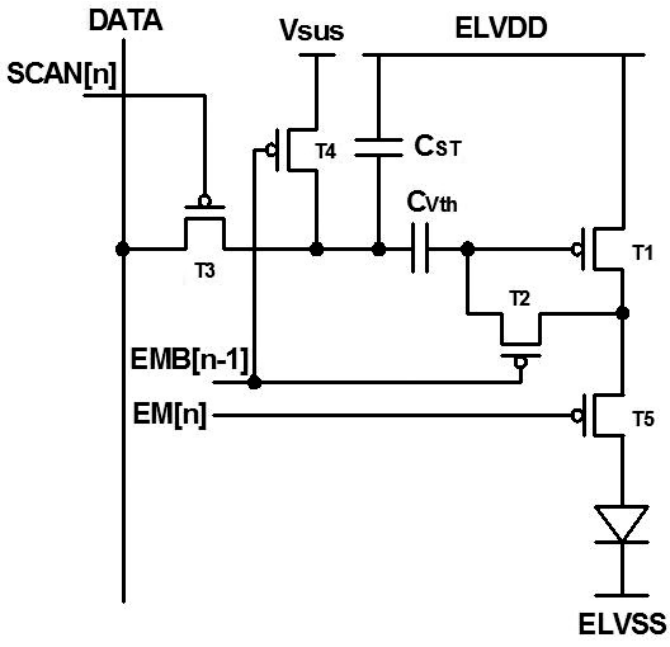

FIGURE 5 — Schematic of 5T-2C AMOLED pixel circuit for high-speed operation.

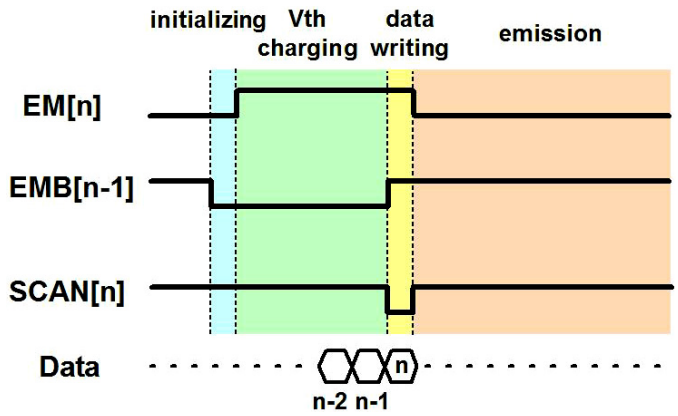

FIGURE 6 — Timing diagram of input signals using EMB[n – 1].

extend the time for V_{th} compensation. Figure 6 shows a timing diagram for the input signals. The operation period is divided into four steps: initializing, V_{th} charging, data writing, and emission. A detailed description of the working mechanism is given next.

The first step in the new scheme is initialization, which occurs by turning on the driving transistor (T1). When both of the EM[n] and EMB[n – 1] signals are low, the switching transistors T2 and T5 turn on. Consequently, the T1 transistor turns on regardless of previous data because the gate voltage of T1 is changed to a value less than ELVDD – $|V_{th}|$.

The next operation is V_{th} charging, which is a key step for compensation of V_{th} variations. In this step, only the EMB[n – 1] signal is low such that T2 and T4 are turned on while other transistors are turned off. Through T1 and T2, the gate node of T1 is charged to ELVDD – $|V_{th}|$ as a result of the diode connection of T1. Here, the stored V_{th} voltage level is highly dependent on the timing for charging. For full high definition (FHD) resolution, one horizontal line time (1H) for 240 and 480 Hz is about 3.7 and 1.85 μsec, respectively. Because of this short time for V_{th} charging, use of a conventional scheme makes it difficult to save the full level of V_{th}. However, in the proposed driving scheme, it is possible to secure complete V_{th} charging due to the controllable length of the EMB signal. In other words, by separating the V_{th} charging period from scan timing, V_{th} compensation can be achieved regardless of frame rates.

The third step is data writing. In this step, the switching transistor T3 turns on so that the data voltage is stored to the gate node of T1 by boosting operation through C_{Vth}. The speed of data writing is relatively faster than V_{th} charging due to the nature of boosting. Finally, the OLED emits when the EM[n] signal is low. The emission current is determined by the equation

$$I_d = \frac{1}{2}\mu \cdot C_{ox}\frac{W}{L}\left(V_{sg} - |V_{th}|\right)^2$$
$$= \frac{1}{2}\mu \cdot C_{ox}\frac{W}{L}\left[\text{ELVDD} - \left(\text{ELVDD} - |V_{th}| + V_{data} - V_{sus}\right) - |V_{th}|\right]^2$$
$$= \frac{1}{2}\mu \cdot C_{ox}\frac{W}{L}\left(V_{sus} - V_{data}\right)^2.$$

As a result of complete V_{th} charging and data writing, the V_{th} term in the equation is eliminated so that the final current is proportional to square of $V_{sus} - V_{data}$.

If an extended Scan[n – 2] signal is used instead of EMB[n – 1], the operating mechanism is similar. Instead of using a long EMB[n – 1] signal, all scan signals are extended to 2H. A longer scan signal can be obtained by the design of the integrated scan driver. The timing diagram for the input signals using Scan[n – 2] is depicted in Fig. 7. Detailed circuit operation for the nth pixel is as follows. Due to the 2H scan length, Scan[n – 2] signal is used instead of Scan[n – 1] to avoid overlap of the V_{th}-charging and data-writing steps. When Scan[n – 2] is low, the pixel circuit is initialized and V_{th} is charged in the same way as described earlier. As the extended Scan[n – 2] signal is presented to the T2 and T4 transistors, the result is longer V_{th} compensation time compared to conventional pixel circuits. Data writing then occurs when the Scan[n] signal is low. During the 2H scan time, [n – 1] data and nth data is entered through switching transistor T3. But this is not a problem because only the final data (nth data) is written to the pixel circuit and expressed as an image. By the same mechanism, the [n – 1]th pixel achieves V_{th} compensation and data writing by using Scan[n – 3] and Scan[n – 1].

In the same way, a Scan[n – 3] signal could be used if its length were extended to 3H. As described in Fig. 8, the nth pixel uses Scan[n – 3] and Scan[n] to perform V_{th} compensation and data writing, and the [n – 1]th pixel uses

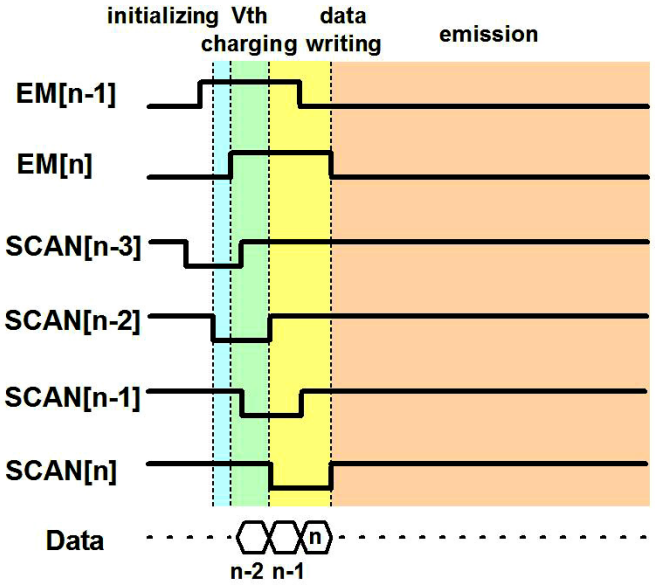

FIGURE 7 — Timing diagram of input signals using Scan[n – 2].

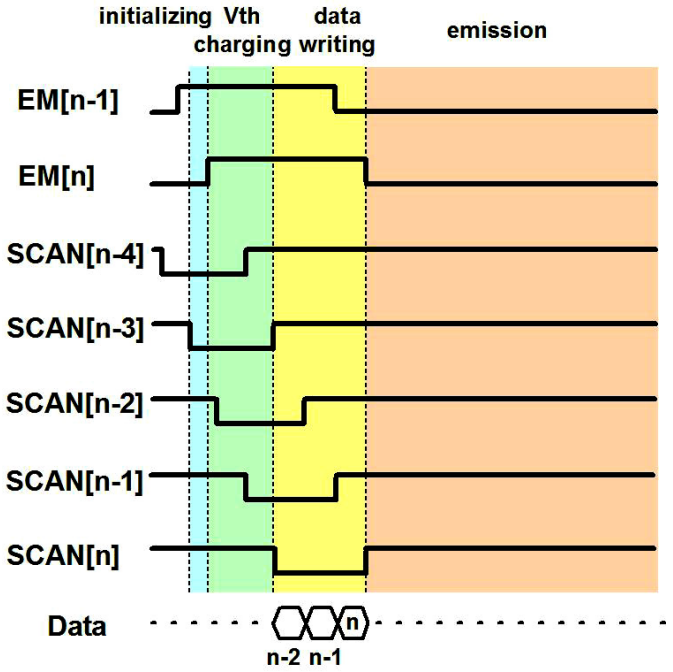

FIGURE 8 — Timing diagram of input signals using Scan[n – 3].

Scan[n – 4] and Scan[n – 1]. The circuit operation is the same as explained above.

3.4 Simulation results

Figure 9 illustrates the simulation result of the proposed driving scheme when frame rates are 480 Hz. The data shows the gate voltage of the driving transistor for each operating step. In this simulation, it is assumed that the panel has a TFT V_{th} distribution range of ±0.5 and ±1.0 V.

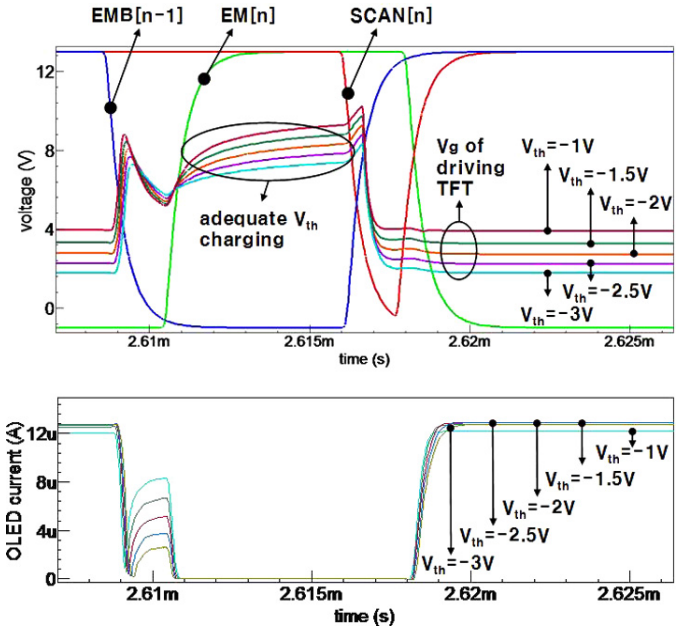

FIGURE 9 — Simulation result of the proposed driving scheme when frame rates are 480 Hz.

The result shows proper circuit operation at each step. Notably, it is observed that the appropriate V_{th} compensation is achieved because adequate time is provided for V_{th} charging. In this figure, OLED current deviation is reduced compared to that of using the conventional driving scheme in Fig. 4.

Figure 10 shows a comparison of OLED current deviation between a conventional circuit and driving scheme and the new proposed circuit and driving scheme at frame rates of 120, 240, and 480 Hz. A 40-in. RC load condition was used in both cases. The simulation results are for a high-gray-level image and the average OLED current is 12.3 μA. Both driving schemes have similar V_{th} compensation performance at frame rates of 120 Hz. However, at high frame rates, the conventional scheme showed significantly greater current deviation. The conventional scheme had current deviations of 22.8 and 39.8% for 240 and 480 Hz, respectively. However, current deviations of only 2.6 and 5.4% were obtained using the proposed scheme. These results clearly show that the proposed method has better V_{th} compensation performance at high-speed operation.

In summary, the proposed scheme makes it possible to operate the pixel circuit at high frame rates because the time provided for V_{th} charging is independent of scan time. In addition, this high-speed operation offers benefits for 2-D operation. When the frame rates are increased, LCDs show better (lower) MPRT, or moving picture response time. Similarly, when driven at higher frame rates as enabled by the new scheme, AMOLEDs will achieve better moving picture perceptual resolution (MPPR), which is a new measurement method for moving image quality.[13]

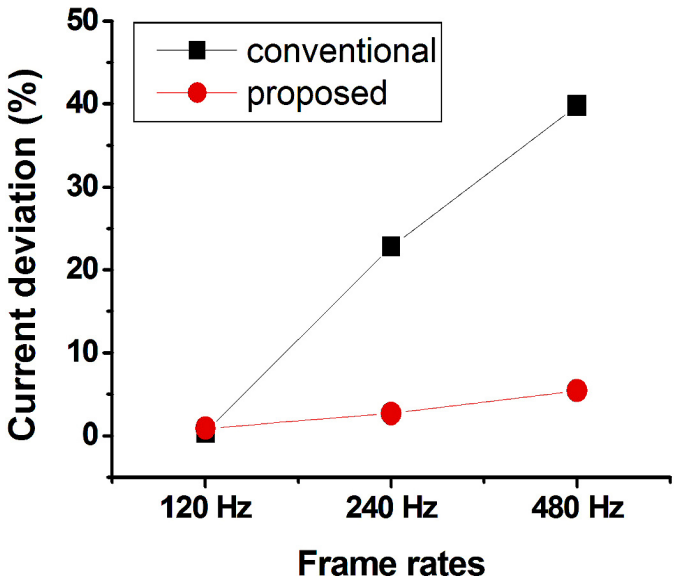

FIGURE 10 — Comparison of current deviation between conventional scheme and proposed scheme.

4 Conclusions

An AMOLED pixel circuit and driving scheme are proposed for operation at high frame rates. The proposed driving scheme ensures sufficient time for V_{th} compensation using controllable input signals. A 3-D AMOLED display can be achieved by using this driving scheme because it is possible to operate the pixel circuit at frame rates of 240 Hz or higher. In the 480-Hz system, crosstalk between left and right images can be reduced. In addition, high-speed circuit operation results in improved MPPR.

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