# Control Integrated POwer System (CIPOS™)

## Reference Board for IGCMxxF60GA with 3-shunt

## AN-CIPOS mini-2-Reference Board-3

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For Power Management Application

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**Table of contents**

# 1 Introduction

This reference board is composed of the IGCMxxF60GA, its minimum peripheral components and three shunt resistors. It is designed for customers to evaluate the performance of CIPOS™ with simple connection of the control signals and power wires. Figure 1 shows the external view of reference board.

This application note also describes how to design the key parameters and PCB layout.

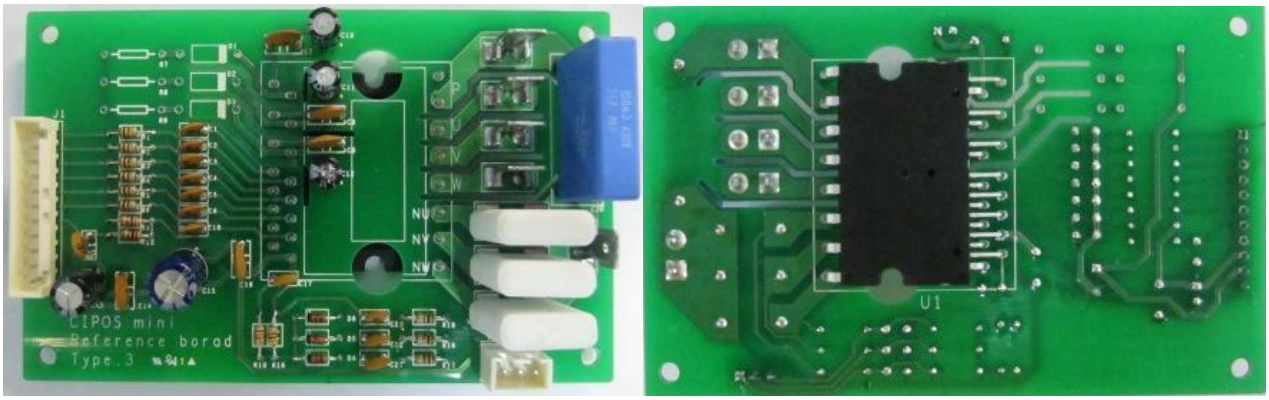


**Figure 1. Reference board for IGCMxxF60GA**

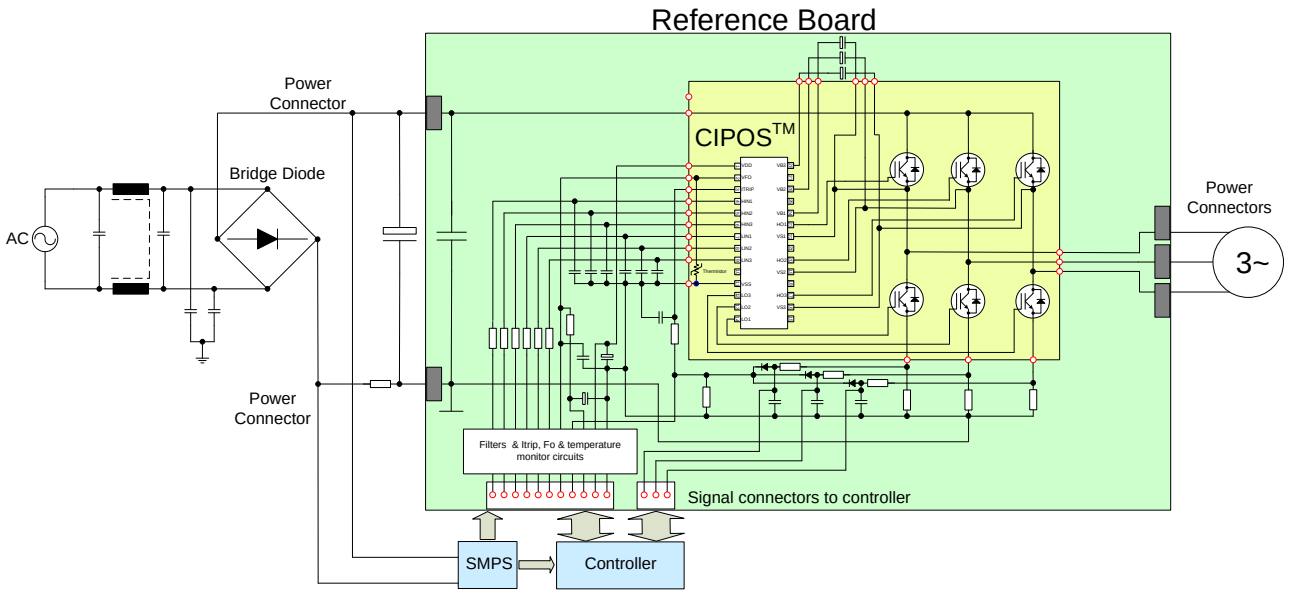


**Figure 2. Application example**

# 2 Schematic

Figure 3 shows a circuitry of the reference board for IGCMxxF60GA.

The reference board consists of interface circuit, bootstrap circuit, snubber capacitor, short-circuit protection, fault output circuit and three shunt resistors.

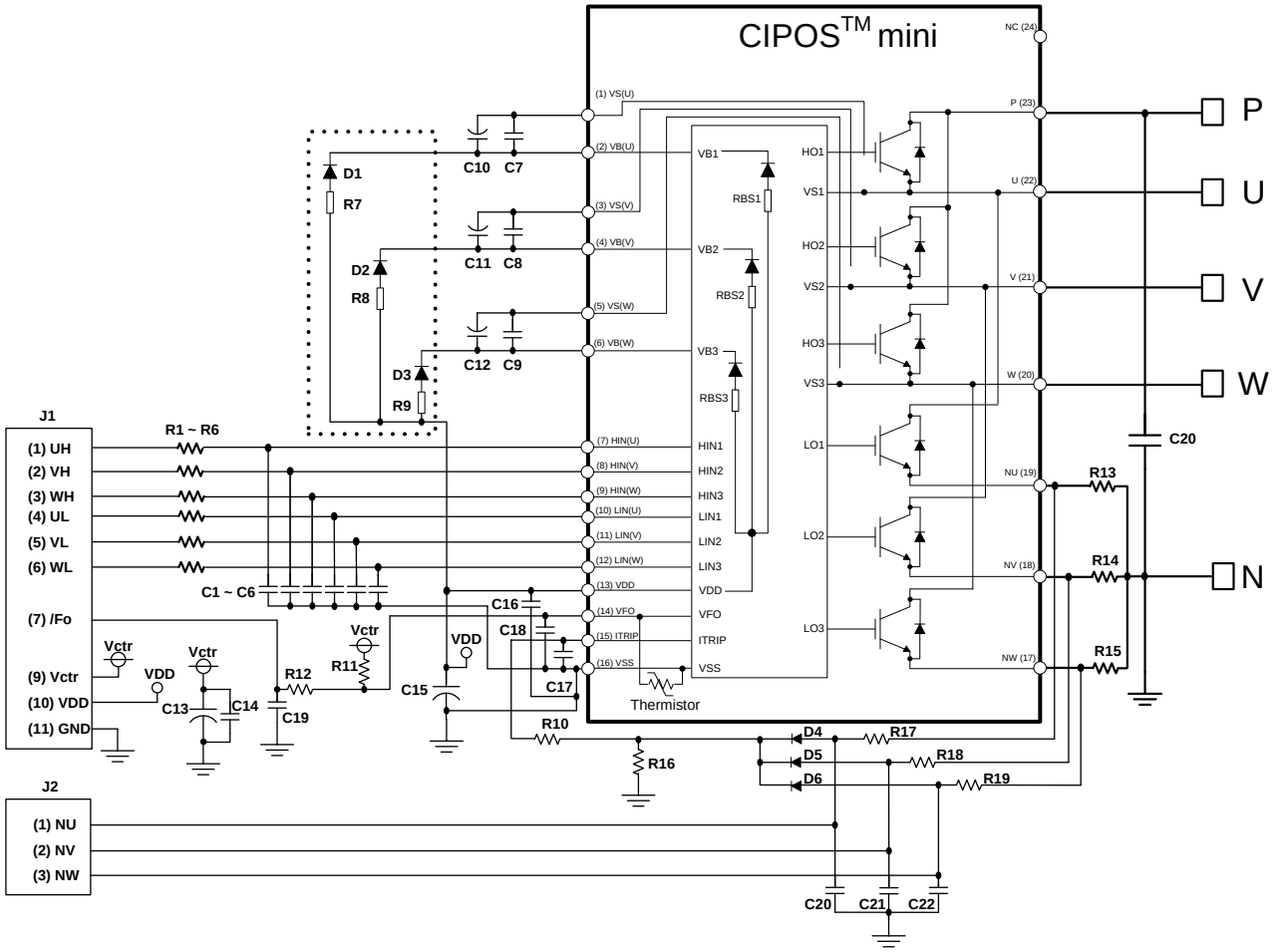


**Figure 3. Circuit of the reference board**

Note: Vctr denotes the controller supply voltage such as 5V or 3.3V.
It is optional to use external bootstrap circuit together with internal one as shown in dot line, in case that smaller bootstrap resistor is necessary.

# 3 External Connection

## 3.1 Signal Connector (J1, 2.5mm pitch connector)

| Pin | Name | Description |
|---|---|---|
| 1 | HIN(U) | High side control signal input of U phase |
| 2 | HIN(V) | High side control signal input of V phase |
| 3 | HIN(W) | Low side control signal input of W phase |
| 4 | LIN(U) | Low side control signal input of U phase |
| 5 | LIN(V) | Low side control signal input of V phase |
| 6 | LIN(W) | Low side control signal input of W phase |
| 7 | /Fo | Fault output signal / Temperature monitor |
| 8 | NC | No Connection |
| 9 | Vctr | External control voltage (5V or 3.3V) |
| 10 | VDD | External 15V supply voltage |
| 11 | GND | Ground |

## 3.2 Signal Connector (J2, 2.5mm pitch connector)

| Pin | Name | Description |
|---|---|---|
| 1 | ISEN(NU) | Current monitor output of NU |
| 2 | ISEN(NV) | Current monitor output of NV |
| 3 | ISEN(NW) | Current monitor output of NW |

## 3.3 Power Connector

| Pin | Description |
|---|---|
| U | Output terminal of U phase |
| V | Output terminal of V phase |
| W | Output terminal of W phase |
| P | Positive terminal of DC link voltage |
| N | Negative terminal of DC link voltage |

# 4 Key Parameters Design Guide

## 4.1 Circuit of Input Signals (LIN, HIN)

The input signals can be either TTL- or CMOS-compatible. The logic levels can go down to 3.3V. The maximum input voltage of the pins is internally clamped to 10.5V. However, the recommended voltage range of input voltage is up to 5V. The control pins LIN and HIN are active high.
They have an internal pull-down structure with a pull-down resistor value of nominal 5kΩ. The input noise filter inside CIPOS™ suppresses short pulse and prevents the driven IGBT from unintentional operation. The input noise filter time ($t_{FLIN}$) is typically 270ns. This means that an input signal must stay on more than 270ns so that the input signal can be processed correctly. CIPOS™ can be connected directly to controller without external input RC filter thanks to the internal pull down resistor and input noise filter as shown in Figure 4.

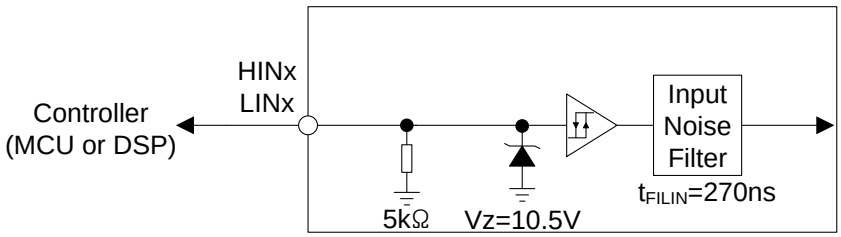


**Figure 4. Filter of input signals and pull-down circuit**

## 4.2 Bootstrap Capacitor

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to Figure 5. It is only the effective circuit shown for one of the three half bridges. The bootstrap functionality is composed internally to limit current. Please refer to the datasheet and application note for bootstrapping method in detail.

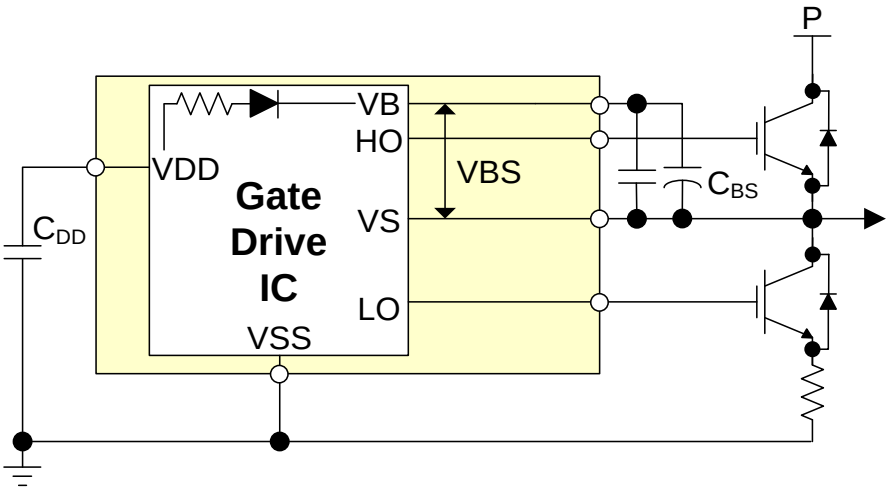


**Figure 5. Bootstrap circuit for the supply of a high side gate drive**

A low leakage current of the high side section is very important in order to keep the bootstrap capacitors small. The $C_{BS}$ discharges mainly by the following mechanisms:

- Quiescent current to the high side circuit in the IC
- Gate charge for turning high side IGBT on
- Level-shift charge required by level shifters in the IC
- Leakage current in the bootstrap diode
- $C_{BS}$ capacitor leakage current (ignored for non-electrolytic capacitor)
- Bootstrap diode reverse recovery charge

The calculation of the bootstrap capacitor results in

$$C_{BS} = \frac{I_{leak} \times t_P}{\Delta V_{BS}}$$

with $I_{leak}$ being the maximum discharge current of $C_{BS}$, $t_P$ the maximum on pulse width of high side IGBT and $\Delta V_{BS}$ the voltage drop at the bootstrap capacitor within a switching period.

Practically, the recommended leakage current is 1mA of $I_{leak}$ for CIPOS™.

Figure 6 shows the curve corresponding to above equation for a continuous sinusoidal modulation, if the voltage ripple $\Delta V_{BS}$ is 0.1V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range up to 4.7µF for most switching frequencies. In other PWM method case like a discontinuous sinusoidal modulation, $t_P$ must be set the longest period of the low side IGBT off.

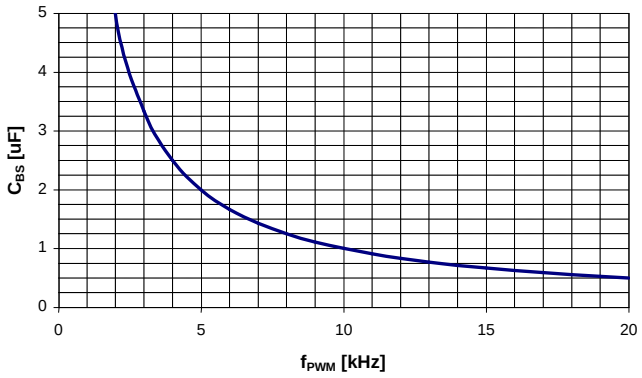


**Figure 6. Size of the bootstrap capacitor as a function of the switching frequency $f_{PWM}$**

## 4.3 Internal Bootstrap Functionality Characteristics

CIPOS™ includes three bootstrap functionalities in internal drive IC, which consist of three diodes and three resistors, as shown in Figure 5. Typical value of internal bootstrap resistor is 40Ω. For more information, please refer to the below table. It's noted that $R_{BS2}$ and $R_{BS3}$ have same value to $R_{BS1}$.

| Description | Condition | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Repetitive peak reverse voltage | | $V_{RRM}$ | 600 | | | V |
| Bootstrap resistance of U-phase | VS2 or VS3=300V, $T_J$=25°C<br>VS2 and VS3=0V, $T_J$=25°C<br>VS2 or VS3=300V, $T_J$=125°C<br>VS2 and VS3=0V, $T_J$=125°C | $R_{BS1}$ | | 35<br>40<br>50<br>65 | | Ω |
| Reverse recovery | $I_F$=0.6A, di/dt=80A/µs | $t_{rr\_BS}$ | | 50 | | ns |
| Forward voltage drop | $I_F$=20mA, VS2 and VS3=0V | $V_{F\_BS}$ | | 2.6 | | V |

## 4.4 Over Current Protection

The OC (Over Current) protection level is decided by ITRIP positive going threshold voltage $V_{IT,TH+}$ in CIPOS™ and shunt resistance. When ITRIP voltage exceeds $V_{IT,TH+}$, CIPOS™ turns off 6 IGBTs and fault-output is activated during fault-output duration time, typically 65us.

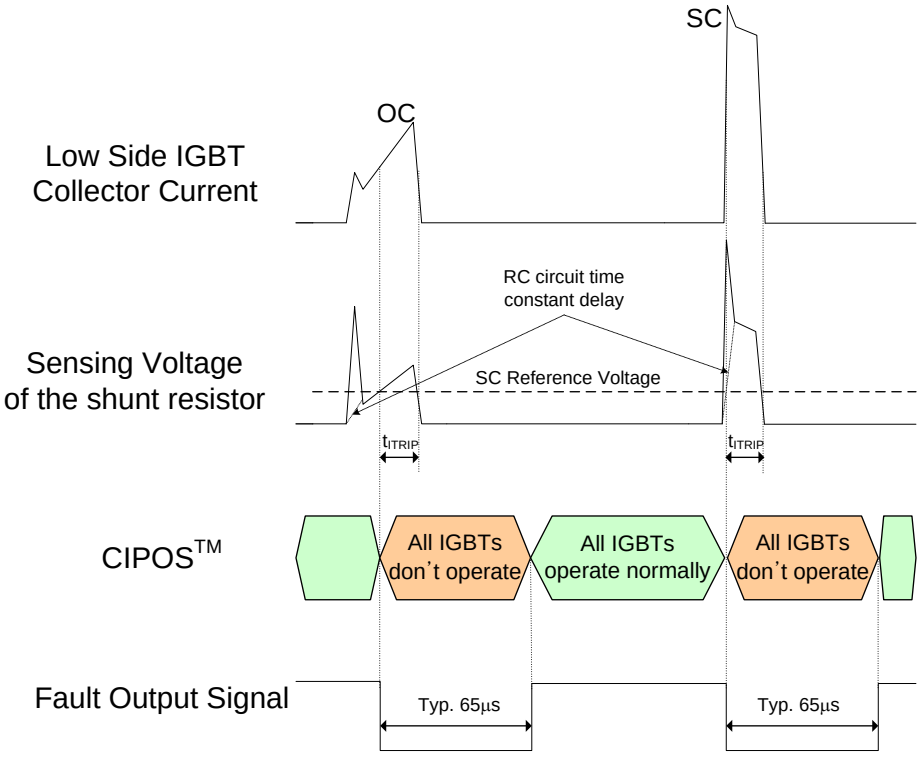


**Figure 7. Timing chart of OC protection**

### 4.4.1 Shunt Resistor Selection

The value of shunt resistor is calculated by the following equation.

$$R_{SH} = \frac{V_{IT,TH+} + V_{FILTER,DIODEDROP}}{I_{OC}}$$

Where $V_{IT,TH+}$ is the ITRIP positive going threshold voltage of CIPOS™ and $I_{OC}$ is the current of SC detection level. $V_{IT,TH+}$ is $0.47V_{typ.}$ $V_{FILTER,\ DIODE}$ is drop voltage between ITRIP and Rsh. $V_{FILTER,\ DIODE}$ is 0.62V. So the voltage of ITRIP is reached to 0.47V when voltage of $R_{SH}$ is 1.09V.
The maximum value of OC protection level should be set less than the repetitive peak collector current in the datasheet considering the tolerance of shunt resistor.
For example, the maximum peak collector current of IGCM10F60GA is $18A_{peak}$,

$$R_{SH(min)} = \frac{1.09}{18} = 0.06\Omega$$

So the recommended value of shunt resistor is over 60mΩ for IGCM10F60GA.
For the power rating of the shunt resistor, the below lists should be considered.

- Maximum load current of inverter ($I_{rms}$)
- Shunt resistor value at Tc=25°C ($R_{SH}$)
- Power derating ratio of shunt resistor at $T_{SH}$=100°C
- Safety margin

And the power rating is calculated by following equation.

$$P_{SH} = \frac{1}{2} \times \frac{I_{rms}{}^2 R_{SH} \times \text{marigin}}{\text{Derating ratio}}$$

For example, In case of IGCM10F60GA and $R_{SH}$=60mΩ

- Max. load current of inverter : $6A_{rms}$
- Power derating ratio of shunt resistor at $T_{SH}$=100°C : 80%
- Safety margin : 30%

$$P_{SH} = \frac{1}{2} \times \frac{6^2 \times 0.06 \times 1.3}{0.8} = 1.76W$$

So the proper power rating of shunt resistor is over 2W.

Based on the previous equations, conditions and calculation method, minimum shunt resistance and resistor power according to all kinds of IGCMxxF60GA products are introduced as shown in below table. It's noted that a proper resistance and its power over than minimum values should be chosen considering over-current protection level required in the application set.

| Product | Maximum Peak Current | Minimum Shunt Resistance, RSH | Minimum Shunt Resistor Power, PSH |
|---|---|---|---|
| IGCM06F60GA | 12 | 91mΩ | 1.5W |
| IGCM10F60GA | 18 | 60mΩ | 2W |
| IGCM15F60GA | 30 | 37mΩ | 3W |
| IGCM20F60GA | 45 | 25mΩ | 5W |

### 4.4.2 Delay Time

The RC filter should be necessary in OC sensing circuit to prevent malfunction of OC protection from noise interference. The RC time constant is determined by applying time of noise and the withstand time capability of IGBT. When the current on shunt resistor exceeds OC protection level ($I_{OC}$), this voltage is applied to the ITRIP pin of CIPOS™ via the RC filter. The filter delay time ($t_{Filter}$) that the input voltage of ITRIP pin rises to the ITRIP positive threshold voltage is caused by RC filter time constant. In addition there is the shutdown propagation delay of Itrip ($t_{ITRIP}$). Please refer to the below table.

| Item | | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Shut down propagation delay ($t_{ITRIP}$) | IGCM20F60GA | $I_{out}$ =15A, from $V_{IT,TH+}$to 10% $I_{out}$ | - | 1540 | - | ns |
| | IGCM15F60GA | $I_{out}$ =10A, from $V_{IT,TH+}$to 10% $I_{out}$ | - | 1340 | - | |
| | IGCM10F60GA | $I_{out}$ =6A, from $V_{IT,TH+}$to 10% $I_{out}$ | - | 1260 | - | |
| | IGCM06x60GA | $I_{out}$ =4A, from $V_{IT,TH+}$to 10% $I_{out}$ | - | 1300 | - | |

Therefore, the total delay time from occurrence of OC to shutdown of the IGBT gate becomes

$$t_{total} = t_{Filter} + t_{ITRIP}$$

Shut down propagation delay is in inverse proportion to the current range, therefore $t_{ITRIP}$ is reduced at higher current condition than condition of table 14. The total delay must be less than 5μs of short circuit withstand time ($t_{SC}$) in datasheet. Thus, RC time constant should be set in the range of 1~2μs. It is recommended that R10 of 1.8kΩ, R16~R18 of 100Ω, C17 of 1nF and C2~C22 of 1nF.

## 4.5 Temperature Monitor and Protection

In case of CIPOS™, built-in thermistor (85kΩ at 25°C) is connected between VFO and VSS. The typical application circuit is like Figure 8 where the VFO pin is used for both thermistor temperature detection and fault detection. The voltage of VFO pin decreases as the thermistor temperature increases due to external pull-up resistor. It is noted that the voltage variation of VFO pin due to temperature variation should be always higher than the fault detection level of micro controller. In this reference board, the pull-up resistor is set to 3.6kΩ so that the VFO voltage becomes 2.95V and 1.95V respectively for 5V and 3.3V control voltage (Vctr) when the temperature of thermistor is 100°C as shown in Figure 9.

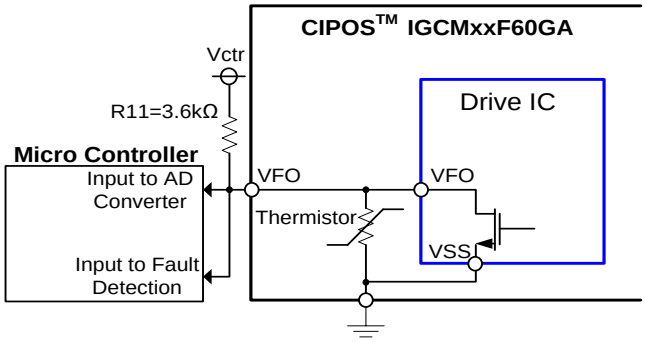


**Figure 8. Temperature monitor with built in thermistor and pull up resistor**

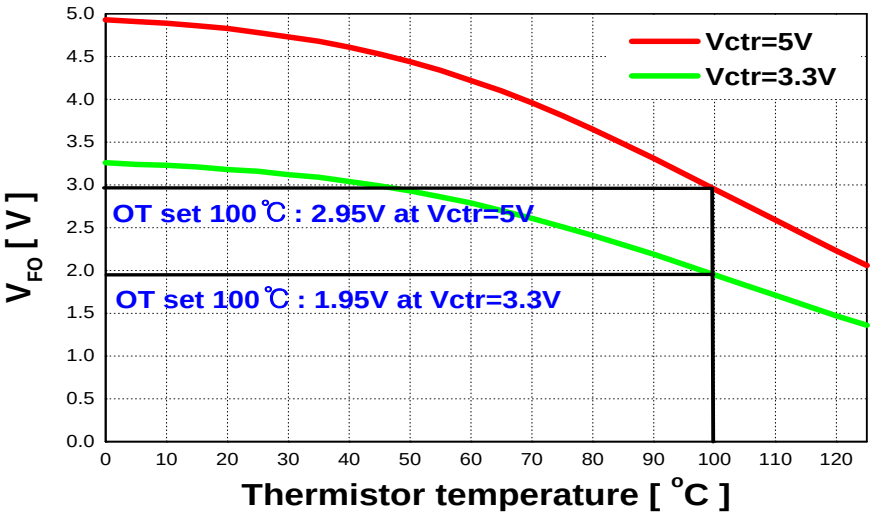


**Figure 9. Voltage of $V_{FO}$ according to the temperature**

# 5 Part list

| Symbol | Components | Note |
|---|---|---|
| R1 ~ R6 | 100Ω, 1/8W, 5% | Series resistors for input voltage |
| R7 ~ R9 | No Connection | Note 1 |
| R10 | 1.8kΩ, 1/8W, 1% | Series resistor for current sensing voltage |
| R11 | 3.6kΩ, 1/8W, 1% | Pull-up resistor for fault output voltage |
| R12 | 1kΩ, 1/8W, 5% | Series resistor for fault output voltage |
| R13 ~ R15 | Content 4.4.1 | Current sensing resistor |
| R16 | 3kΩ, 1/8W, 5% | Pull-down resistor for ITRIP voltage |
| R17 ~ R19 | 100Ω, 1/8W, 1% | Series resistor for current sensing voltage |
| C1 ~ C6 | 1nF, 25V | Bypass capacitors for input voltage |
| C7 ~ C9 | 0.1uF, 25V | Bypass capacitors for high side bias voltage |
| C10 ~ C12 | 22uF, 35V | Bootstrap capacitors |
| C13 | 100uF, 35V | Source capacitor for 5 or 3.3V supply voltage |
| C14 | 0.1uF, 35V | Bypass capacitor for 5 or 3.3V supply voltage |
| C15 | 220uF, 35V | Source capacitor for VDD supply voltage |
| C16 | 0.1uF, 35V | Bypass capacitor for VDD supply voltage |
| C17 | 1nF, 25V | Bypass capacitor for current sensing voltage |
| C18 | 1nF, 16V | Bypass capacitor for fault output voltage |
| C19 | 1nF, 16V | Bypass capacitor for fault output voltage |
| C20 | 0.1uF, 630V | Snubber capacitor |
| C20 ~ C22 | 1nF, 25V | Bypass capacitor for current sensing voltage |
| D1 ~ D3 | No Connection | Note 1 |
| D4 ~ D6 | 1N4148 | Series diode for current sensing voltage |
| J1 | SMW250-11P | Signal & Power supply connector |
| J2 | SMW250-03P | Current sensing connector |
| U, V, W, P, N | Fasten Tap | Power terminals |

Note 1: It is optional to use external bootstrap circuit together with internal one, in case that smaller bootstrap resistor is necessary.

# 6 PCB Design Guide

In general, there are several issues to be considered when designing an inverter board as below lists.

- Low stray inductive connection
- Isolation distance
- Component placement

This chapter explains above considerations and method for the layout design.

## 6.1 Layout of Reference Board

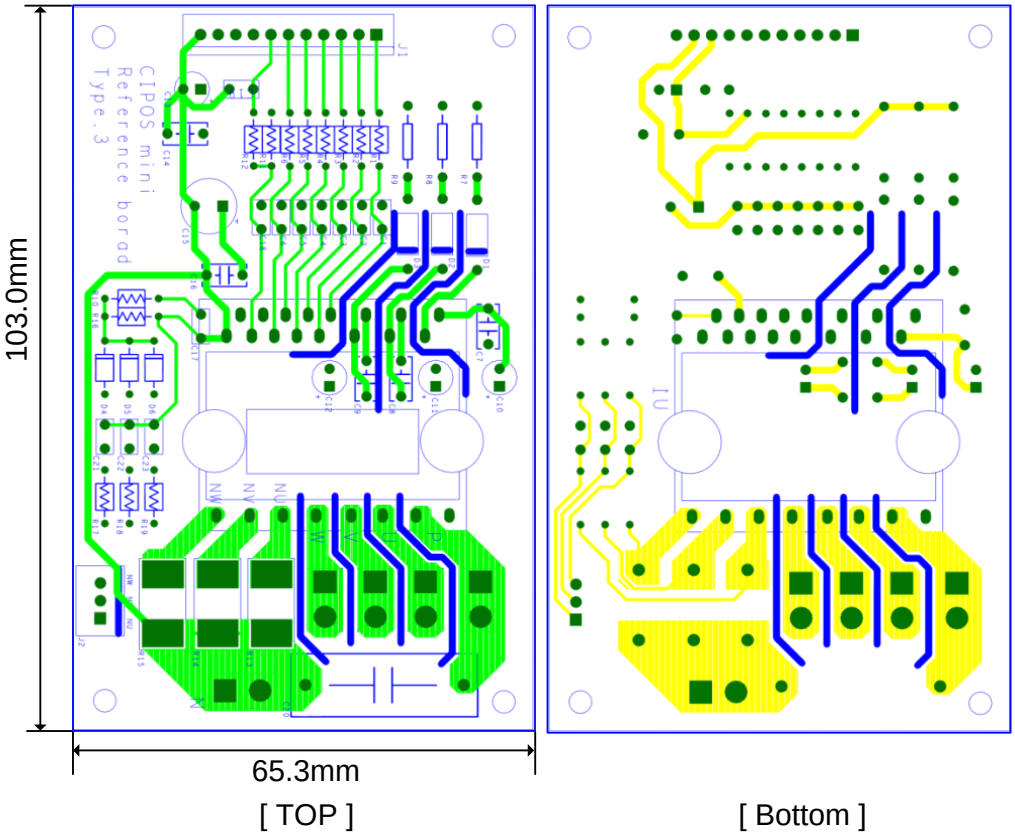


**Figure 10. Layout of reference board for IGCMxxF60GA**

Note.

2. The connection between emitters of CIPOS™ (NU, NV, NW) and shunt resistor should be as short and as wide as possible.
3. It is recommended that ground pin of micro-controller be directly connected to VSS pin. Signal ground and power ground should be as short as possible and connected at only one point via the capacitor (C16).
4. All of the bypass capacitors should be placed as close to the pins of CIPOS™ as possible.
5. The capacitor (C17) for shunt voltage sensing should be placed as close to ITRIP and VSS pins as possible.
6. In order to detect sensing voltage of the shunt resistor exactly, both sensing and ground patterns should be connected at pins of the shunt resistor and should not be overlapped with any patterns for load current as shown in Figure 10.
7. The snubber capacitor (C19) should be placed as close to the terminals as possible.
8. The power patterns of U, V, W, P, NU, NV and NW should be designed on both layer with via to cover the high current and there should be kept the isolation distance among the power patterns over 2.54mm.
9. There are milling profiles in blue line to keep the isolation distance
10. All components except IGCMxxF60GA are placed on the top layer.

# 7 Reference

[1] **LS Power Semitech:** CIPOS™ IGCM10F60GA; Datasheet Ver. 1.0; LS Power Semitech, 2010



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