Figure 23.

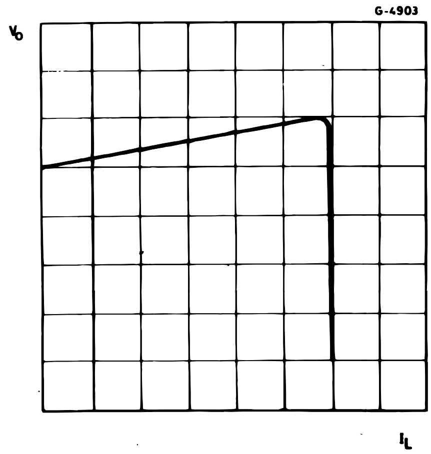
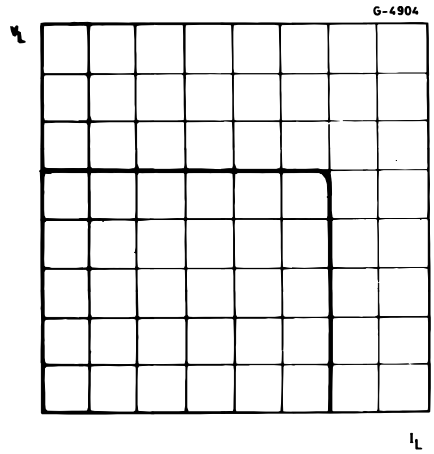


Figure 24.



MOTOR SPEED CONTROL

Fig. 25 shows how to use the device for the speed control of permanent magnet motors. The desired speed, proportional to the voltage at the terminal of the motor, is obtained by means of R1 and R2.

$$V_M = V_{ref} \left(1 + \frac{R2}{R1}\right)$$

To obtain better compensation of the internal motor resistance, which is essential for good regulation, the following equation is used :

$$R3 \leq \frac{R1}{R2} \bullet RM$$

This equation works with infinite R4. If R4 is finite, the motor speed can be increased without altering the ratio R2/R1 and R3. Since R4 has a constant voltage (V_{ref}) at its terminals, which does not vary as R4 varies, this voltage acts on R2 as a constant current source variable with R4. The voltage drop on R2 thus increases, and the increase is felt by the voltage at the terminals of the motor. The voltage increase at the motor terminals is :

$$V_M = \frac{V_{ref}}{R4 + R3} \bullet R2$$

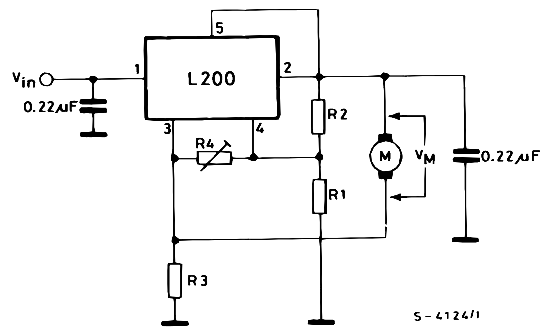
A circuit for a 30 W motor with $R_M = 4\ \Omega$, R1 = 1 kΩ, R2 = 4.3 kΩ, R4 = 22 kΩ and R3 = 0.82 Ω has been realized.

POWER AMPLITUDE MODULATOR

In the configuration of fig. 26 the L200 is used to send a signal onto a supply line. Since the input signal V_i is DC decoupled, the V_o is defined by :

$$V_O = V_{ref} \left(1 + \frac{R2}{R1}\right)$$

Figure 25.



The amplified signal V_i whose value is :

$$G_V = -\frac{R2}{R3}$$

is added to this component. By ignoring the current entering pin 4, we must impose $i_1 = i_2 + i_3$ (1) and since the voltage between pin 4 and ground remains fixed (V_{ref}) as long as the device is not in saturation, $i_1 = 0$ and equation (1) becomes :

$$i_2 = -i_3 \text{ with } i_3 = \frac{V_i}{R3} \qquad (\text{for } X_c \ll R3) \quad \text{Therefore}$$

$$V_o = R2\ i_2 = -\frac{V_i}{R3} \bullet R2$$

An application is shown in fig. 27. If the DC level is to be varied but not the AC gain, R1 should be replaced by a potentiometer.

Figure 26.

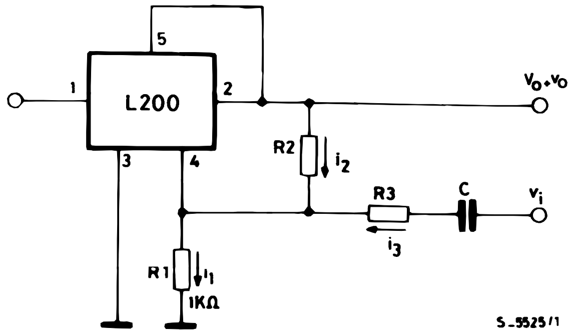
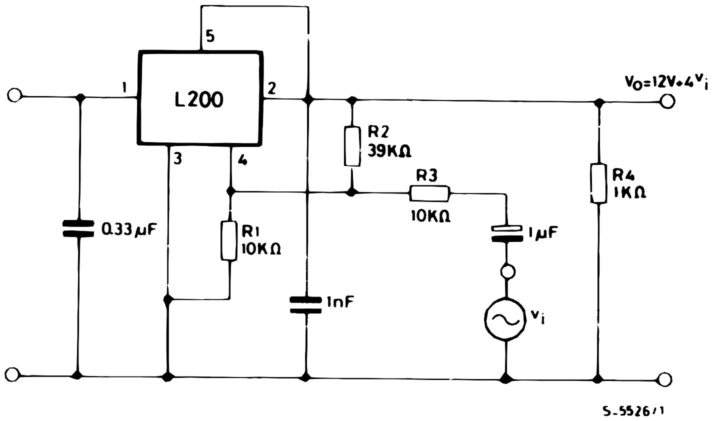


Figure 27.



HIGH CURRENT REGULATORS

To get a higher current than can be supplied by a single device one or more external power transistors must be introduced. The problem is then to extend all the device's protection circuits (short-circuit protection, limitation of T_j of external power devices and overload protection) to the external transistors. Constant current or foldback current limitation therefore becomes necessary.

When the regulator is expected to withstand a permanent shortcircuit, constant current limitation becomes more and more difficult to guarantee as the nominal V_o increases. This is because of the increase in V_{CE} at the terminals of the transistor, which leads to an increase in the dissipated power. The heatsink has to be calculated in the heaviest working conditions, and therefore in shortcircuit. This increases weight, volume and cost of the heatsink and increase of the ambient temperature (because of high power dissipation). Besides heatsink, power transistors must be dimensioned for the short-circuit.

This type, of limitation is suited, for example, with highly capacitive loads. Efficiency is increased if preregulation is used on the input voltage to maintain a constant drop-out on the power element for all V_{out}, even in shortcircuit. Foldback limitation, on the other hand, allows lighter shortcircuit operating conditions than the previous case. The type of load is important.

If the load is highly capacitive, it is not possible to have a high ratio between I_{max} and I_{sc} because at switch-on, with load inserted, the output may not reach its nominal value.

Other protection against input shortcircuit, mains failure, overvoltages and output reverse bias can be realized using two diodes, D1 and D2, inserted as indicated in fig. 28.

Figure 28.

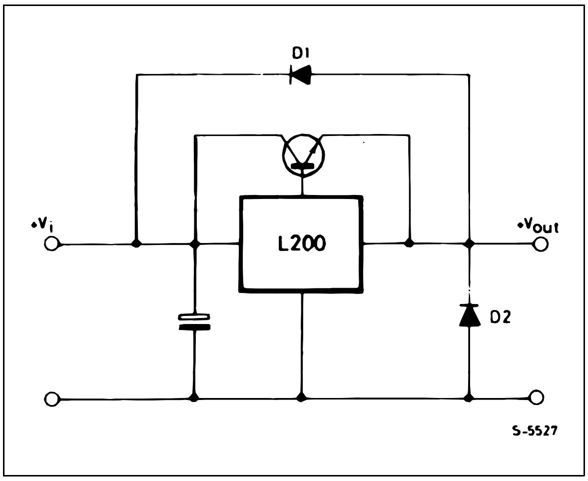
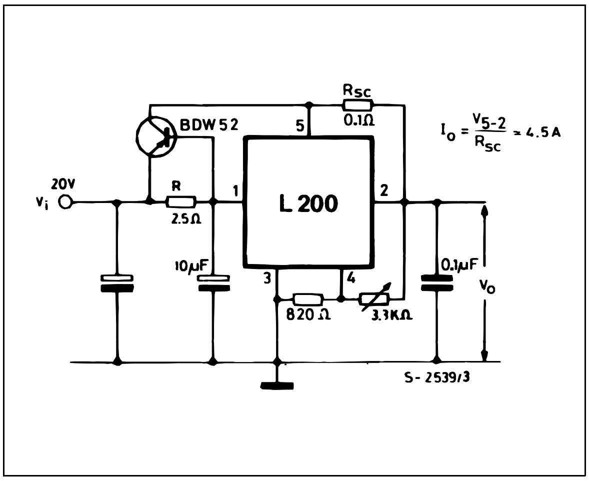


Figure 29.



USE OF A PNP TRANSISTOR

Fig. 29 shows the diagram of a high current supply using the current limitation of the L200. The output current is calculated using the following formula :

$$I_o = \frac{VSC}{RSC} \cong \frac{0.45\ V}{0.1\ \Omega} = 4.5\ A$$

Constant current limitation is used ; so, in output shortcircuit conditions, the transistor dissipates a power equal to :

$$P_D = V_i \bullet I_o = V_i \bullet \frac{V_{SC}}{R_{SC}}$$

The operating point of the transistor should be kept well within the SOA ; with $R_{SC} = 0.1\ \Omega$, V_i must not exceed 20 V. Part of the I_o crosses the transistor and part crosses the regulator.

The latter is given by : $I_{REG} = I_B + \frac{V_{BE}}{R}$

where I_B is the base current of the transistor (– 100 mA at $I_C = 4$ A) and V_{BE} is the base-emitter voltage (– 1 V at $I_C = 4$ A) ; with R = 2.5 Ω, $I_{REG} \cong 500$ mA.

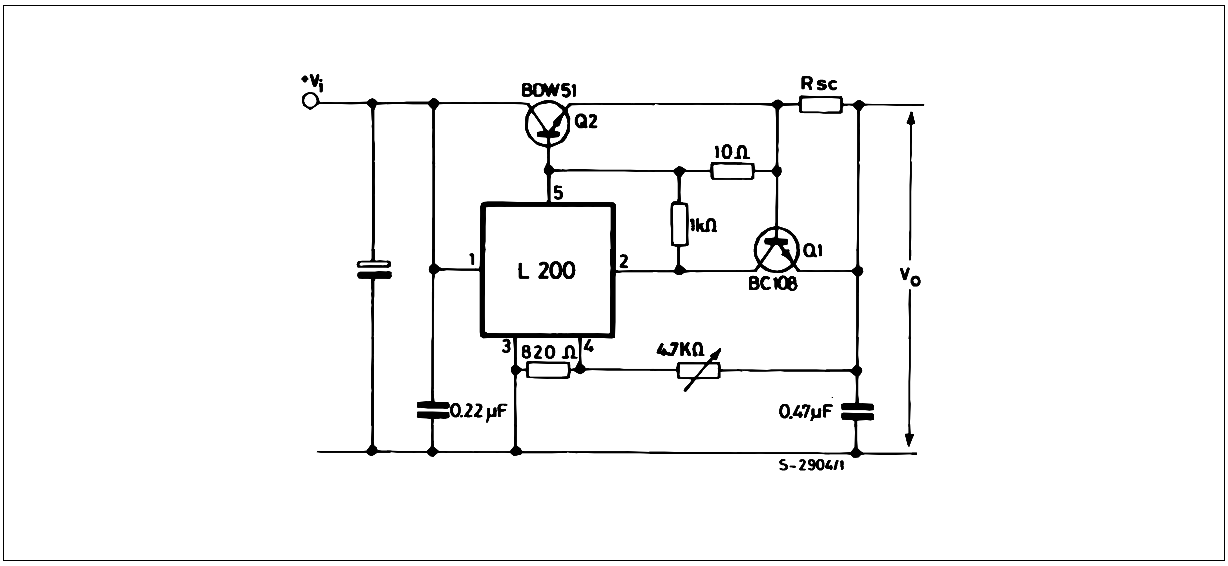
USE OF AN NPN POWER TRANSISTOR

Fig. 30 shows the same application as described in figure 29, using an NPN power transistor instead of a PNP. In this case an external signal transistor must be used to limit the current. Therefore :

$$I_o = \frac{V_{BE\ Q1}}{R_{SC}}$$

As regards the output shortcircuit, see par. 1.5.

Figure 30.



12V - 4A POWER SUPPLY

The diagram in fig. 31 shows a supply using the L200 and the BD705. The 1 kΩ potentiometer, PT1, together with the 3.3 k resistor are used for fine regulation of the output voltage.

Current limitation is of the type shown in fig. 32. Trimmer PT2 acts on strech AB of characteristic. With the values indicated (PT2 = 1 kΩ, PT3 = 470 Ω, R = 3 kΩ), currents from 3 to 4 A can be limited. The field of variation can be increased by increasing the value of R_{SC} or by connecting one terminal of PT to the base of the power transistor, which, however, provides less stable limitation. If section AB is moved, section BC will also be moved.

The slope of BC can be varied using PT3. The voltage level at point B is fixed by the voltage of the zener diode. The capacitor in parallel to the zener ensures correct switch-on with full load. The BD705 should always be used well within its safe operating area. If this is not possible two or more BD705s should be used, connected in parallel (fig. 33).

Further protection for the external power transistor can be provided as shown in fig. 34. The PTC resistor, whose temperature intervention point must prevent the T_j of the power transistor from reaching its maximum value, should be fixed to the dissipator near the power transistor. Dimensioning of R_A and R_B depends on the PTC used.

Figure 31.

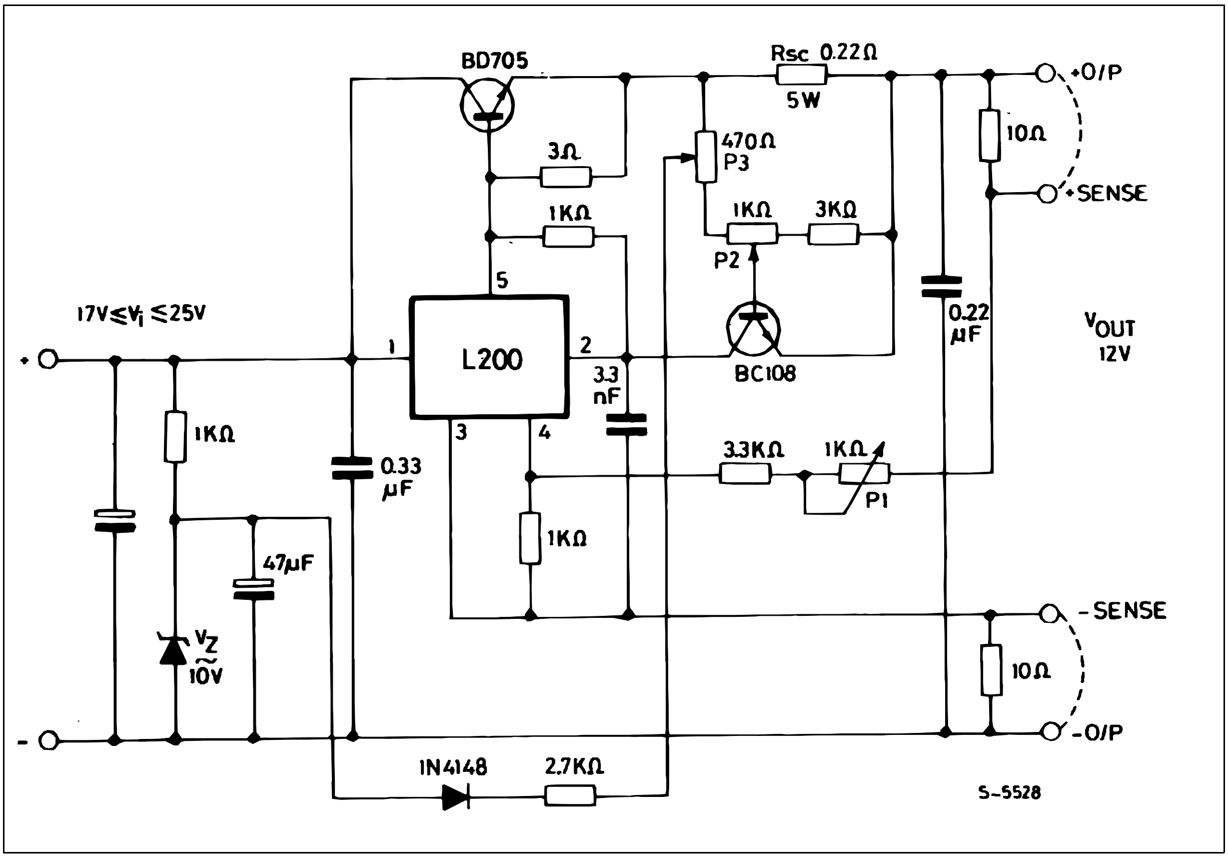


Figure 32.

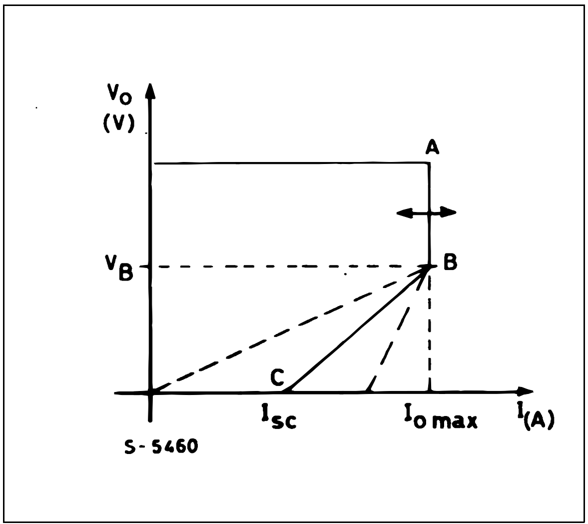


Figure 33.

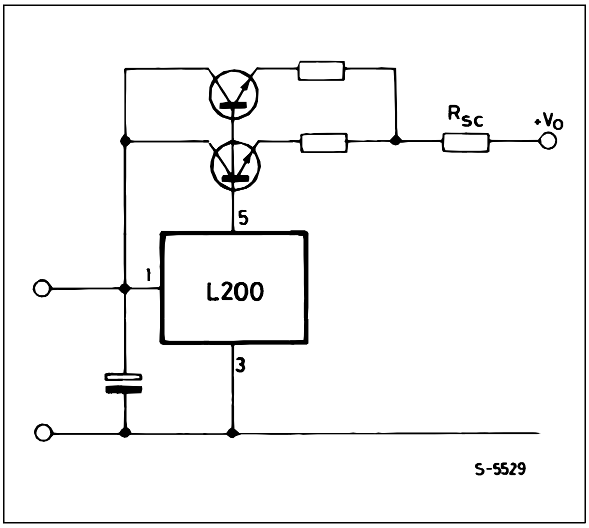
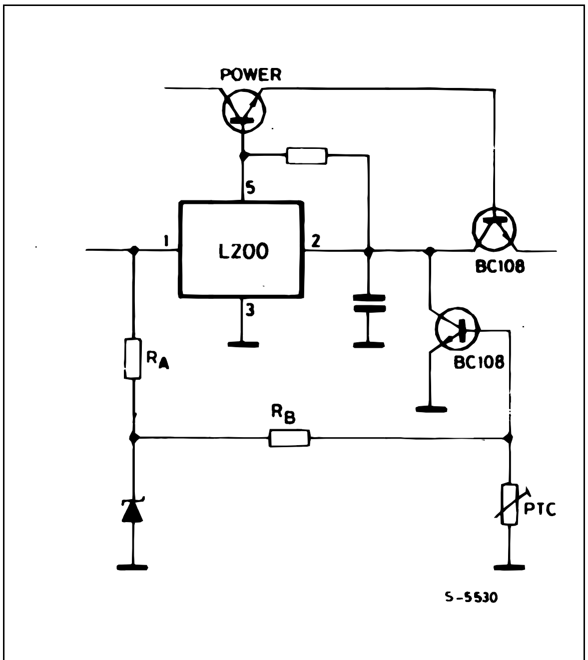


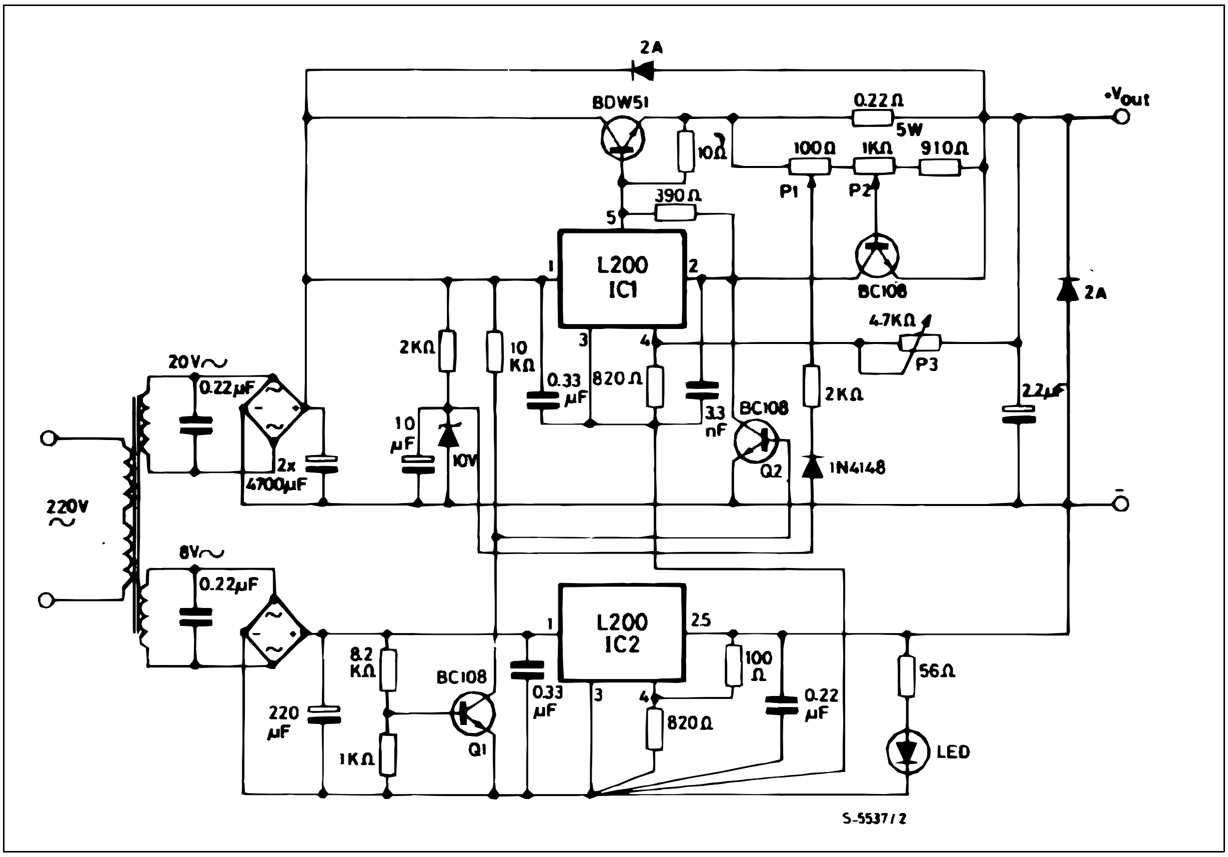
Figure 34.



VOLTAGE REGULATOR FROM 0V TO 16V - 4.5A

Fig. 35 shows an application for a high current supply with output voltage adjustable from 0 V to 16 V, realized with two L200 regulators and an external power transistor. With the values indicated, the current can be regulated from 2 A to 4.5 A by potentiometer PT2. PT1, on the other hand, is used for constant current or foldback current limitation. The integrated circuit IC2, which does not require a heatsink and has excellent temperature stability, is used to obtain the 0 V output. It is connected so as to lower pin 3 of IC1 until pin 4 reaches 0 V. Q1 and Q2 ensure correct operation of the supply at switch-on and switch-off.

Figure 35.



POWER SUPPLY WITH V_o = 2.8 TO 18 V, I_o = 0 TO 2.5 A

The diagram in fig. 36 shows a supply with output voltage variable from 2.8 V to 18 V and constant current limitation from 0 A to 2.5 A. The output current can be regulated over a wide range by means of the op. amp. and signal transistor TR_2. The op. amp. and the transistor are connected in the voltage-current converter configuration. The voltage is taken at the terminals of R3 and converted into current by PT_2.

I_o is fixed as follows :

$$\frac{R4\ I_o}{PT2} = I_1\ (*) \qquad (**)\ I_{sc} = \frac{V_{SC}}{R2}$$

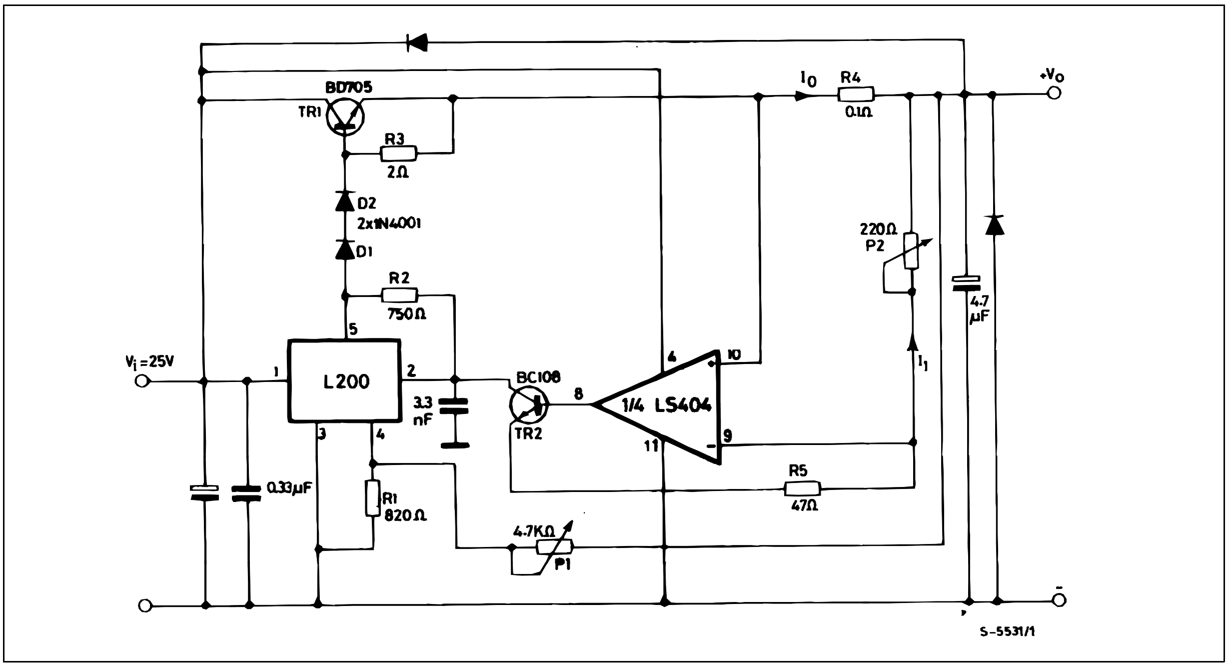
When $I_1 = I_{SC}$, the regulator starts to operate as a current generator. By making (*) equal to (**) we get :

$$\frac{R4\ I_o}{PT_2} = \frac{V_{SC}}{R2} \quad \text{Therefore} \quad I_o = \frac{VSC}{R2 \bullet R4} \bullet PT_2$$

Diodes D1 and D2 keep transistor TR_2 in linear condition in the case of small output currents. If it is not necessary to limit the current to zero, one of the diodes can be eliminated : the second diode could also be eliminated if TR_1 were a darlington instead of a transistor.

The op. amp. must have inputs compatible with ground in order to guarantee current limitation even in shortcircuit. With a negative voltage available, even of only &a few volts, current limitation is simplified.

Figure 36.



LAYOUT CONSIDERATIONS

The performance of a regulator depends to a great extent on the case with which the printed circuit is produced. There must be no impulsive currents (like the one in the electrolytic filter capacitor at the input of the regulator) between the ground pin of the device (pin 3) and the negative output terminal because these would increase the output ripple. Care must also be taken when inserting the resistor connected between pin 4 and pin 3 of the device.

The track connecting pin 3 to a terminal of this resistor should be very short and must not be crossed by the load current (which, since it is generally variable, would give rise to a voltage drop on this stretch of track, altering the value of V_{ref} and therefore of V_o.

When the load is not in the immediate proximity of the regulator output "+ sense" and " – sense" terminals should be used (see fig. 37). By connecting the "+ sense" and "– sense" terminals directly at the charge terminals the voltage drop on the connection cable between supply and load are compensated. Fig. 37 shows how to connect supply and load using the sensing clamps terminals.

Figure 37.

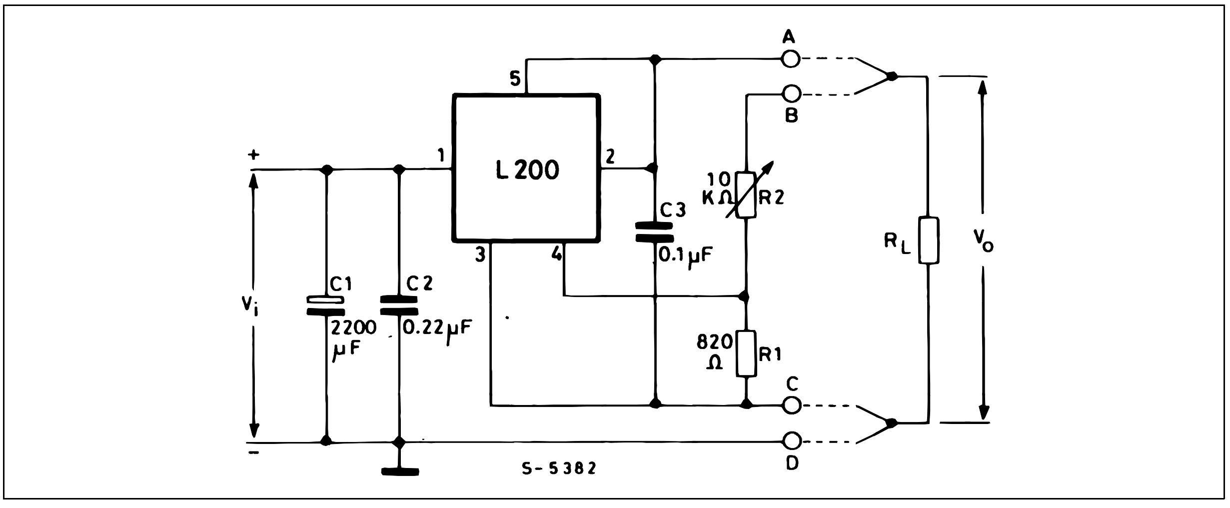
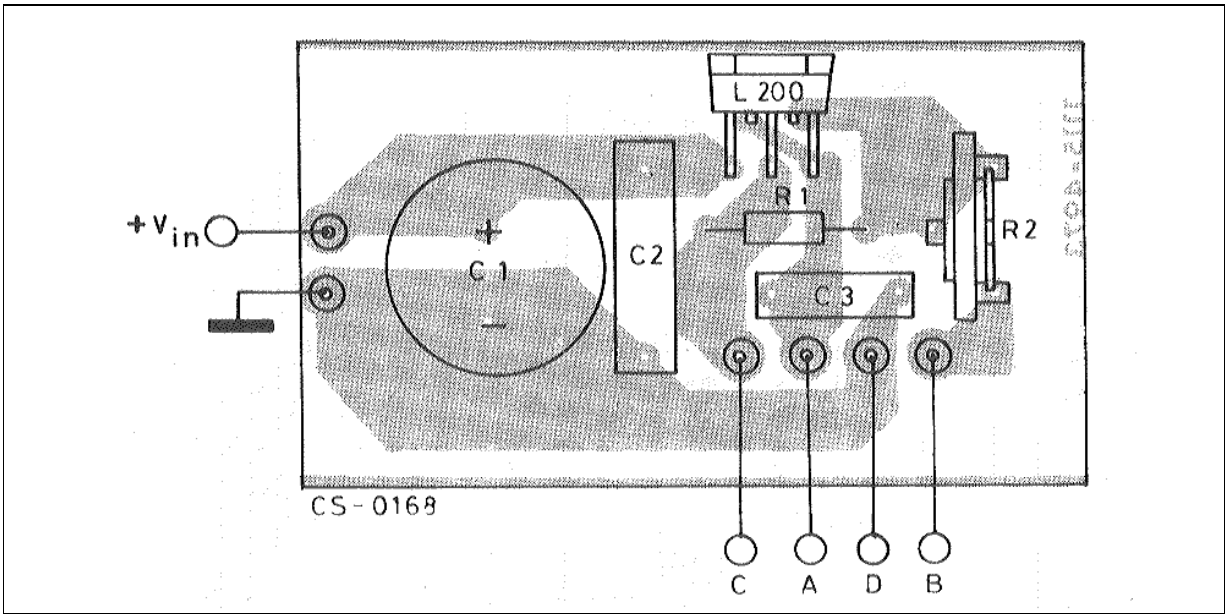


Figure 38.



HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching value which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150 °C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150 °C for long periods or of more than 170 °C for short periods (24 h). In any case the temperature accelerates the ageing process and therefore influences the device life ; an increase of 10 °C can halve the device life. A well designed heatsink should keep the junction temperature between 90 °C and 110 °C. Fig. 39 shows the structure of a power device. As demonstrated in thermodynamics, a thermal circuit can be considered to be an electrical circuit where R1, 2 represent the thermal resistance of the single elements (expressed in C/W) ;

Figure 39.

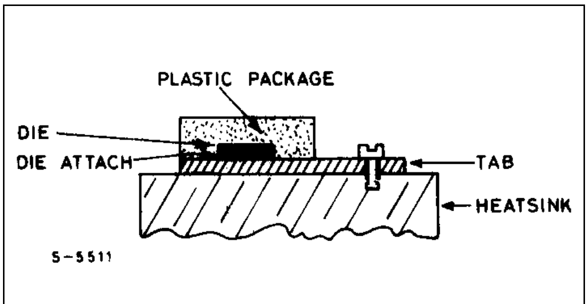
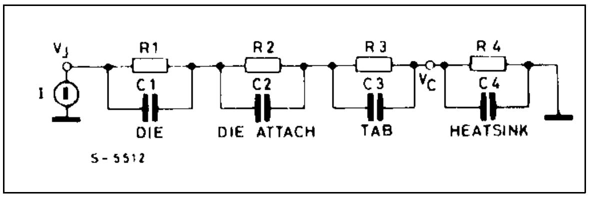


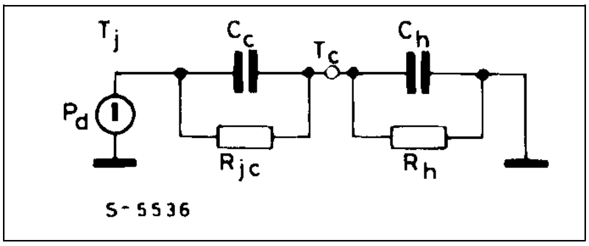
Figure 40.



C1, 2 the thermal capacitance (expressed in °C/W)
I the dissipated power
V the temperature difference with respect to the reference (ground)

This circuit can be simplified as follows :

Figure 41.

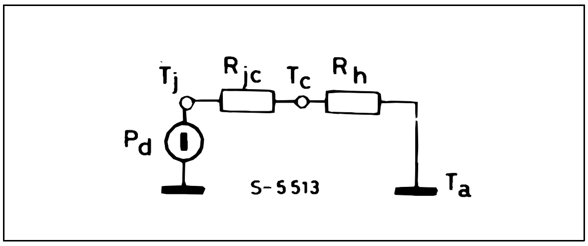


Where C_e is the thermal capacitance of the die plus that of the tab.

C_h is the thermal capacitance of the heatsink
R_{jc} is the junction case thermal resistance
R_h is the heatsink thermal resistance

But since the aim of this section is not that of studing the transistors, the circuit can be further reduced.

Figure 42.



If we now consider the ground potential as ambient temperature, we have :

$$T_i = T_a + (R_{jc} + R_h)\, P_D \qquad (1)$$

$$R_{th} = \frac{T_i - T_a - R_{IC} \bullet P_d}{P_d} \qquad (1a)$$

$$T_c = T_a + R_h \bullet P_d \qquad (2)$$

For example, consider an application of the L200 with the following characteristics :

$V_{in\ typ} = 20$ V
$V_o = 14$ V
Io typ = 1 A
$T_a = 40$ °C
— typical conditions

$V_{in\ max} = 22$ V
$V_o = 14$ V
$I_{o\ max} = 1.2$ A
$T_a = 60$ °C
— overload conditions

$P_{d\ typ} = (V_{in} - V_o) \bullet I_o = (2014) \bullet 1 = 6$ W

$P_{d\ max} = (2214) \bullet 1.2 = 9.6$ W

Imposing $T_j = 90$ °C of (1a) we get (from L200 characteristics we get $R_{jc} = 3$ °C/W).

$$R_h = \frac{90 - 40 - 3 \bullet 6}{6} = 5.3\ °C/W$$

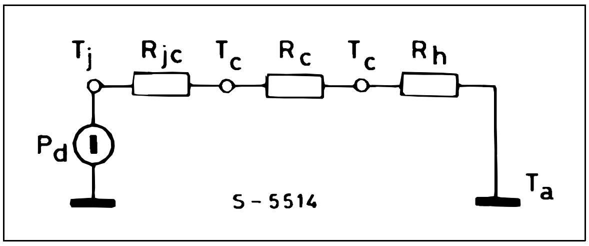
Using the value thus obtained in (1), we get that the junction temperature during the overload goes to the following value :

$$T_j = 60 + (3 + 5.3)\ .\ 9.6 = 140\ °C$$

If the overload occurs only rarely and for short periods, dimensioning can be considered to be correct. Obviously during the shortcircuit, the dissipated power reaches must higher values (about 40 W for the case considered) but in this case the thermal protection intervenes to maintain the temperature below the maximum values allowed.

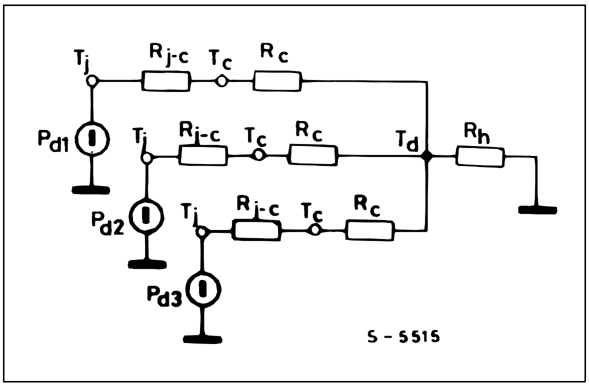
Note 1 : If insulating materials are used between device and heatsink, the thermal contact resistance must be taken into account (0.5 to 1 °C/W, depending on the type of insulant used) and the circuit in fig. 43 becomes :

Figure 43.



Note 2 : In applications where one or more external transistors are used together with the L200, the dissipated power must be calculated for each component. The various junction temperatures can be calculated by solving the following circuit :

Figure 44.



This applies if the various dissipating elements are fairly near to one another with respect to the heatsink dimensions, otherwise the heatsink can no longer be considered as a concentrated constant and the calculation becomes difficult.

This concept is better explained by the graph in fig. 45 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of dissipator and the same dissipated power. The graph in fig. 45 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the dissipated power and one the device geometry but we want to show that there exists an optimal position between the two devices :

$$d = \frac{1}{2} \bullet \text{side of the plate}$$

Fig. 46 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4).

This graph may be useful in applications with the L200 + external transistor (in which the transistor generally dissipates more than the L200) where the temperature of the L200 has to be kept as low as possible and especially where the thermal protection of the L200 is to be used to limit the transistor temperature in the case of an overload or abnormal increase in the ambient temperature. In other words the distance between the two elements can be selected so that the power transistor reaches the $T_{j\,max}$ (200 °C for a TO-3 transistor) when the L200 reaches the thermal protection intervention temperature.

Figure 45.

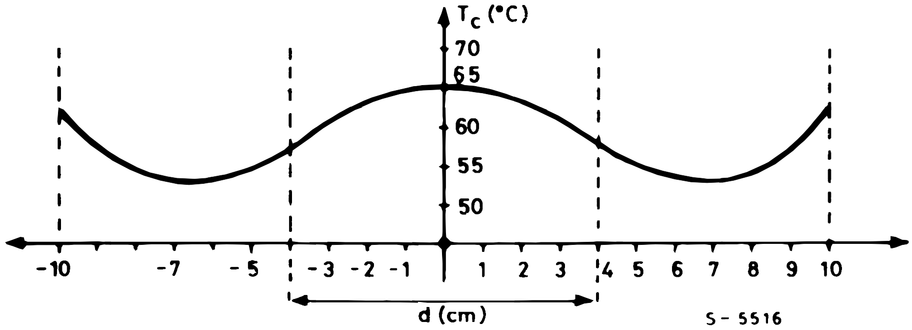
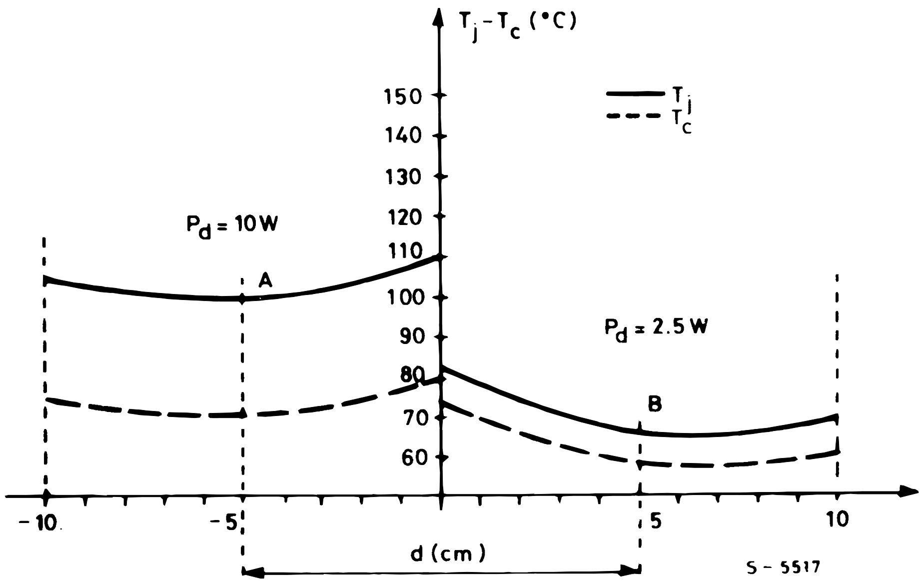


Figure 46.



A : Position of the device with high power dissipation (10 W)
B : Position of the device with low power dissipation (2.5 W)

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