Interleaved Zero-Current-Transition Buck Converter

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***Abstract*—This paper introduces interleaved zero-current-transition (ZCT) converters where two sets of switches are operating out-of-phase and share the load power equally. Turn-on transitions at zero current and a significant reduction of the losses associated with diode reverse recovery are accomplished through addition of two small inductors. This paper describes a 30-kW (300 V/100 A) interleaved ZCT buck converter operating at 32-kHz effective switching frequency. Losses and efficiency of the experimental prototype compare favorably against the standard and interleaved hard-switched buck converters. Constant frequency operation with low switching losses and low output current ripple is very well suited for the realization of dc power supplies in plasma processes.**

***Index Terms*—DC–DC power conversion, modeling, soft switching, zero-current transition (ZCT).**

I. Introduction

POWER semiconductor switches in high-power applications are subject to high switching stresses and switching losses, which limit the operation to relatively low switching frequencies. Various soft-switching techniques have been proposed to mitigate these problems [1]–[12]. In particular, zero-current transition (ZCT) [1], [2] and zero-voltage transition (ZVT) [10] techniques incorporate soft-switching functions into standard pulsewidth-modulated (PWM) converters, so that the switching losses can be reduced, ideally without increasing the switch-voltage or current stresses.

For high-power/high-voltage applications, insulated gate bipolar transistors (IGBTs) are preferred devices. Hence, ZCT techniques provide better results than ZVT techniques.

In the ZCT technique proposed in [1], an auxiliary circuit forces the switch current to zero prior to turn off, thus reducing the turn-off losses due to the current tailing of the IGBTs. However, the turn-on of the main switch is not affected by the auxiliary circuit. As a result, the turn-on losses caused by the diode reverse recovery remain significant. With the newest generation of IGBTs, which have greatly reduced the turn-off times and losses, the majority of losses in high-power and high-voltage applications are the switch turn-on and diode recovery losses (more than 75% of the total loss, as discussed in [13]).

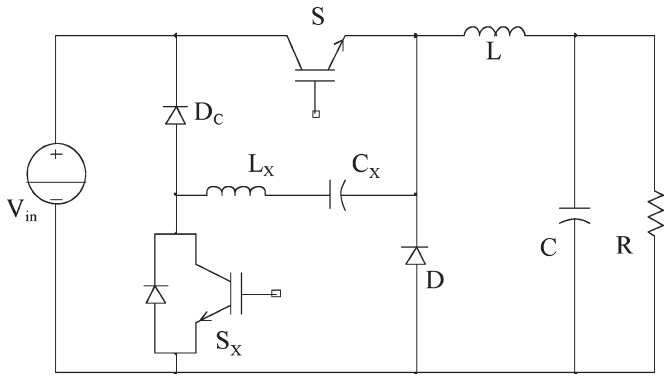

Fig. 1. ZCT buck converter proposed in [2].

The ZCT topology described in [1] can be improved to some degree with a modified control, as described in [12]. With this change, it is possible to get the auxiliary and main switches to turn on ideally at zero current. Disadvantages of this approach include a very high peak current in the auxiliary switch, increased conduction losses, and a more complicated control.

In the ZCT topology proposed in [2], which is shown in Fig. 1, the auxiliary circuit has been modified to reduce the high peak current problem and simplify the control timing of the auxiliary switch. The main and auxiliary switches are switched on and off under zero-current conditions so that the total switching losses can be significantly reduced (by around 80% compared to the hard-switched case, as described in [2]). These advantages are achieved at the expense of the auxiliary circuit consisting of a resonant tank, an increased main switch peak current, and an increased conduction loss: The resonant current flows through the main switch during the turn-off cycle. In addition, a more complicated control circuit is required to generate the appropriately timed drive signal for the auxiliary switch.

Interleaving technique has been widely used in power electronics [14]–[24]. In microprocessor power supplies, interleaved multiphase converters are commonly used in order to achieve better dynamic performance, lower current ripple, and lower losses per switch for an easier thermal design [14], [15]. In the context of power-factor-correction (PFC) rectifiers, interleaved boost converters have been proposed to reduce input current ripple, improve power scaling, and reduce switching losses [16]–[24]. In [18], it was shown that reverse-recovery losses can be greatly reduced in the interleaved boost converter with coupled inductors. Further soft-switching techniques applied to the interleaved boost converters for PFC applications can be found in [19]–[22]. It is also well known that the

IPCSD-07-046, presented at the 2006 IEEE Applied Power Electronics Conference and Exposition, Dallas, TX, March 19–23, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Power Converter Committee of the IEEE Industry Applications Society. Manuscript submitted for review April 30, 2006 and released for publication June 8, 2007.

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Digital Object Identifier 10.1109/TIA.2007.908175

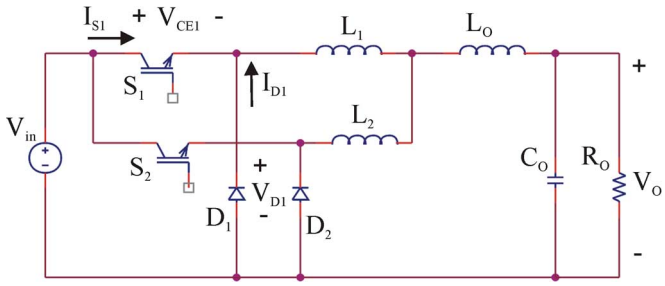

Fig. 2. Interleaved ZCT buck converter proposed in this paper.

operation in discontinuous conduction mode (DCM) [23] or critical conduction mode [24] can lead to elimination of diode reverse recovery losses at the expense of increased inductor current ripples.

In this paper, the objectives are to facilitate relatively high-frequency operation by addressing the diode reverse recovery losses in high-power step-down (buck) dc–dc applications. In particular, the focus is on plasma power supplies in physical vapor deposition applications, which require low-ripple, constant-frequency, and constant current operation over a wide range of output voltages and power [25], [26]. We propose a simple ZCT scheme [26], which addresses the switch turn-on and diode recovery losses using an interleaved buck converter configuration with small auxiliary inductors, as shown in Fig. 2. In this scheme, which is similar to the approaches described in [18] and [20] for the boost PFC rectifier applications, there is no need for a resonant tank with circulating currents, and the control of the switches is very simple. Compared with the hard-switched PWM converters, the switch voltage and current stresses are not increased, and there are no significant restrictions on the range of operating duty ratios. Compared with the standard hard-switched PWM converter, each switch operates at two times lower switching frequency and conducts half of the time. Furthermore, both switches in the interleaved ZCT configuration participate in the power processing function of the converter and share the power equally. The small auxiliary inductors L_1 and L_2 enable the ZCT turn-on and reduced switching losses, whereas the larger inductor L_0 results in a continuous conduction mode (CCM) of operation with good average current sharing and low current ripple, which is well suited for plasma power supplies.

This paper is organized as follows. Operation of the interleaved ZCT buck converter is described in Section II, including ideal waveforms as well as nonideal effects of the residual diode reverse recovery currents. Steady-state and dynamic models are derived in Section III using the averaged switch modeling technique. Design guidelines related to the selection of the switches and the auxiliary inductors are discussed in Section IV. Section V presents an experimental 30 kW (300 V/100 A) interleaved ZCT buck converter, together with a loss analysis comparing the achieved results with the standard hard-switched buck converter, the interleaved CCM buck, the interleaved critical DCM (CDCM) buck, and the ZCT technique described in [2]. Conclusion is presented in Section VI.

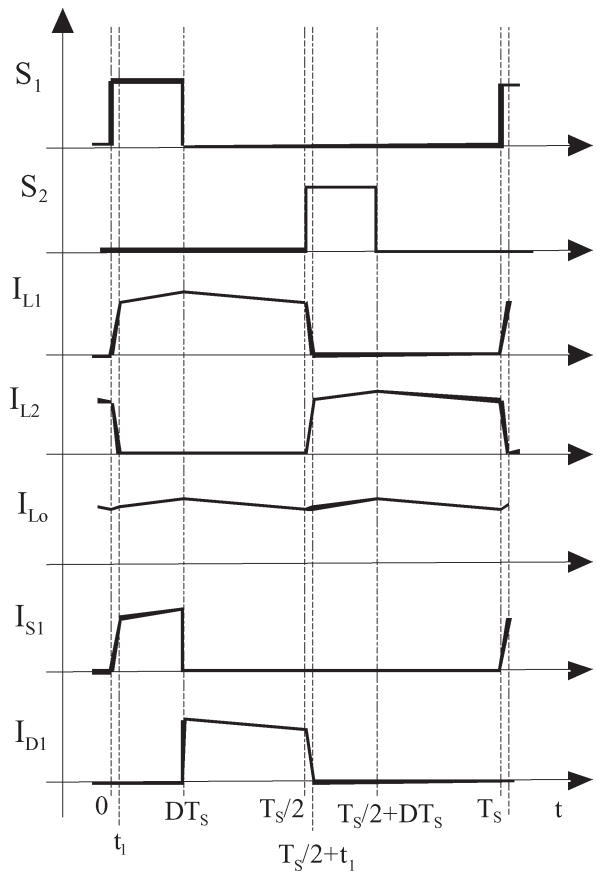

Fig. 3. Interleaved ZCT-buck-converter waveforms.

II. Interleaved ZCT-Circuit Topology

The interleaved ZCT buck converter is shown in Fig. 2. The circuit can be derived from the standard buck converter where two pairs of switches (S_1/D_1 and S_2/D_2) are connected in parallel. The key modifications include the addition of two small inductors L_1 and L_2 and the phase-shifted operation of the two stages. The phase-shifted interleaved operation is the same as the operation of switches in multiphase converters commonly applied in microprocessor power supplies [14], [15] or in the interleaved boost PFC rectifiers [16]–[24].

To explain the operation of the interleaved ZCT converter, we assume that the auxiliary inductors L_1 and L_2 are identical ($L_1 = L_2 = L$), the output inductance L_o is much larger than L_1 and L_2, the phase shift between the switches S_1 and S_2 is 180°, and the duty cycle for each switch is less than 0.5.

A. Ideal Interleaved ZCT-Circuit Operation

Typical waveforms in the interleaved ZCT buck converter are shown in Fig. 3. During one switching period, the circuit goes through six different stages, which are listed in the following sections.

1) S_1 Turn-On Transition ($0 < t < t_1$): Prior to $t = 0$, D_1 is off, and D_2 and L_2 conduct the current equal to the main inductor current I_{Lo}. This assumption will be discussed in more detail later. At $t = 0$, the switch S_1 turns on at zero current. The current commutates from L_2 to L_1 with the slope $V_{\mathrm{in}}/(L_1 + L_2)$, where V_{in} is the input voltage. This transition is finished at

$t = t_1$ when the inductor L_2 current drops to zero and the diode D_2 turns off

$$t_1 = \frac{I_{\mathrm{Lo}}(L_1 + L_2)}{V_{\mathrm{in}}}. \tag{1}$$

By choosing the inductances L_1 and L_2, we can control the current slope during the transition and, therefore, reduce the losses associated with the reverse recovery of D_2 (note that, here, we assumed the ideal case: there is no reverse current through the diode D_2). During this interval, the main inductor current changes with the slope

$$\frac{V_{\mathrm{in}}/2 - V_{\mathrm{o}}}{L_{\mathrm{o}}} = \frac{V_{\mathrm{in}} - 2V_{\mathrm{o}}}{2L_{\mathrm{o}}}. \tag{2}$$

2) Switch S_1 on Stage ($t_1 < t < DT_{\mathrm{S}}$): In this interval, the current flows through the inductor L_1 and the main inductor L_{O}. The current increases with the slope

$$\frac{V_{\mathrm{in}} - V_{\mathrm{o}}}{L_{\mathrm{o}} + L_1} \approx \frac{V_{\mathrm{in}} - V_{\mathrm{o}}}{L_{\mathrm{o}}} \tag{3}$$

where V_{o} is the output voltage. This interval ends when the switch S_1 turns off at DT_{S}.

3) S_1 Turn-Off Transition and Off Stage ($DT_{\mathrm{S}} < t < T_{\mathrm{S}}/2$): When the switch S_1 turns off, the diode D_1 turns on to conduct the main inductor current; during this interval, the inductor current is decreasing with the slope $V_{\mathrm{o}}/(L_{\mathrm{o}} + L_1) \approx V_{\mathrm{o}}/L_{\mathrm{o}}$. For $L_{\mathrm{O}} \gg L_1$, the voltage across L_1 is approximately zero. This means that the voltage across L_2 is also very close to zero, and the current through L_2 and D_2 remains zero. This interval ends when the switch S_2 turns on at $T_{\mathrm{S}}/2$.

4) S_2 Turn-On Transition ($T_{\mathrm{S}}/2 < t < T_{\mathrm{S}}/2 + t_1$): The switch S_2 turns on at zero current, and in addition, losses due to the reverse recovery of D_1 are practically eliminated. This stage is the same as the stage in Section II-A1, except that the switch S_2 turns on and that the diode D_2 current is zero. By controlling the current slope during the transition (by choosing L_1 and L_2), we control the losses associated with the reverse recovery of D_1.

5) Switch S_2 on Stage and S_2 Turn-Off Transition and Off Stage: These stages are the same as the stages in Sections II-A2 and A3, except that the roles of the elements S_1, D_1, and L_1 are played by the elements S_2, D_2, and L_2, and vice versa. At the end of the S_2 turn-off transition, D_1 is off, and the circuit is ready for the next S_1 turn-on transition at zero current.

In the ZCT buck converter, the two switches are ideally operated at the same duty cycle. Since both switches use the same relatively large output inductor L_0, any duty-cycle mismatches would result in only small mismatches in the average switch currents. As a result, nearly equal average-current sharing between the two switches is accomplished automatically, which is consistent with the results reported in [18] for the interleaved boost converters.

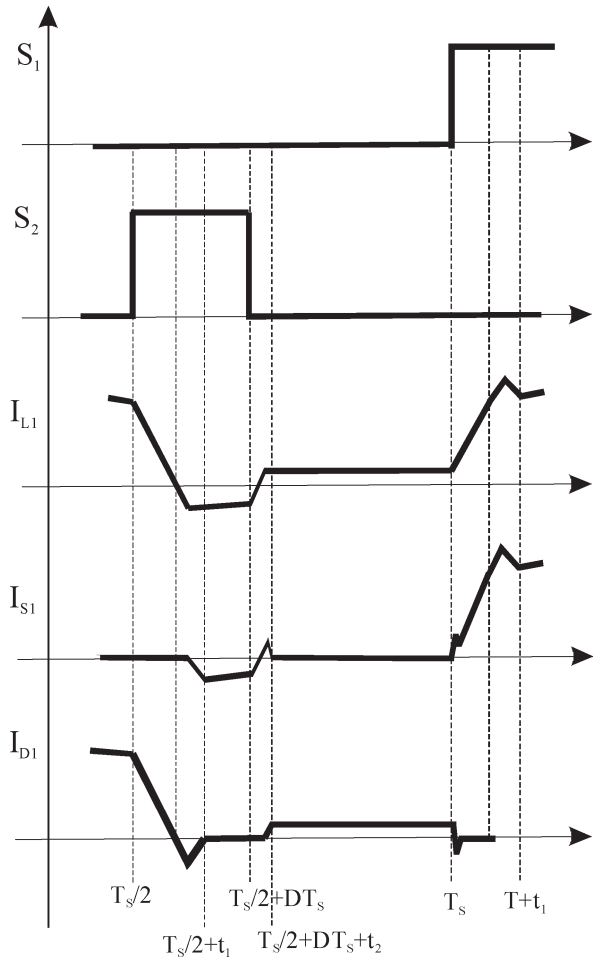

Fig. 4. Characteristic waveforms with diode reverse recovery.

B. Interleaved ZCT-Circuit Operation With Nonideal Diode Reverse Recovery

In a practical and experimental circuit, the values for L_1 and L_2 are chosen to be large enough to greatly reduce the losses associated by the reverse recovery of the diodes, yet small enough so that there are no significant restrictions on the range of operating duty ratios, i.e., $t_1 \ll T_{\mathrm{S}}$. At relatively high switching frequencies (e.g., 32 kHz in the experimental prototype described in Section V), a practical choice for L_1 and L_2 results in a small negative current through the diode upon reverse recovery. The operating waveforms differ slightly from the idealized waveforms shown in Fig. 3, but the impact on practical circuit design and efficiency can be significant. This case was not considered for the interleaved boost circuits discussed in [18] and [20]. The waveforms shown in Fig. 4 illustrate the operation with nonideal reverse recovery. The analysis is presented in detail for one switch/diode pair; the second pair has the same behavior.

Let us consider the case when the switch S_2 turns on and the diode D_1 goes through the recovery process. During one half of the switching period, the circuit goes through five different stages, which are listed in the following sections.

1) S_2 Turn-On Transition ($T_{\mathrm{S}}/2 < t < T_{\mathrm{S}}/2 + t_1$): Prior to $t = T_{\mathrm{S}}/2$, D_1 and L_1 conduct the current equal to the main inductor current I_{Lo}. At $t = T_{\mathrm{S}}/2$, the switch S_2 turns on. The

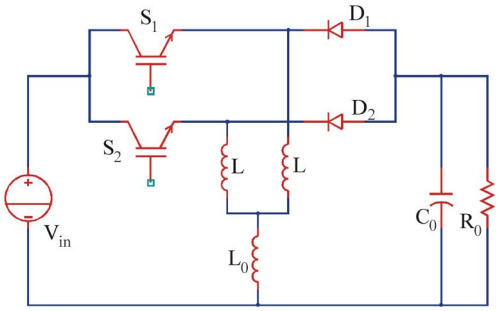

Fig. 5. Interleaved ZCT buck–boost converter.

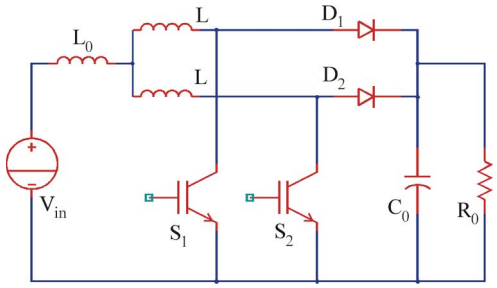

Fig. 6. Interleaved ZCT boost converter.

current commutates from L_1 to L_2, and the diode D_1 goes through the recovery process. We assume that there is some relatively small negative reverse current through D_1 (typically, 5%–10% of the nominal diode current).

After the D_1 recovery process is completed, the small current through L_1 continues to flow, which forces the conduction of the antiparallel diode across the switch S_1, as shown in Fig. 4. This interval ends when the diode D_1 is completely recovered.

2) Switch S_2 on Stage $(T_S/2 + t_1 < t < T_S/2 + DT_S)$*:* In the circuit consisting of S_2, L_2, L_1, and the antiparallel diode of S_1, the voltage drops are small, which means that the current through L_1 may still flow when S_2 is turned off. This case is considered here, and it is illustrated by the waveforms shown in Fig. 4.

3) S_2 Turn-Off Transition $(T_S/2 + DT_S < t < T_S/2 + DT_S + t_2)$*:* When S_2 turns off, the inductor L_2 current forces conduction of the diode D_2, and at the same time, the reverse-recovery process of the S_1 antiparallel diode occurs. The antiparallel diode will be recovered with the same current slope as the main diodes $V_{in}/(L_1 + L_2)$. This interval ends when the antiparallel diode is completely recovered. After the antiparallel diode recovery is completed, the small current that is still flowing through L_1 forces conduction of the diode D_1.

4) S_2 Turn-Off Stage $(T_S/2 + DT_S + t_2 < t < T_S)$*:* In this stage, the majority of the main inductor current flows through the inductor L_2, and a much smaller portion flows through the inductor L_1. If the main inductor current stays constant during this interval, then in the circuit consisting of D_2, L_2, L_1, and D_1, the voltage drops are small, which means that the current through L_1 may still flow when S_1 is turned on. This worst-case situation is assumed in our analysis.

5) S_1 Turn-On Transition $(T_S < t < T_S + t_1)$*:* At $t = T_S$, the switch S_1 turns on. The current commutates from L_2 to L_1, and the diode D_2 goes through the recovery process (with the controlled current slope). In addition, because of the small residual current flowing through D_1 and L_1 prior to the switch S_1 turn-on, a small additional loss occurs because of the abrupt reverse recovery of D_1. This small additional loss is the main difference in the converter operation compared with the ideal case shown by the waveforms in Fig. 3.

The amount of the residual current through D_1, and therefore the additional turn-on loss, can be controlled by the choice of the auxiliary inductances L_1 and L_2. There is a practical tradeoff between the additional turn-on losses and the lengths of time allocated for the turn-on transitions. Larger L_1 and L_2 result in smaller residual currents, but the transition times are longer. Design considerations are discussed in more detail in Section III.

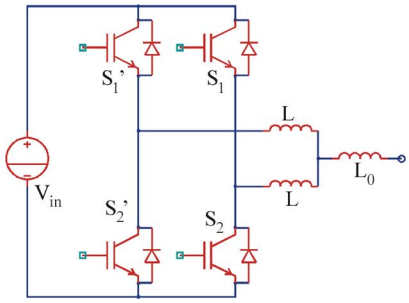

Fig. 7. One leg of an interleaved ZCT three-phase inverter.

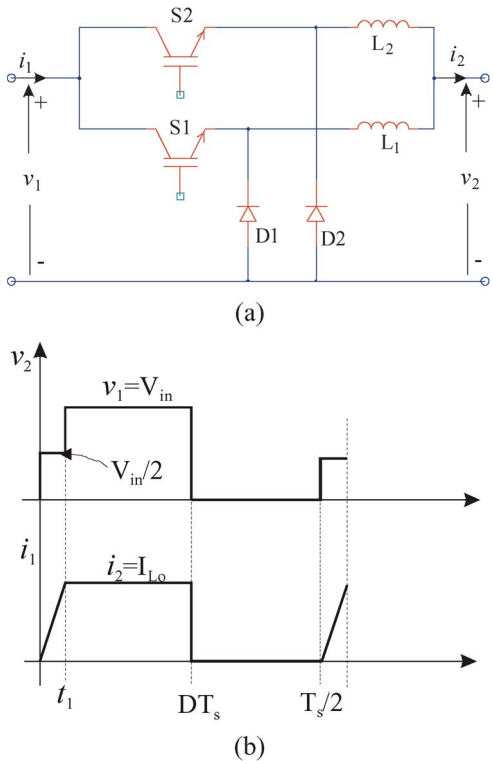

Fig. 8. (a) Switch network for the interleaved ZCT buck converter. (b) Switch-network terminal waveforms.

C. Applications of the Interleaved ZCT Circuit

The interleaved ZCT switch topology shown in Fig. 2, in the context of a buck converter, can be used as an interleaved

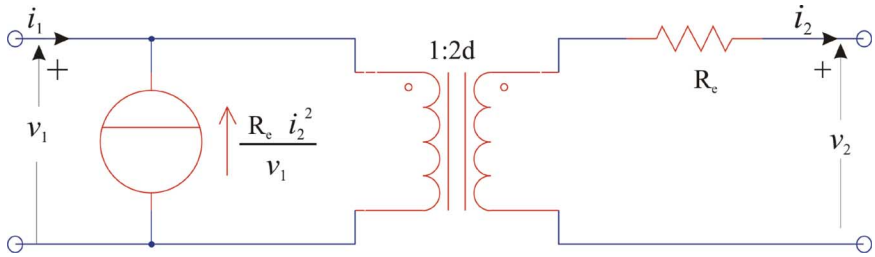

Fig. 9. Large-signal nonlinear averaged switch model for the switch network of the interleaved ZCT buck converter.

ZCT switch cell in other PWM converters. For example, Figs. 5 and 6 show the interleaved ZCT buck–boost converter and the interleaved ZCT boost converter, respectively.

The proposed interleaved ZCT topology is equally applicable to the bridge-type converters. For example, Fig. 7 shows one leg of a three-phase interleaved ZCT inverter. In this case, additional simple control circuitry is required to send PWM pulses first to S_1 (or S_2) and then in the next cycle to S_1' (or S_2'). With the addition of two small inductors and the switches operated out-of-phase, the interleaved ZCT legs applied to a bridge or a three-phase inverter result in zero-current turn-on for all switches, significantly reduced diode-recovery losses, and power sharing between the switches.

The bridge configuration can be compared to the auxiliary-resonant-commutated-pole topologies [11], [12] and the ZCT topologies [4], [6]. The interleaved ZCT technique does not rely on a resonant circuit and may allow shorter commutation times. In addition, the power sharing between the branches in the interleaved ZCT configuration may be preferable for thermal design.

It is clear that the proposed topology can be extended to more than two switches. In the general case of n switches, n small auxiliary inductors are used to achieve the ZCT turn-on with reduced reverse-recovery losses. The switches are phase-shifted by $2\pi/n$, and they operate with equal duty cycles up to $1/n$ to achieve a full output-voltage range. An extension to multilevel configurations is discussed in [28].

III. Averaged Switch Model of the Interleaved ZCT Buck Converter

A steady-state dc conversion ratio and a small-signal dynamic model are derived in this section based on the standard averaged switch-modeling approach. Fig. 8(a) shows a convenient definition of the switch network in the interleaved ZCT buck converter.

From the description of the converter operation in Section II and the operating waveforms in Fig. 3, we find the switch-network waveforms $\nu_2(t)$ and $i_1(t)$, as shown in Fig. 8(b). Since the waveforms from $T_S/2$ to T_S are the same, the averaging can be performed over the interval from 0 to $T_S/2$. Our objective is to express the averaged quantities $\langle\nu_2\rangle$ and $\langle i_1\rangle$ as functions of $\langle\nu_1\rangle$ and $\langle i_2\rangle$, and the switch duty cycle $d(t)$. Note that the "$\langle\ \rangle$" sign denotes the averaging of a quantity over a switching period. From Figs. 3 and 8, it follows that $\langle\nu_1\rangle = \langle\nu_{in}\rangle$ and $\langle i_2\rangle = \langle i_{Lo}\rangle$.

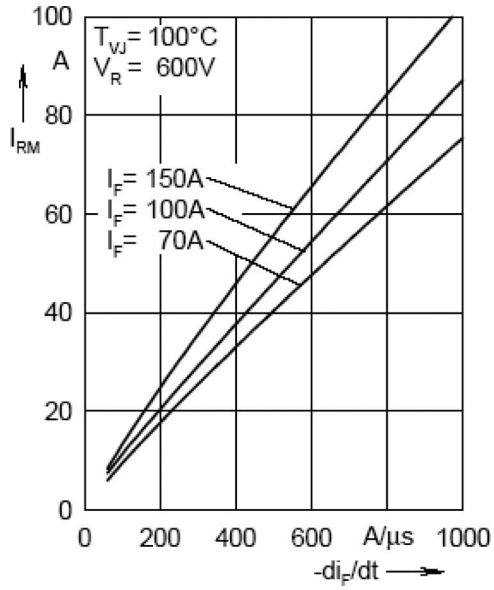

Fig. 10. Typical reverse-recovery data for 1200-V ultrafast diode.

The transition time t_1 [found in (1)] can be rewritten as

$$t_1 = \frac{2L\langle i_2\rangle}{\langle\nu_1\rangle}. \tag{4}$$

Then, the expressions for $\langle\nu_1\rangle$ and $\langle i_2\rangle$ can be written as

$$\begin{aligned}\langle\nu_2\rangle &= 2d\langle\nu_1\rangle - \frac{2L}{T_S}\langle i_2\rangle \\ \langle i_1\rangle &= 2d\langle i_2\rangle - \frac{2L}{T_S}\frac{\langle i_2\rangle^2}{\langle\nu_1\rangle}.\end{aligned} \tag{5}$$

Using (5) and defining R_e as $R_e = 2L/T_S$, a large-signal time-invariant averaged circuit model is obtained for the switch network, as shown in Fig. 9.

The contribution of the two small inductors and the interleaving is represented by the additional resistance R_e (in series with the output terminal) and one additional controlled source that is dependent on the input voltage, the output current, and the resistance R_e.

Using the large-signal model in Fig. 9, we can derive the dc conversion ratio $M(D)$

$$M(D) = \frac{V_o}{V_{in}} = \frac{2D}{1 + \frac{R_e}{R_o}}. \tag{6}$$

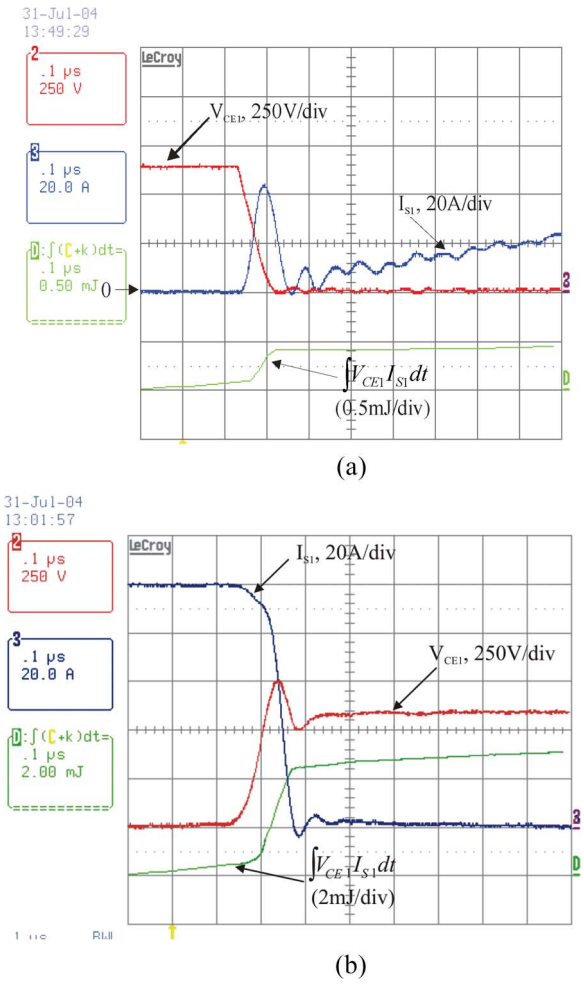

Fig. 11. Switch S_1 losses. (a) Turn-on loss: 0.4 mJ. (b) Turn-off loss: 4.0 mJ.

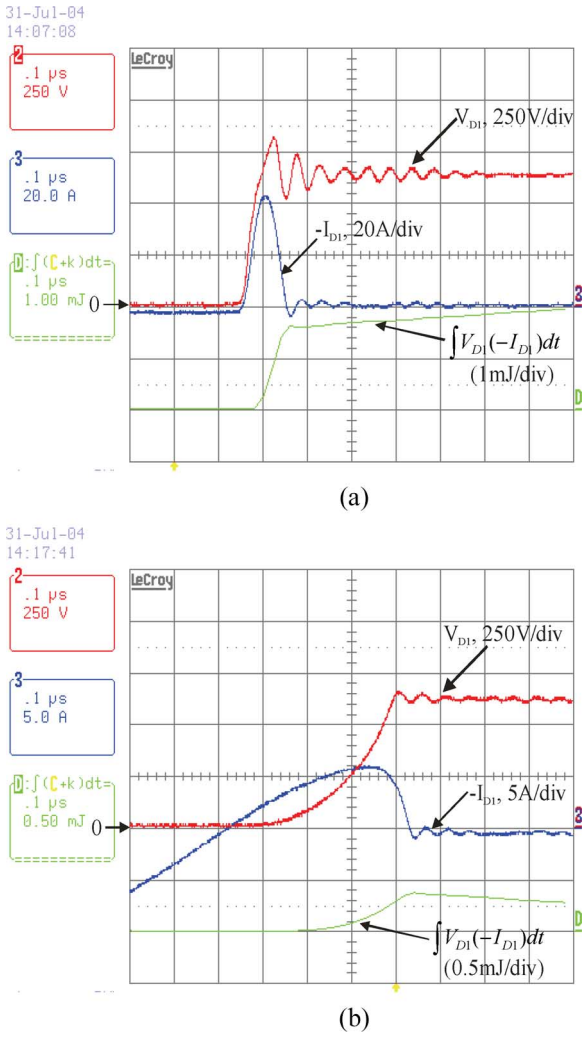

Fig. 12. Diode D_1 loss. (a) During the S_1 turn-on: 1.6 mJ. (b) During the S_2 turn-on: 0.4 mJ.

Since the auxiliary inductors are chosen such that the transition time is much smaller than the switching period, in a practical circuit, the value of the resistance R_e is relatively small compared with the load resistance R_o. Therefore, the steady-state conversion ratio (6) can be approximated by

$$M(D) \approx 2D. \tag{7}$$

Equation (7) shows that the full range of dc conversion ratios $0 < M(D) < 1$ can be obtained by operating each switch with the duty ratios in the range from 0 to $D = 0.5$. There is no need to operate the converter switches with duty ratios above 0.5.

Perturbation and linearization of the model in Fig. 9 give a small-signal averaged circuit model described in [29]. The small-signal model shows that the ZCT waveforms result in significant lossless damping in the converter frequency responses compared with the frequency responses of the standard PWM buck converter. Application of the small-signal model in the design of a digital current-mode controller around the ZCT power stage has been described in [26].

In DCM, the filter inductor current drops to zero before the end of the diode (D_1 or D_2) conduction. As a result, there are no transition intervals, and the interleaved ZCT buck converter operates in exactly the same way as the standard PWM buck converter.

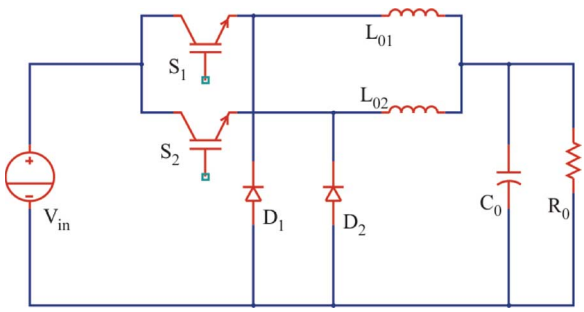

Fig. 13. Interleaved hard-switched buck converter.

IV. Interleaved ZCT-Circuit Design Considerations

In this section, we discuss circuit design considerations as related to the selection of the switches and the auxiliary inductors.

As described in Section II-A, the inductances L_1 and L_2 control the current slopes during the transitions and, therefore, affect the losses associated with the reverse recovery. In addition, the amount of the residual diode current, and therefore the additional turn-on losses, can also be controlled by the choice of the auxiliary inductances L_1 and L_2, as described in

TABLE I
ESTIMATED LOSSES FOR THE HARD-SWITCHING CONVERTERS, THE ZCT [2], AND THE INTERLEAVED ZCT CIRCUIT PROPOSED IN THIS PAPER

Powerex: CM150DU-24NFH		Hard switched buck	Circuit [2]	Proposed circuit	Interleaved CDCM Buck	Interleaved CCM Buck
Turn-on loss	(mJ)	3.8	0.4	0.4	0.0	2.5
Turn off loss	(mJ)	4.0	0.4	4.0	4.1	0.0
Conduction loss (one sw. period)	(mJ)	6.1	7.4	6.1	5.7	4.9
Loss per switch	(W)	444.2	263.0	168.0	156.8	118.4
Diode recovery loss	(mJ)	12.0	1.2	2.0	0.0	6.1
Diode conduction loss (one sw. per.)	(mJ)	4.0	4.1	4.0	3.6	3.3
Diode loss	(W)	512.0	169.6	96.0	57.6	150.4
Aux switch, eq 10* [2]	(mJ)		2.8			
Total loss (32kHz)	(W)	956.2	522.2	528.0	428.8	537.6

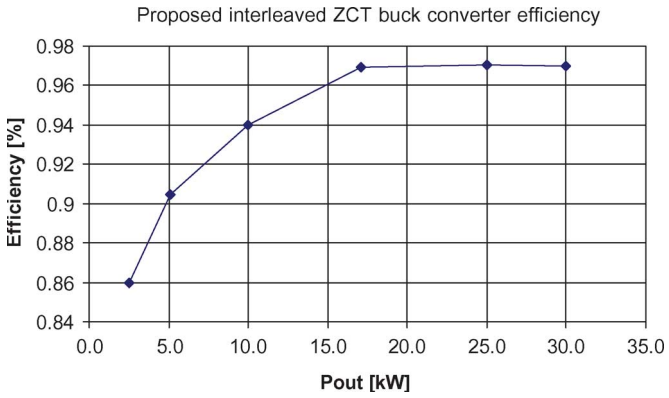

Fig. 14. Measured efficiency of the experimental ZCT buck converter as a function of the output power.

Section II-B. Larger L_1 and L_2 result in smaller reverse-recovery and residual currents, but the transition times are longer. This tradeoff, which is related to the switching frequency, the loss of the duty-cycle control range, and the total power loss, is discussed in more detail here, using our experimental circuit as example.

In our application, the circuit is designed so that the residual current due to the nonideal reverse recovery amounts to about 5% of the nominal current through the diodes. To accomplish this design goal, the first step is to check the reverse-recovery waveforms for the selected devices. For the device in the experimental prototype (1200 V/150 A ultrafast diode), the reverse-recovery characteristics are shown in Fig. 10.

In the experimental circuit with the output current of 100 A, the residual current of 5% (or 5 A) is obtained by noting that the required current slope (di/dt) is around 40–50 A/μs.

Given that $V_{\rm in} = 600$ V, $V_{\rm out} = 300$ V, and $I_{\rm out} = 100$ A, we select $L_1 = L_2 = 8.5$ μH, which results in the current slope of 35 A/μs during the turn-on transitions, the transition lengths of approximately 2.8 μs at nominal load, and the reverse-recovery current of approximately 5–6 A. This value has been confirmed by measurements in the experimental circuit.

We conclude that relatively fast and high switching frequencies are possible, while preserving the benefits of near-zero-current switching at turn-on, and that additional turn-on losses are almost negligible due to the residual reverse-recovery currents.

It is worth noting that the interleaved ZCT circuit may lose the zero-current turn-on at very low duty cycles. Knowing that, in most cases, a low duty cycle is required only at low output currents, the loss associated with the loss of zero-current switching is not a significant concern. This is an additional advantage compared with the ZCT approach described in [2].

In the interleaved ZCT configuration, the switches handle half of the output power with significantly lower losses. Taking into account the current/voltage ratings and thermal issues, although each of the two switches has to be rated at full output current, it may be possible to use smaller transistors compared with the standard hard-switched configuration or with the alternative ZCT schemes. This point is discussed further in the next section.

V. EXPERIMENTAL RESULTS

The interleaved ZCT buck converter in Fig. 2 has been used to construct a 30 kW (300 V/100 A) power supply. Powerex 150 A/1200 V IGBT (CM150DU-24NFH) devices [30] are used for the main switches. Each switch operates at 16 kHz switching frequency. Therefore, the effective switching frequency is 32 kHz. The output filter components are $L_0 =$ 300 μH (hence, the output inductor current ripple is very small) and $C_0 = 1$ μF.

Experimental waveforms for the turn-on and the recovery losses in the interleaved ZCT-buck-converter prototype are given in Figs. 11 and 12, respectively. The measured switch turn-on loss [Fig. 11(a)] is 0.4 mJ, and the turn-off loss is 4.0 mJ [Fig. 11(b)]. In order to measure the switch current, a piece of wire was added between the input dc voltage bus and the IGBT collector. The added parasitic inductance resulted in voltage overshoots ($\sim$750 V) across the switch and slightly increased turn-off loss. The diode loss due to the residual current is 1.6 mJ [Fig. 12(a)], and the diode-recovery loss for the low di/dt recovery is 0.6 mJ [Fig. 12(b)]. The total diode-recovery losses amount to 2 mJ. To compute the corresponding power losses, note that the switching frequency for each switch is only 16 kHz.

It is of interest to compare the proposed solution with the ZCT technique described in [2], the standard hard-switched buck converter, and the interleaved hard-switched buck converter, shown in Fig. 13, operating in CCM or CDCM. In all cases, the effective switching frequency is the

TABLE II
COMPONENT RATINGS: ZCT BUCK [2] AND THE PROPOSED INTERLEAVED ZCT BUCK

	Component	Peak current [A]	Average current [A]	Loss [W]
Circuit [2]	main switch	260	51	263
	aux switch	151	8	89.6
Proposed interleaved ZCT circuit	main switch S1	107	25	168
	main switch S2	107	25	168

same—32 kHz. Operating conditions for each topology are the following.

1) Hard-switched buck converter: $V_{\rm in} = 600$ V, $L_0 = 300$ μH, $C_0 = 1$ μF, $V_0 = 300$ V, $P_0 = 30$ kW, and one IGBT switch operates at 32 kHz.
2) ZCT technique described in [2]: $V_{\rm in} = 600$ V, $L_0 = 300$ μH, $C_0 = 1$ μF, $V_0 = 300$ V, $P_0 = 30$ kW, $L_{\rm X} = 1.5$ μH, $C_{\rm X} = 150$ nF, the main IGBT operates at 32 kHz, and the auxiliary switch operates at 64 kHz.
3) Proposed interleaved ZCT buck converter: $V_{\rm in} = 600$ V, $L_0 = 300$ μH, $C_0 = 1$ μF, $V_0 = 300$ V, $P_0 = 30$ kW, $L_1 = L_2 = 8.5$ μH, and two IGBTs, each operates at 16 kHz. All parameters are the same as in the experimental prototype.
4) Hard-switched interleaved buck converter operating in CCM: $V_{\rm in} = 600$ V, $L_{01} = L_{02} = 600$ μH, $C_0 = 1$ μF, $V_0 = 300$ V, $P_0 = 30$ kW, and two IGBTs; each operates at 16 kHz.
5) Hard-switched buck converter operating in CDCM: $V_{\rm in} = 600$ V, $L_{01} = L_{02} = 90$ μH, $C_0 = 1$ μF, $V_0 = 300$ V, $P_0 = 30$ kW, and two IGBTs; each operates at 16 kHz.

Table I shows the estimated or measured losses in the compared converters.

In all cases, the conduction losses are estimated using the manufacturer's data. For the hard-switched cases, the switching losses are also estimated using the manufacturer's data. For the case of the ZCT technique described in [2], we apply the authors' conclusion that the total switching losses can be reduced to about 20% of the hard-switched case.

Several conclusions follow from the results reported in Table I and the analysis of Sections II and III.

1) The standard hard-switched buck converter cannot operate at 32 kHz: The junction-to-case temperature difference for the estimated 956 W of loss is around 120 °C. Much bigger devices or much lower switching frequency would be required to make the thermal design feasible.
2) The interleaved hard-switched CCM buck has much lower losses than the single-switch hard-switched buck, but it also has about 20% higher losses than the considered ZCT solutions.
3) The interleaved CDCM buck converter results in the lowest estimated losses. However, in applications where variable switching frequency is not acceptable (such as synchronized master/slave operation) or where high ripple current is a problem (such as current source applications and dc power supplies for plasma deposition processes where the output capacitance is required to be very low [24], [25]), constant-frequency CCM operation is required.
4) The approach described in [2] and the proposed interleaved ZCT buck converter result in similar losses (522 W versus 528 W). However, in the interleaved ZCT configuration, both switches participate in the power processing function of the converter and share the power equally. This significantly simplifies the practical thermal design.
5) Resonant-circuit losses for the ZCT approach described in [2] are more significant at lower output-power levels. The proposed interleaved ZCT converter, which does not employ a resonant circuit to accomplish zero-current switching, does not have this problem, as can be seen from the measured efficiency as a function of the output power shown in Fig. 14. The measured efficiency is around 97% for the output power over 15 kW. Even at light load (10% of the full power), the measured efficiency is as high as 86%.

Table II shows a comparison in switch ratings for the circuit described in [2] and the proposed circuit.

The switch rating in the proposed circuit is significantly lower than the rating for the main switch in the ZCT circuit [2]: The peak current is about 2.4 times lower, the average current is about two times lower, and the total losses are about 36% lower. The auxiliary switch in ZCT [2] has much lower average current and losses, but the peak current is about 40% higher than for the switches in the proposed circuit. Since the IGBTs are usually rated at two times higher peak current than the average current [29], the device required for the auxiliary switch in [2] would be comparable to the devices suitable for each of the two switches in the proposed circuit.

VI. CONCLUSION

This paper has described the interleaved ZCT converters where the switches are operating out-of-phase, whereas the turn-on transitions at zero current and a significant reduction of the losses associated with the diode reverse recovery are accomplished through the addition of two small inductors.

Compared with the hard-switched PWM converters, the switch-voltage and current stresses are not increased, and there are no significant restrictions on the range of operating duty ratios. Furthermore, although the two switches must be rated at full output current, both switches in the interleaved ZCT configuration participate in the power processing function and share the power equally: Each switch operates at two times lower switching frequency and conducts for only one half of the time compared with the hard-switched case. Compared with the interleaved DCM or critical conduction-mode converters, the proposed interleaved ZCT converters have the advantages of constant-frequency and low-ripple operation over a wide range

of output voltages and power, which is important in applications such as dc power supplies for plasma processes.

This paper describes an experimental 30 kW (300 V/100 A) interleaved ZCT buck converter operating at 32 kHz effective switching frequency. Losses, efficiency, switch-rating, and thermal-design issues in the experimental prototype compare favorably against the standard and interleaved hard-switched cases and the previously proposed ZCT schemes.

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