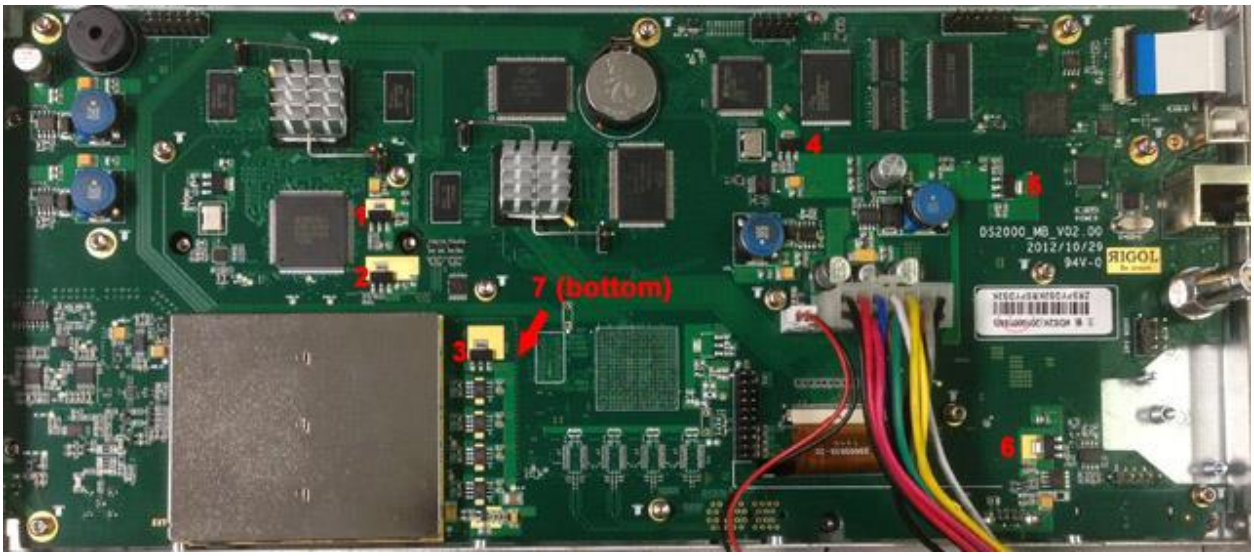
Project Yaigol

Part 4. Other Power Supplies

You guessed it – the title says it all. After finishing the PLL and its power supply fix I decided to check the other LDO regulators on the top of the PCB. I did not know at the time what I was getting myself into.

I still had the front panel attached so I could only have access to the PCB top side. The board has seven of 1117 LDO regulators marked in Red in this landscape photo. Six regulators on top and one (#7) on the PCB bottom:



Armed my little EMC probe I sniffed all of them and that led me to another [already not so] shocking discovery:

- **All 1117 LDO regulators in DS2072A were oscillating.**

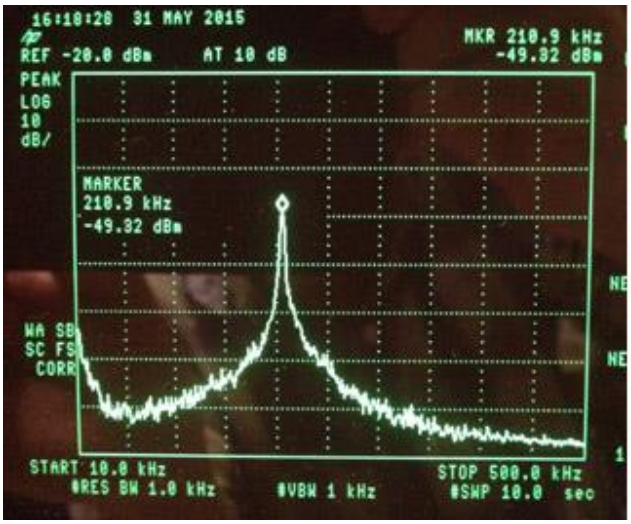
There it was. Yaigol could not have done any better than that.

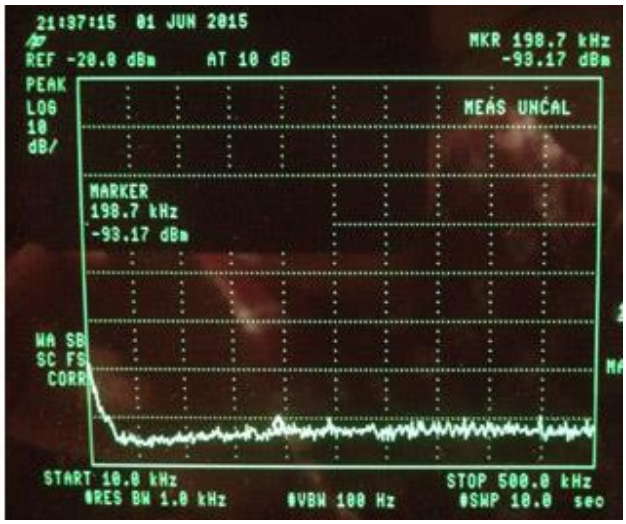
The regulators annotated in the photo are as follows:

1. +2V ADC Digital
2. +2V ADC Analog
3. +3.3V Trigger stage
4. +1.5V
5. +1.4V
6. +5V
7. +5V Input Attenuator control (located on PCB bottom side)

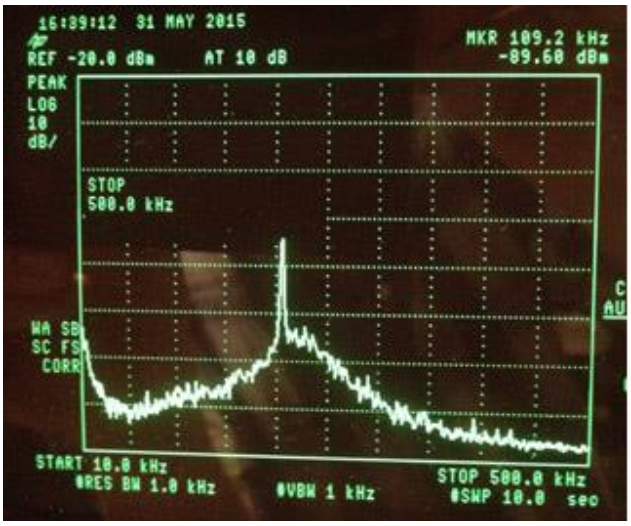
I started from #1 and #2 which are the ADC DVDD and AVDD +2V regulators. I checked the output rails with the spectrum analyzer, sure enough they were bad bad bad. I went ahead and replaced the output ceramic caps. Here is the screenshots for #1 and #2 before and after the fix:

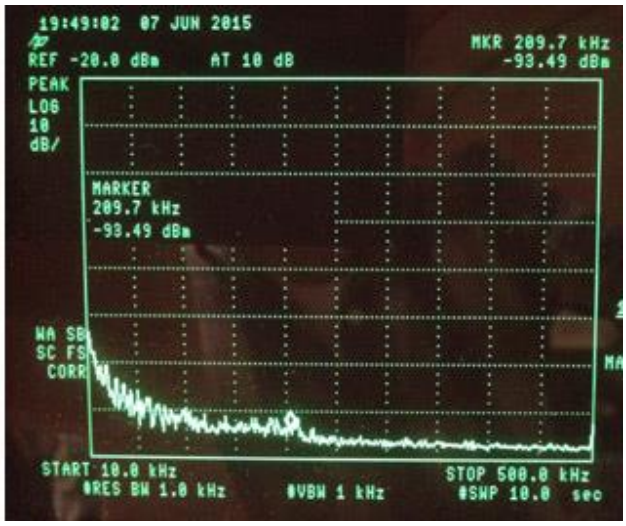
LDO #1 Before After





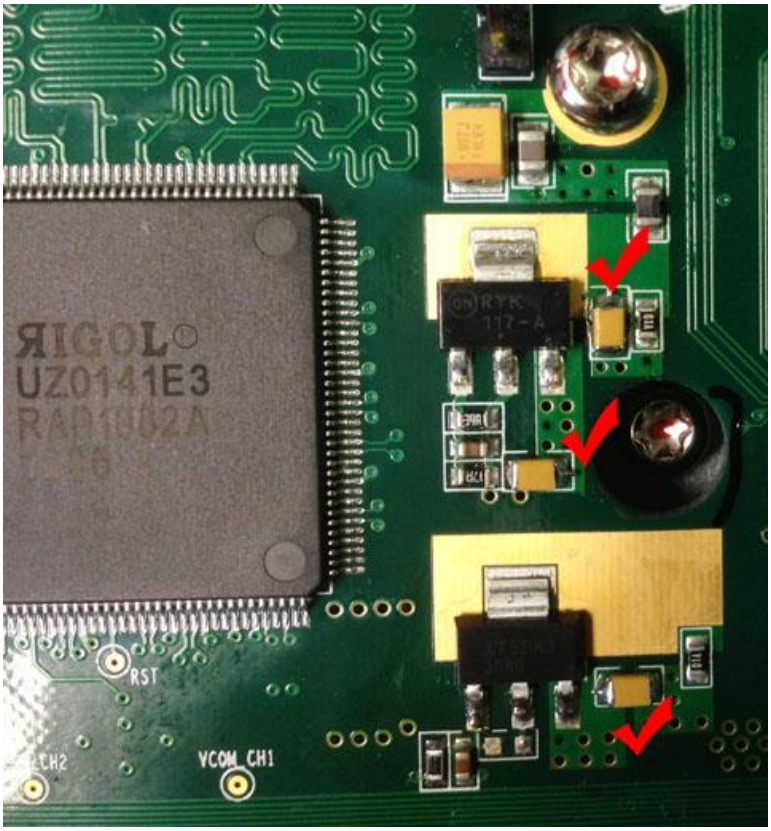
LDO #2 Before After





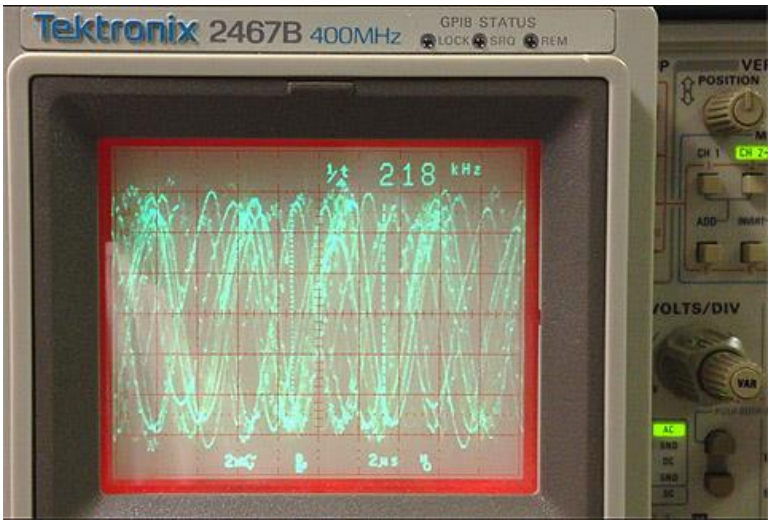
Mind you those are the ADC power regulators. Do I need to repeat? The ADC power regulators. The screenshots on the left are what you have in your Yaigol now. The pictures on the right is what you will have after you do the fix. You gain a 40dB improvement in ADC supply noise.

For your reference here is a photo of LDOs #1 and #2 with the output capacitors replaced with tantalum caps:

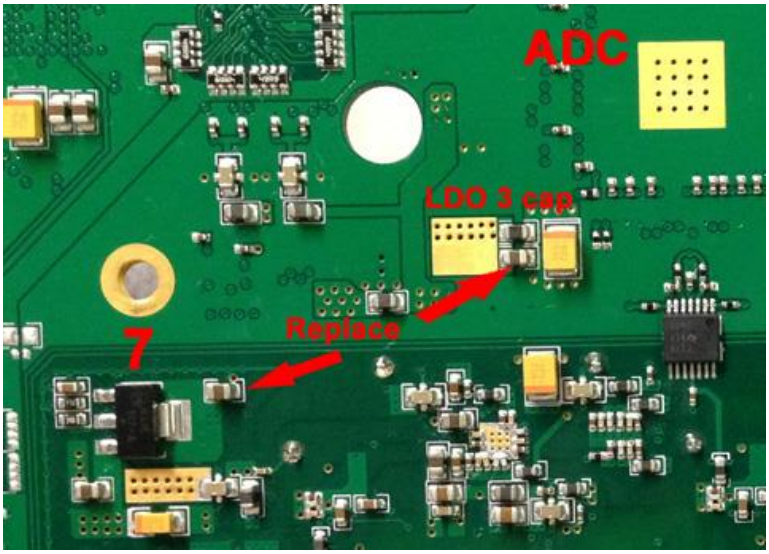


It seems I also replaced the input capacitor on LDO #1 for some reason, perhaps I saw it improved noise at the LDO input. I also replaced the LDO #2 (ADC Analog VDD) with a low noise LT 3080 adjustable regulator. You do not have to do this. I just attempted to minimize ADC supply noise as much as possible. LT1038 requires only one set resistor, so I removed one of the divider resistors and replaced the other with a new value calculated using the formula in the datasheet.

If you look again at the landscape photo of the annotated board, there are 5 more voltage regulators under the LDO #3, four in SOIC-8 and one in small SOT23 package. Those are the input stage power regulators. They are low ESR tolerant parts and did not oscillate but they shared the input +6.3V rail with the LDO #3, and that 6.3V rail was horribly oscillating at about 220kHz and some of it passed right through the input stage regulators and into the scope analog front-end. In fact it was the worst oscillation out of all I have seen so far in this crappy scope. Here is a screenshot of the 6.3V shared rail:

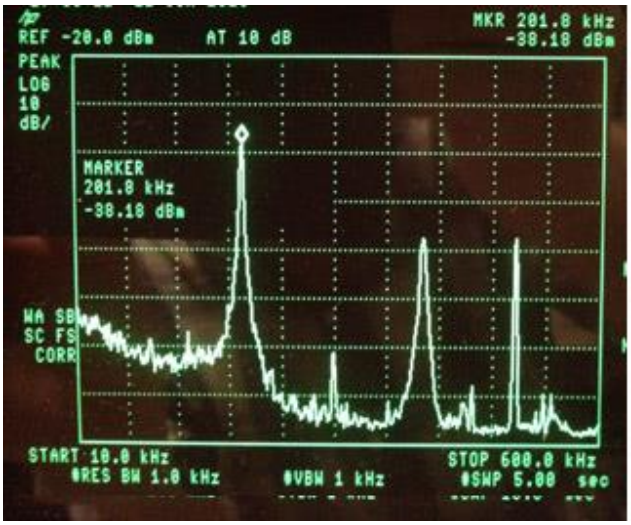


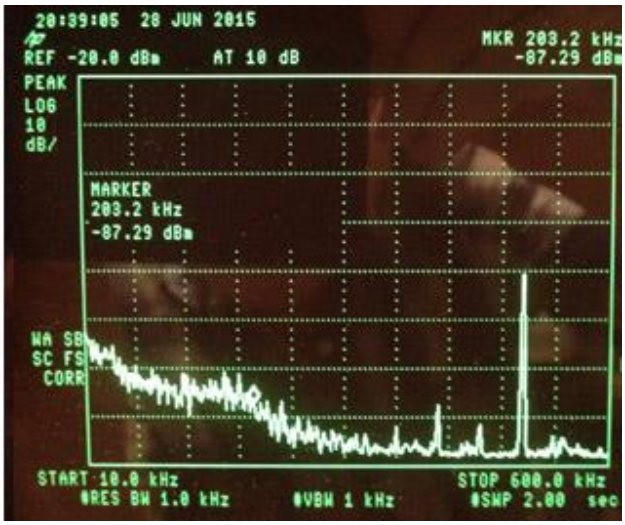
Sadly, there was no capacitor seen at LDO #3 output on the top side of the PCB. Was it on the bottom side? There was no choice left so I had to take the front panel off and sure enough there it was. And to my enjoyment there was another regulator (LDO #7) on the bottom:



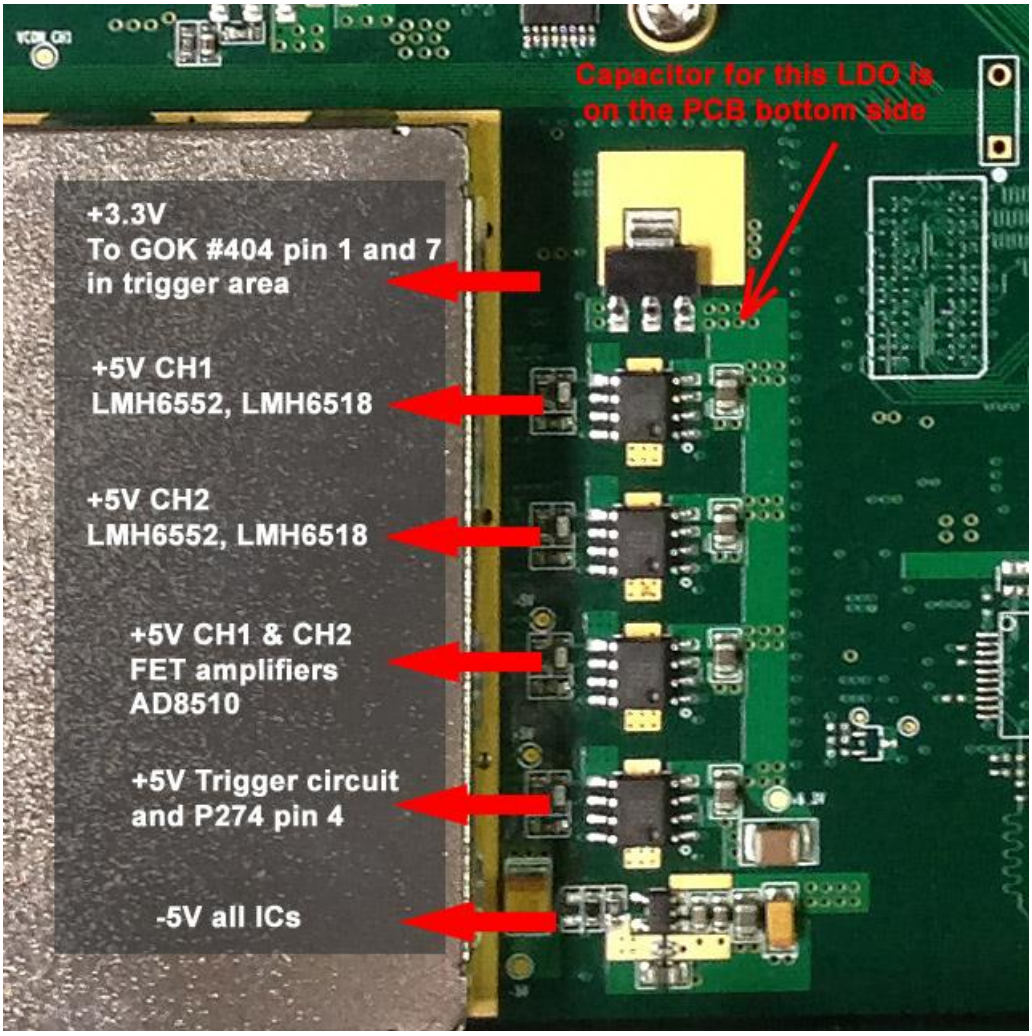
Here is screenshots of the 6.3V shared power rail before and after the fix. To remind you again, all regulators for the analog front-end were sitting on that rail. The two leftmost peaks in the left picture is the oscillation cause by the LDO #3 and #7 output caps. I observed that the two peaks were moving back and forth as the oscilloscope started up, performed startup check and went to acquisition state. Evidently, frequency of oscillation depended on the load on the rail. And this can happen because variations in consumed power cause variation in the load impedance and that affects the regulator's feedback loop. The rightmost third peak was not caused by LDO oscillation; it was a leftover from the upstream switching power regulator working at 500kHz switching frequency. It was not affected by the caps swap and remained on the rail after the change as can be seem in the right picture.

Shared +6.3V rail Before After





The following photo shows the power regulators for the analog input stage. Beside the top 1117 LDO, they are specified to work with ceramic capacitors and did not oscillate themselves, however before the fix they all had attenuated oscillation passing through them from their input 6.3V rail.



Before performing the LDO fix I had the oscilloscope self-calibrated. After completing this fix I noticed the offset level changed on both channels. Recalibrating the scope again removed it. That made me think that the change in the offset could have been caused by the oscillating LDOs. It was possible that RF voltage produced by oscillation was rectified in the input stage and caused a DC offset that the scope compensated during calibration. Now when I killed the oscillation, that quantity manifested itself from the grave as a change in the offset. I do not know for sure this was the case, just a guess. Interestingly enough, there was a post from a DS1000 scope user in the other thread where he said his scope has a offset that he can't get rid of. Recalibrating the scope did not help. Well, maybe he could try cracking the scope open and do the LDO capacitor fix and see if that helps.

I also replaced the output capacitors on the regulators #4 to #6. I will not bother you with screenshots, they all show oscillation before getting fixed. Just locate them using the landscape board photo and replace the ceramics soldered to the LDO's metal tab. Observe polarity on the replacement capacitors.

Conclusion

In DS2000 oscilloscope not only the PLL power regulator oscillates, all 1117 type LDO voltage regulators oscillate in factory scopes. The reason identified was:

- Incorrect selection of the LDO output capacitor and ignoring the manufacturer specification on ESR limits. That caused the LDOs to oscillate

And I am tired to tell you what I think about Yaigol. This time I am going to ask you to tell me what you think about their level of competency and if their Yingineers read Datasheets.

Though I had not performed testing after the fix and cannot confirm it, it may be possible that the LDO fix may help reduce random freezes/glitches because we improved the quality of supply power on several power rails on the board.

Main board 1117 LDO regulators Fix Instructions Summary

This is how to make the change described in this Part 4 and in addition to the change described in Part 3 to fully fix Yaigol DS2000 NCP1117 LDO voltage regulators:

- Replace the LDO output ceramic capacitor with a tantalum 10uF 10V…16V capacitor (observe the tantalum capacitor polarity). Use the landscape board photo at the beginning of this section to locate LDO regulators #1 to #6 on the PCB top and #7 on PCB bottom.

This completes the fix part of the Project Yaigol.

There will be no more fixes, likely not because there are none left but because I stopped at this point and did not find them. You can go ahead if you want and perform the fixes.

And a mandatory disclaimer is: this worked for me and I have no clue if this will work for you. Do this at your own risk and do not blame me for anything.

There is still a plenty of information to share with you but it is of exploratory nature. We will look at the front end, how it works; perhaps we will find some gimmicks there, stress test what the ADC is capable of and have some fun with thermal imaging.