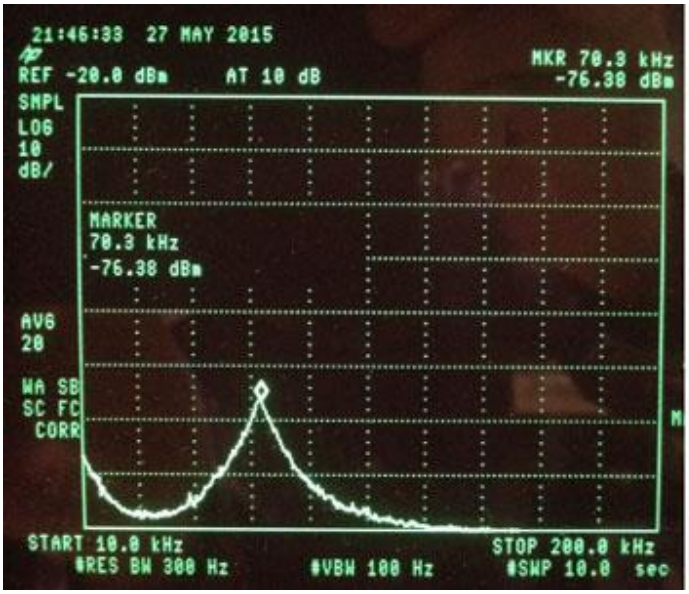
Project Yaigol

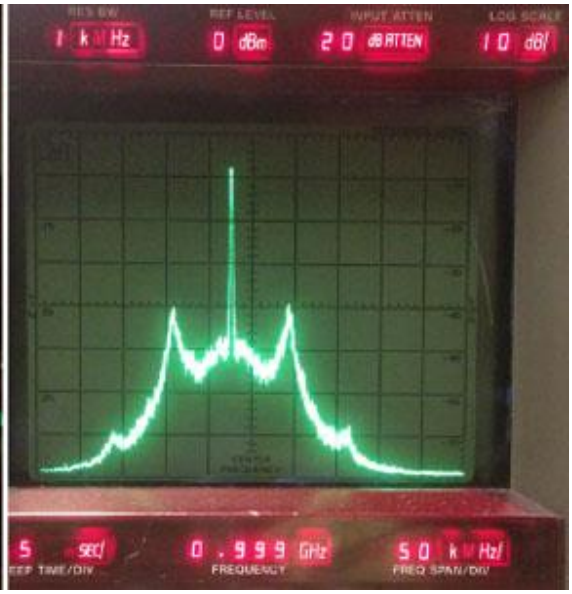
Part 3. The PLL Power Supply

So the bat wings… For a while I was not sure if I should just let it go and assemble the scope back and it would be end of story since I have fixed the PLL. But I decided to sniff around using my little EMI probe made from a piece of semi-rigid cable with a small wire loop on its end. The other end of the probe was connected to the spectrum analyzer. This is a beauty of having a spectrum analyser, you can see instantly what is happening in a wide range of frequencies at once (sweep time aside). With a RF voltmeter that would be not that much fun. I thought that the bat wings could have been caused by a stray coupling to some digital source nearby. I brought the probe close to the big ass chips including the ADC and looked if it emits something that has a correlation with the bat wings on the PLL skirt. It was almost accidentally that I bumped the probe into the PLL power supply LDO 1117 regulator. To my amusement (or horror, not sure what it was more of) the noise was coming out of the 1117 regulator. That led me to a little discovery:

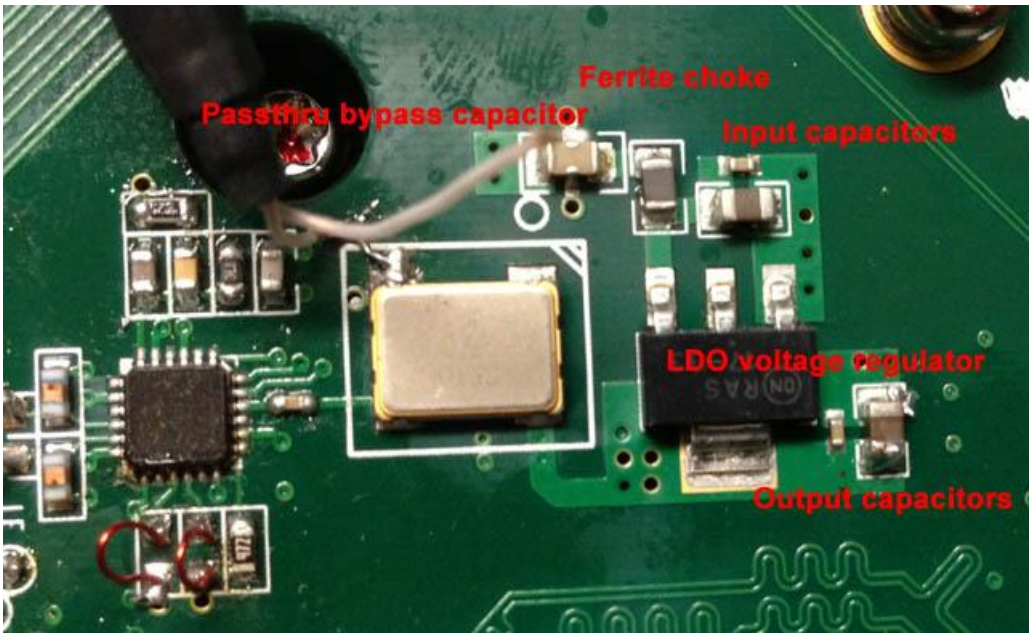
- The PLL power supply in DS2072A was oscillating.

The 1117 LDO supplies 3.3V to the reference oscillator and the PLL chip. I hooked up my SA to the power supply output and there it was – oscillation can be seen on the LDO output (left picture) that correlated with the PLL bat wings (right picture). It can be seen the peaks on both are at about 70kHz from the carrier:

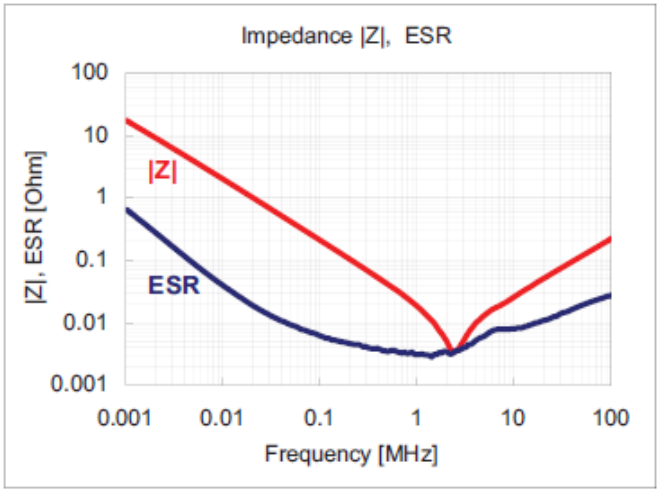




Despite of the oscillation being fairly weak, it was strong enough to affect the PLL's out of band noise. Regardless, you do not want your power supplies to oscillate. Looking at the power supply I already knew what may be causing the problem.

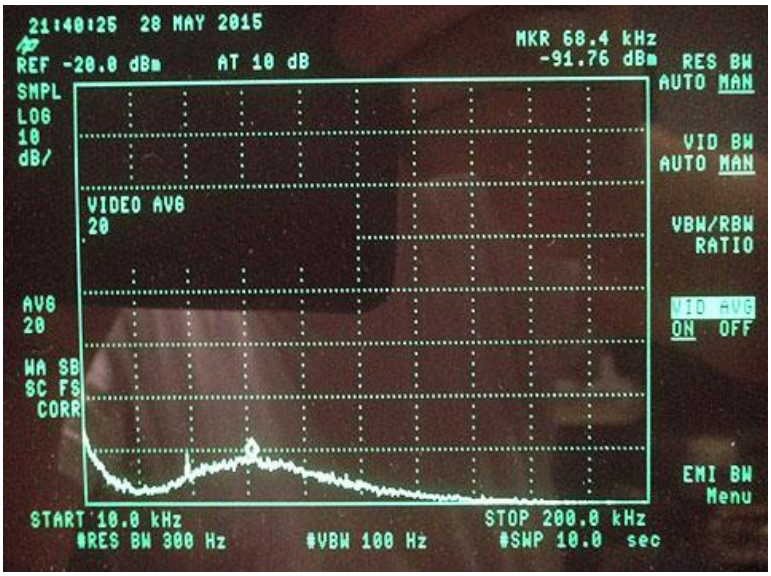


As someone you know says, "A trap for young players". When designing a power supply, you should always check with the datasheet for the voltage regulator you intend to use for any limits on the input and output capacitor ESR (equivalent series resistance). An out of specified limit ESR may cause instability of the internal LDO feedback loop and the LDO may oscillate. Ceramic capacitors have very low ESR and not always suitable for use with LDOs. From the photo we can see ceramic capacitors were used in the PLL power supply. Because we are not Yaigol employees, we can go and check the NCP1117 datasheet (evidently, Yaigol Yingineers did not bother). What it says is the output capacitor ESR for stability is required to be in the range of 33 mOhm to 2.2 Ohm. The output capacitor in the photo is a 10uF 0805 X5R capacitor (I unsoldered and measured the value, more on that later), these capacitors may have ESR of 10 mOhm or less which is outside of the specified limit for NCP1117. For example below is an ESR chart for a 10uF 10V 0805 X5R ceramic capacitor made by Samsung:

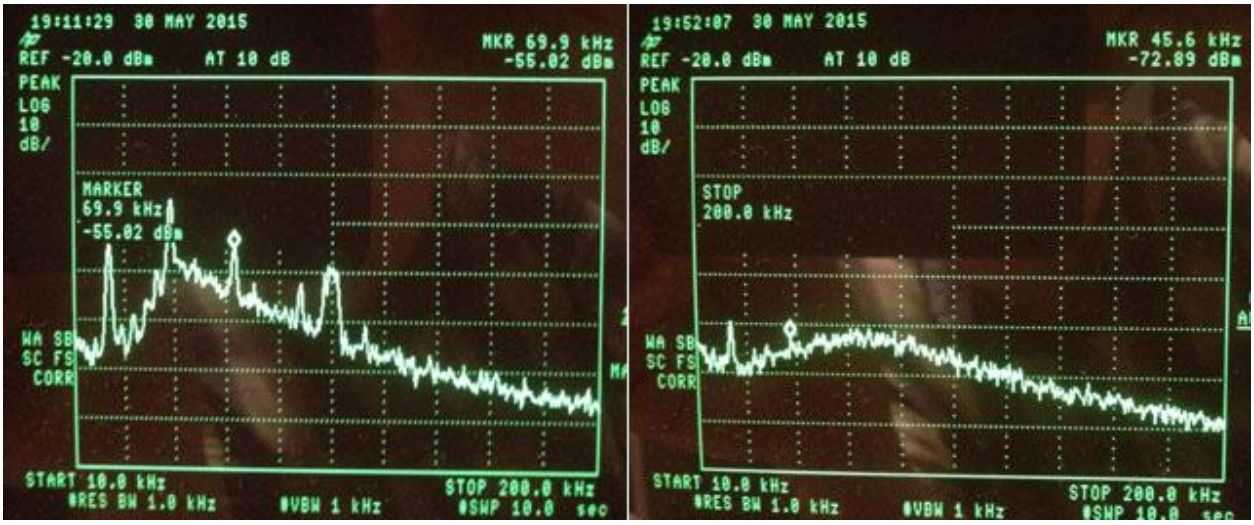


It can be seen the ESR for this particular model goes as low as 3 mOhm. There perhaps be some variance between manufacturers but for a same type of dielectric it would not differ much. No wonder the Yaigol PLL power supply was oscillating.

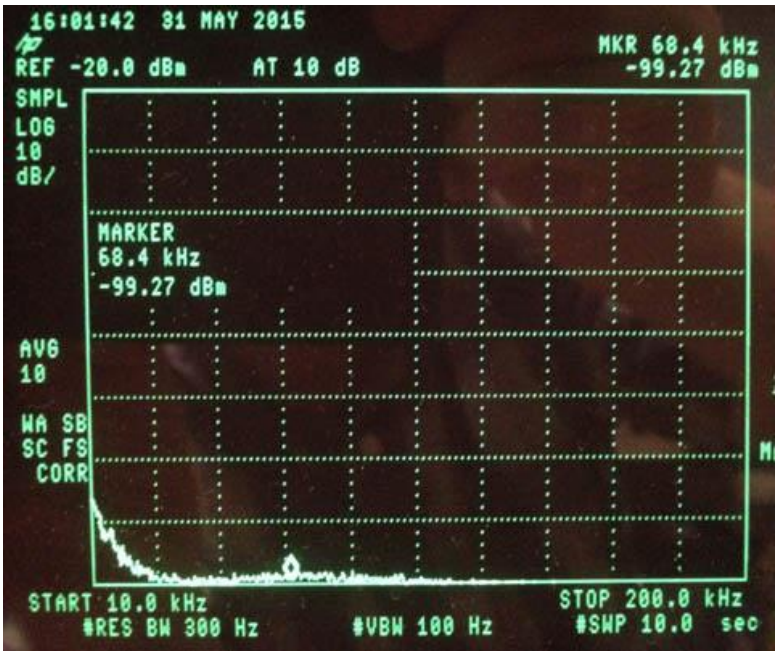
I went ahead and replace the output 10uF ceramic capacitor with a 10uF tantalum one. That damped the oscillation but a hump on the output rail remained:



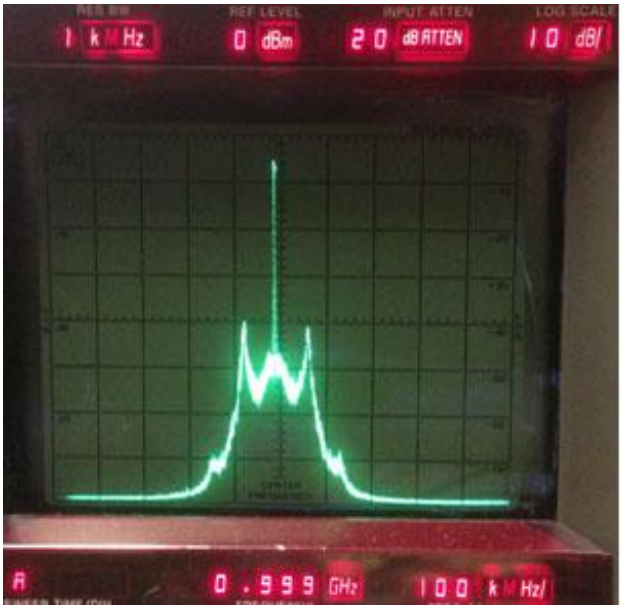
I thought that it could be caused by pass-through noise from LDO input and moved the SA to the LDO input. I checked the input power rail before and after the ferrite choke. There was noise on the rail before the choke and the choke did not appear to be doing a good job, there was plenty of noise passing thru the choke and it had a correlation with the hump on the LDO output. I removed the ferrite choke and replaced it with a 10 Ohm 0805 resistor. There was sufficient voltage headroom for the resistor voltage drop to not cause any problems to the LDO. Below is the resulting screenshots of LDO input rail: before (left) and after (right) replacing the ferrite choke with a 10 Ohm resistor.

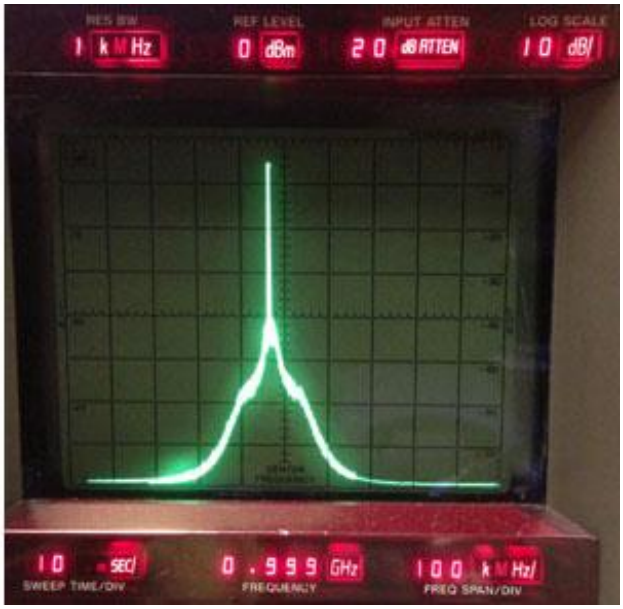


That resulted in the hump disappearing at LDO output. Here is the final PLL LDO output rail spectral screenshot, nice and quiet:



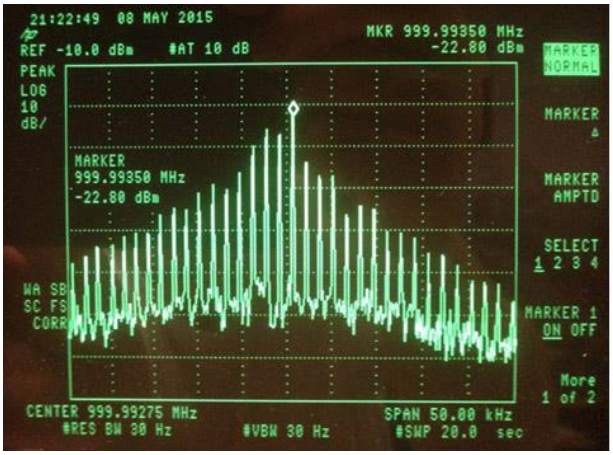
OK, but did it make a difference in the PLL clock output purity? Yes it did and the bat wings have now gone. Here are screenshots before and after the PLL power supply fix:



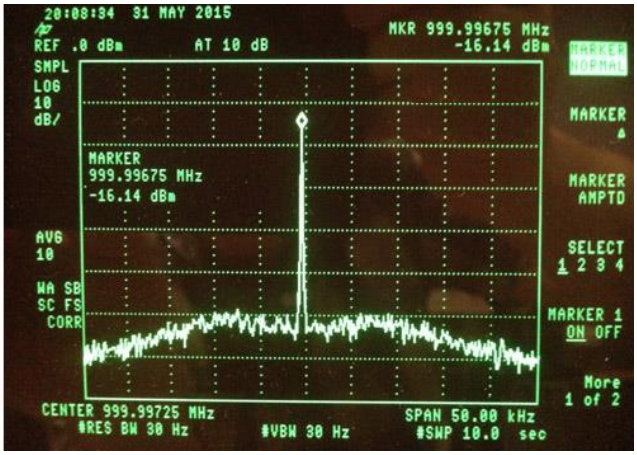


The picture on the right is the final result of the investigation we've performed in Part 2 and Part 3 in this article. That is what my DS2072A had when I completed the Project. This is what you will have if you want to fix yours. And to let you appreciate the overall change in PLL signal quality (read: ADC clock quality) one more time: we went from this to this :

Before



After



Conclusion

DS2000 oscilloscope PLL power supply oscillates in factory scopes. This must not happen in the first place, and this affects the PLL output signal purity. The reasons identified were:

- Incorrect selection of the LDO output capacitor and ignoring the manufacturer specification on ESR limits. That caused the LDO to oscillate
- Suboptimal design of the LDO input network. The ferrite choke did not suppress input power rail noise sufficiently. Input noise passed through the LDO and appeared at LDO output

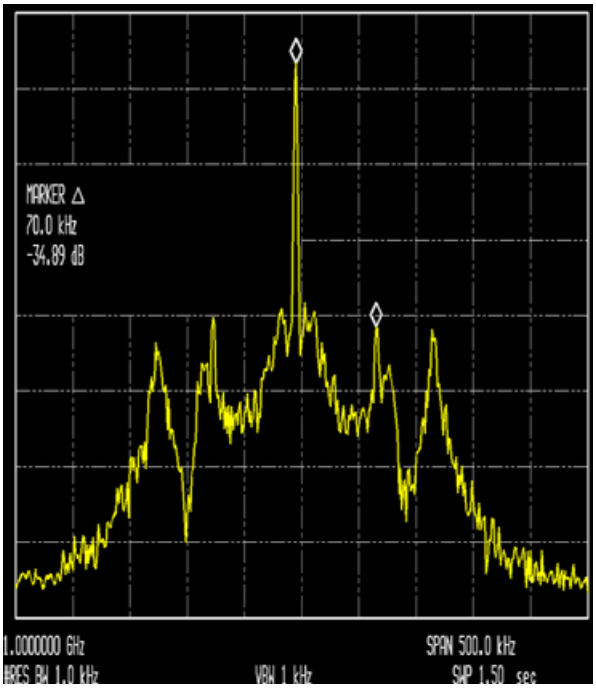
Once again all indications are Yaigol Yingineers do not read Datasheets. It is a grade 1 student error to be unaware of ESR limits checks when building power supplies. For a company that positions itself as a test equipment manufacturer this is sheer incompetence. What possibly you can test with equipment built using these (lack of) practices?

PLL Power Supply Fix Instructions Summary

This is how to make the change described in this Part 3 and in addition to the change described in Part 2 to fully fix Yaigol DS2000 PLL (refer to the photo provided earlier in this article to identify the PLL power supply components):

- Replace the LDO output ceramic capacitor with a tantalum 10uF 10V capacitor (observe the tantalum capacitor polarity) .You can leave the smaller 0.1 uF 0402 blocking capacitor in place
- Replace the ferrite choke at LDO input with a 10 Ohm 0805 resistor.

The last thing that is worth mentioning: you may remember I had a Deja vu back in Part 2 about the bat wings in the PLL spectrum. Sure enough I knew, that came from the original DS1000 PLL fix discussion thread, which caused this investigation. There was the same problem with junky PLL in DS1000 scopes and back then Yaigol issued a firmware update for DS1000 that improved its PLL. Here is a picture of a the DS1000 PLL after that update (borrowed from the DS1000 thread):



Do you see what I see? The bat wings… The same crap we had on DS2000 caused by the PLL power supply. What that may mean is DS1000 scopes may have exact same problem with the PLL power supply oscillating. I do not have a DS1000 to verify but may be one or more of you could look into it and report back. What needs to be checked is the model of the PLL LDO regulator, if its output capacitor is of a ceramic type and if the LDO's datasheet speaks about ESR limits for output capacitors. Having known Yaigol practices (or lack of thereof), I would not be surprised if the two scope models share the same problem.

Having said that and considering our PLL fix complete, we can close the case. Or… should we? What else possibly can be checked? Had any problems recently with your scope freezing? Unexplained crashes? Offset fluctuating? Have you already guessed what else we will be checking? Wait for Part 4 to have even more fun with your Yaigol.