(2)Oscillator operation when intermittent action and OSC control circuit operates.

When over current signal is applied to CLM + or CLM − terminal, and the current limitting circuit, intermittent action and OSC control circuit starts to operate. In this case T-OFF terminal voltage depends on VF terminal voltage, so the oscillation frequency decreases and dead-time spreads.

The rise rate of oscillation waveform is given as

$$\simeq \frac{V_{T\text{-}ON}}{R_{ON} \times C_F} \quad (V/s) \cdots\cdots (5)$$

The fall rate of oscillation waveform is given as

$$\simeq \frac{V_{VF} - V_{VFO}}{R_{OFF} \times C_F} + \frac{V_{T-ON}}{16 \times R_{ON} \times C_F} \quad (V/s) \cdots\cdots (6)$$

where $V_{T-ON} \simeq 4.5V$
V_{VF}; VF terminal voltage
$V_{VFO} \simeq 0.4V$
$V_{VF} - V_{FO} = 0$ if $V_{VF} - V_{VFO} < 0$
$V_{VF} - V_{VFO} = V_{T-OFF}$ if $V_{VF} - V_{VFO} > V_{T-OFF} \simeq 3.5V$

So when $V_{VF} > 3.5V$, the operation is just same as that in the no current limitting operation state.
The maximum on-duration is just same as that in the no-operation state of intermittent and oscillation control circuit and is given as follows;

$$\simeq \frac{(V_{OSCH} - V_{OSCL}) \times R_{ON} \times C_F}{V_{T\text{-}ON}} \quad (s) \cdots\cdots (7)$$

The minimum off-duration is approximately given as ;

$$\simeq \frac{(V_{OSCH} - V_{OSCL}) \times C_F}{\frac{V_{VF} - V_{VFO}}{R_{OFF} \times C_F} + \frac{V_{T\text{-}ON}}{16 \times R_{ON} \times C_F}} \quad (s) \cdots\cdots (8)$$

The oscillation period is given by the summation of Equation (7) and (8).
As shown in Fig. 7, the internal circuit kills the first output pulse in the output waveform. The output waveform will appear from the second pulse cycle because the duration of first cycle takes C_F charging time longer comparing with that at the stable operating state.
Usually the applied voltage to VF terminal must be proportional the output voltage of the regulator.
So when the over current occurs and the output voltage of the regulator becomes low, the off-duration becomes wide.
There are two methods to get the control voltage, which depends on the output voltage, on primary side. For the fly back type regulator application, the induced voltage on the third or bias winding is dependent on output voltage. On the other hand, for the feed forward type regulator application, it can be used that the output voltage depends on the product of induced voltage and "on-duty", as the current of choke coil will continue at over load condition, it means the "continuous current" condition.
Fig. 8 shows one of the examples for VF terminal application for the feed forward type regulator.

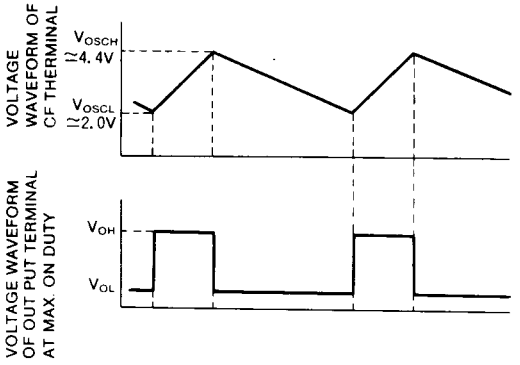


Fig. 6 OSC. waveform with operation of intermittent and OSC. control circuit operation

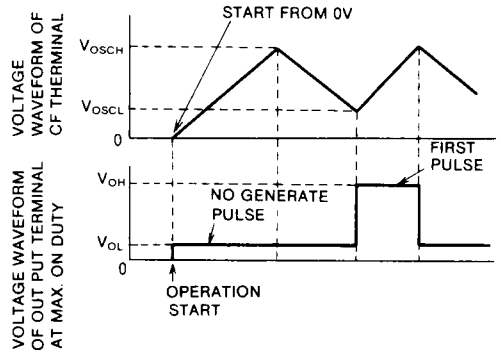


Fig. 7 Relation between OSC. and output waveform circuit operation at start up

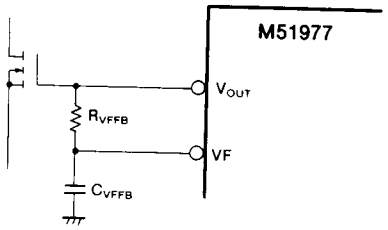


Fig. 8 Feedback loop with low pass filter from output to VF terminal

PWM comparator and PWM latch section

Fig. 9 shows the PWM comparator and latch section. The on-duration of output waveform coincides with the rising duration of CF terminal waveform,when the infinitive resistor is connected between F/B terminal and GND.

When the F/B terminal has finite impedance and current flows out from F/B terminal,"A" point potential shown in Fig. 9 depends on this current. So the "A" point potential is close to GND level when the flow-out current becomes large.

"A" point potential is compared with the CF terminal oscillator waveform and PWM comparator, and the latch circuit is set when the potential of oscillator waveform is higher than "A" point potential.

On the other hand, this latch circuit is reset by high level signal during the deadtime of oscillation (falling duration of oscillation waveform). So the "B" point potential or output waveform of latch circuit is the one shown in Fig. 10.

The final output waveform or "C" point potential is got by combining the "B" point signal and dead-time signal logically. (please refer to Fig. 10)

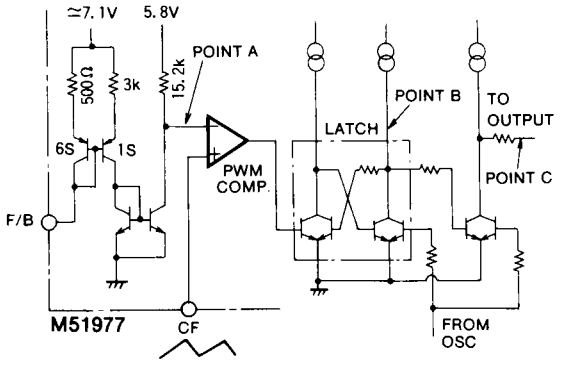


Fig. 9 PWM comparator and latch circuit

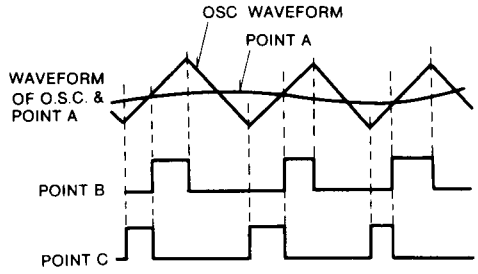


Fig. 10 Waveforms of PWM comparator input point A, latch circuit points B and C

Current limitting section

When the current-limit signal is applied before the crossing instant of "A" point potential and CF terminal voltage shown in Fig. 9, this signal makes the output "off" and the off state will continue until next cycle. Fig. 11 shows the timing relation among them.

The current limitting circuit has two input terminals, one has the detector-sensitivity of + 200mV to the GND terminal and the other has − 200mV. The circuit will be latched if the input signal is over the limit of either terminal.

If the current limitting circuit is set, no waveform is generated at output terminal however this state is reset during the succeeding dead-time.

So this current limitting circuit is able to have the function in every cycle, and is named "pulse-by-pulse current limit".

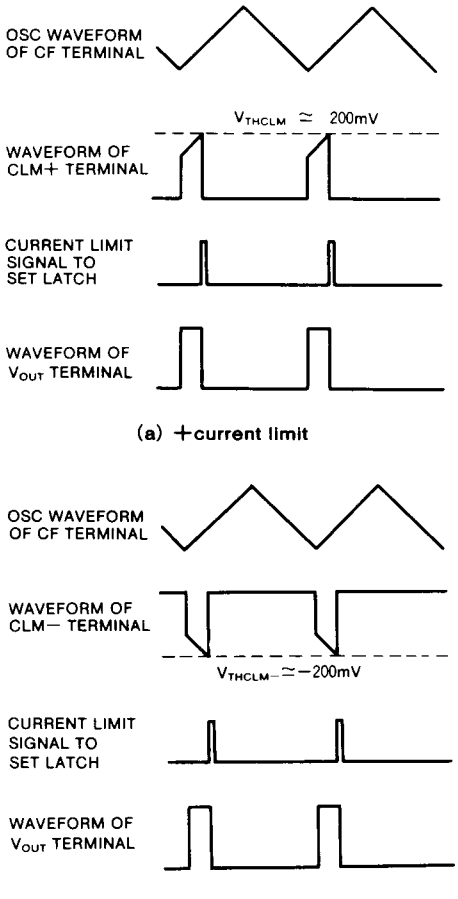
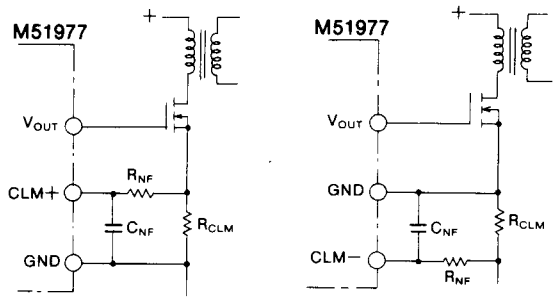


Fig. 11 Operating waveforms of current limitting circuit

It is rather recommended to use not "CLM+" but "CLM−" terminal, as the influence from the gate drive current of MOS-FET can be eliminated and wide voltage rating of +

4V to −4V is guaranteed for absolute maximum rating.
There happen some noise voltage on R_{CLM} during the switching of power transistor due to the snubber circuit and stray capacitor of the transformer windings.
To eliminate the abnormal operation by the noise voltage, the low pass fillter, which consists of R_{NF} and C_{NF} is used as shown in Fig. 12.
It is recommended to use 10~100Ω for R_{NF} because such range of R_{NF} is not influenced by the flow-out current of some 200μA from CLM terminal and C_{NF} is designed to have the enough value to absorb the noise voltage.

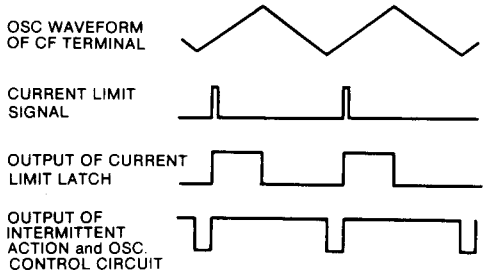


(a) In case of CLM+ (b) In case of CLM−

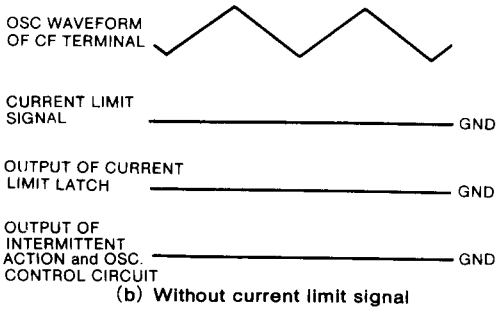
Fig. 12 How to connect current limit circuit

Intermittent action and oscillation control section

When the internal current limitting circuit starts to operate and also the VF level decreases to lower than the certain level of some 3V, the dead-time spreads and intermittent action and OSC control circuit (which is one of the timer-type-protection circuit) starts to operate.
The intermittent action and OSC control circuit is the one to generate the control signal for oscillator and intermittent action circuit.
Fig.13 shows the timing-chart of this circuit. When the output of intermittent action and oscillation control is at "high" level, the waveform of oscillator depends on the VF terminal voltage and the intermittent action circuit begins to operate.



(a) With current limit signal



(b) Without current limit signal

Fig. 13 Timing chart of interrmittent and OSC. control circuit

Intermittent action circuit section

Intermittent action circuit will start to operate when the output signal from the intermittent action and oscillation control circuit are "high" and also VF terminal voltage is lower than V_{THTIME} of about 3V.
Fig. 14 shows the block diagram of intermittent action circuit. Transistor Q is on state when VF terminal voltage is higher than V_{THTIME} of about 3V, so the CT terminal voltage is near to GND potential.
When VF terminal voltage is lower than V_{THTIME}, Q becomes "off" and the CT has the possibility to be charged up.
Under this condition, if the intermittent action and oscillation control signal become "high", the switch SW_A will close only in this "high" duration and C_T is charged up by the current of 120μA through SW_A (SW_B is open) and CT terminal potential will rise. The output pulse can be generated only in this duration..
When the CT terminal voltage reaches to 8V, the control logic circuit makes the SW_A "off" and SW_B "on", in order to flow in the $I_{TIMEOFF}$ of 15μA to CT terminal.
The IC operation will be ceased in the falling duration.
On the other hand, when CT terminal voltage decreses to lower than 2V, the IC operation will be reset to original state, as the control logic circuit makes the SW_A "on" and SW_B "off".
Therefore the parts in power circuit including secondary rectifier diodes are protected from the overheat by the over current.

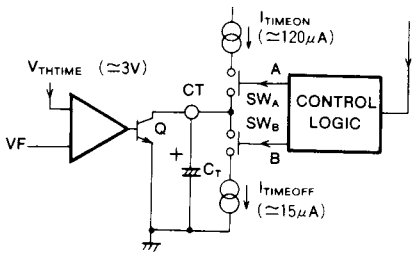


Fig. 14 Block diagram of Intermittent action circuit

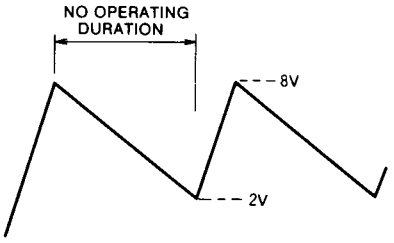


Fig. 15 Waveform of CT terminal

Fig. 16 shows the I_{CC} versus V_{CC} in this timer-off duration. In this duration the power is not supplied to IC from the third winding of transformer but through from the resistor R_1 connected to V_{CC} line.
If the R_1 shown in Fig. 1 and 2 is selected adequate value, V_{CC} terminal voltage will be kept at not so high or low but adequate value, as the I_{CC} versus V_{CC} characteristics has such the one shown in Fig. 16.

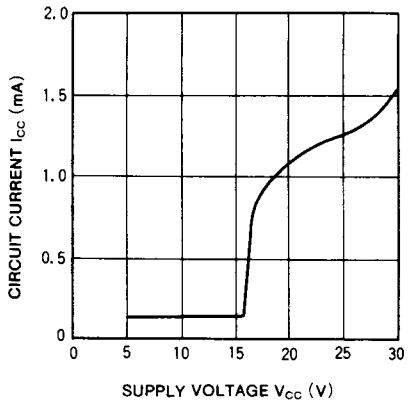


Fig. 16 I_{CC} vs. V_{CC} in timer-off duration of intermittent action circuit

To ground the CT terminal is recommended, when the intermittent mode is not used.
In this case the oscillated frequency will become low but the IC will neither stop the oscillation nor change to the intermittent action mode, when the current limit function becomes to operate and the VF terminal voltage becomes low.

Voltage detector circuit (DET) section

The DET terminal can be used to control the output voltage which is determined by the winding ratio of fly back transformer in fly-back system or in case of common ground circuit of primary and secondary in feed forward system.
The circuit diagram is quite similar to that of shunt regulator type 431 as shown in Fig. 17. As well known from Fig. 17 and Fig. 18, the output of OP AMP has the current-sink ability, when the DET terminal voltage is higher than 2.5V but it becomes high impedance state when lower than 2.5V DET terminal and F/B terminal have inverting phase characteristics each other, so it is recommended to connect the resistor and capacitor in series between them for phase compensation. It is very important, one can not connect by resistor directly as there is the voltage difference between them and the capacitor has the DC stopper function.

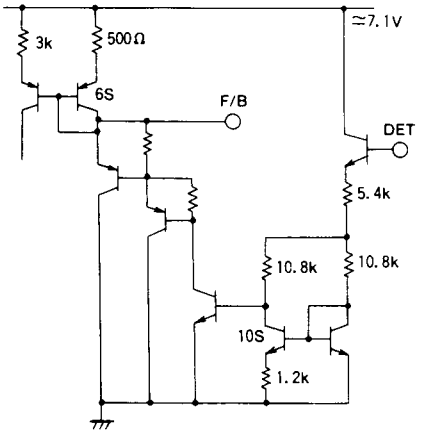


Fig. 17 Equivalent circuit diagram of voltage detector

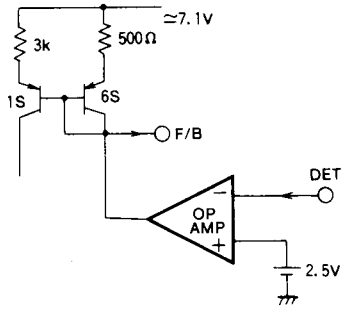


Fig. 18 Equivalent circuit diagram of voltage detector

ON-OFF circuit section

Fig. 19 shows the circuit diagram of ON-OFF circuit. The current flown into the ON/OFF terminal makes the Q_4 "on" and the switching operation stop. On the other hand, the switching operation will recover as no current flown into ON/OFF terminal makes Q_4 "off". As the constant current source connected to Q_4 base terminal has such the hyster-

isis characteristics of 20μA at operation and 3μA at stopping. So the unstable operation is not appeared even if the ON/OFF terminal voltage signal varies slowly.

Fig. 20 shows how to connect the ON/OFF terminal. The switching operation will stop by switch-off and operate by switch-on.

Transistor or photo transistor can be replaced by this switch, of cource. No resistor of 30~100kΩ is connected and ON/OFF terminal is directly connected to GND, when it is not necessary to use the ON/OFF operation.

Fig. 21 shows the I_{CC} versus V_{CC} characteristics in OFF state and V_{CC} will be kept at not so high or low but at the adequate voltage, when R_1 shown in Fig. 1 and 2 is selected properly.

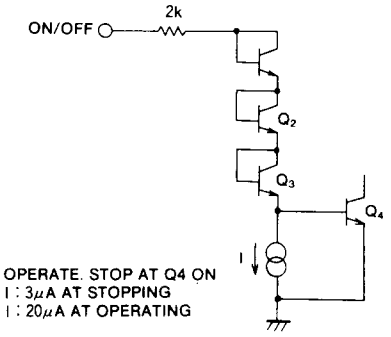


Fig. 19 ON/OFF circuit

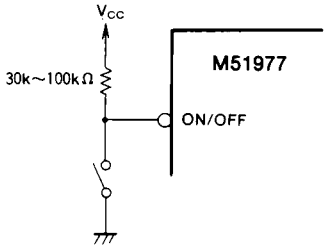


Fig. 20 Connecting of ON/OFF terminal

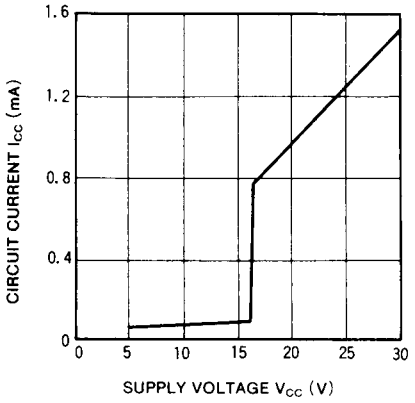


Fig. 21 I_{CC} vs. V_{CC} in OFF state

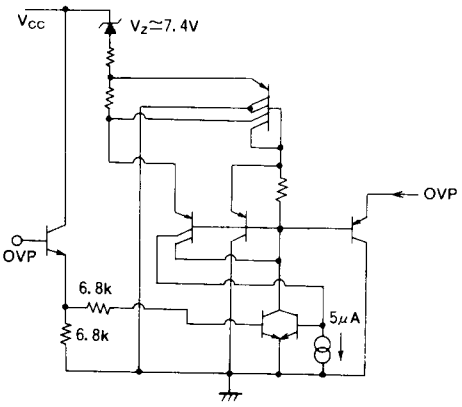


Fig. 22 Equivalent circuit diagram of OVP

OVP circuit section

OVP circuit is basically constructed by the complementary flip-flop circuit as shown in Fig. 22. Once the input signal is applied to the OVP circuit which has the detect sensitivity of $2V_{BE}$ the output becomes "off" and this "off" state will be kept unitil V_{CC} becomes to less than OVP reset voltage($\simeq$ 8.5V).

As the OVP "off" state is kept by the current through R_1 shown in Fig. 1 and 2. M51977 is designed to have the low I_{CC}, which value is some level of adding 10μA to the start-up current at OVP reset voltage.

As M51977 has such the I_{CC} versus V_{CC} characteristics as shown in Fig. 23, no failure is occured by applied high voltage to IC. That is; higher the V_{CC} or DC supply voltage, higher the I_{CC} current and larger the voltage drop at R_1.

As the OVP reset voltage is settled rather high voltage of 8.5V, SMPS can be reset in rather short time from the switch-off of AC power source if the smoothing capacitor is not so large value.

However the reset time may become problem when the C_{FIN} is large and so the discharge time constant of $C_{FIN} \times (R_1+R_2)$ is large.

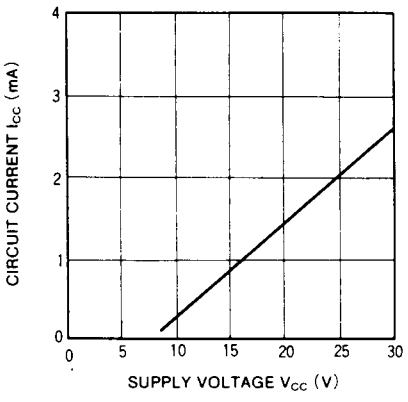


Fig. 23 I_{CC} vs. V_{CC} in OVP operation

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Output section

It is required that the output circuit have the high sink and source abilities for MOS-FET drive. It is well known that the "totempole circuit has high sink and source ability. However, it has the demerit of high through current.

For example, the through current may reach such the high current level of 1A, if type M51977 has the "conventional" totempole circuit. For the high frequency application such as higher than 100kHz, this through current is very important factor and will cause not only the large I_{CC} current and the inevitable heat-up of IC but also the noise voltage.

This IC uses the improved totempole circuit, so without deteriorating the characteristic of operating speed, its through current is approximately 100mA.

APPLICATION NOTE OF TYPE M51977P,FP

Design of start-up circuit and the power supply of IC

(1)The start-up circuit when it is not necessary to set the start and stop input voltage

Fig. 24 shows one of the example circuit diagram of the start-up circuit which is used when it is not necessary to set the start and stop voltage.

It is recommended that the current more than 300μA flows through R_1 in order to overcome the operation start-up current $I_{CC(START)}$ and C_{VCC} is in the range of 10 to 47μF. The product of R_1 by C_{VCC} causes the time delay of operation, so the response time will be long if the product is too much large.

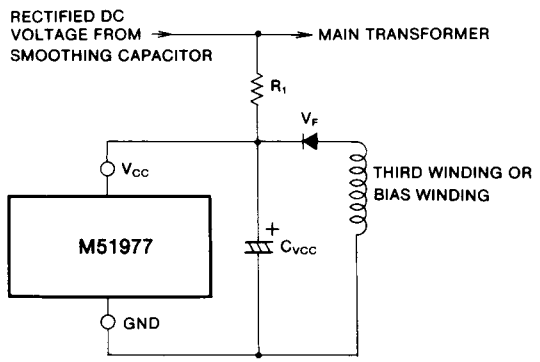

Fig. 24 Start-up circuit diagram when it is not necessary to set the start and stop input voltage

Just after the start-up, the I_{CC} current is supplied from C_{VCC}, however, under the steady state condition, IC will be supplied from the third winding or bias winding of transformer, the winding ratio of the third winding must be designed so that the induced voltage may be higher than the operation-stop voltage $V_{CC(STOP)}$.

The V_{CC} voltage is recommended to be 12V to 17V as the normal and optimum gate voltage is 10 to 15V and the output voltage (V_{OH}) of type M51977P, FP is about (V_{CC}−2V). It is not necessary that the induced voltage is settled higher than the operation start-up voltage $V_{CC(START)}$, and the high gate drive voltage causes high gate dissipation, on the other hand, too low gate drive voltage does not make the MOS-FET fully on-state or the saturation state.

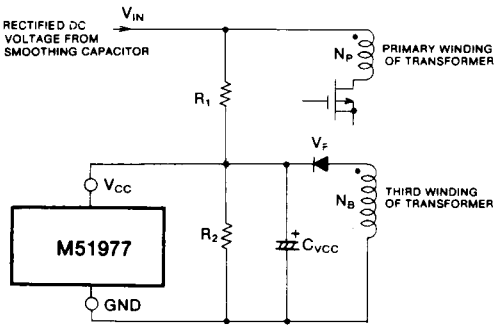

Fig. 25 Start-up circuit diagram when it is necessary to set the start and stop input voltage

(2)The start-up circuit when it is necessary to set the start and stop input voltage

It is recommend to use the third winding of "forward winding" or "positive polarity" as shown in Fig. 25, when the DC source voltages at both the IC operation start and stop must be settled at the specified values.

The input voltage ($V_{IN(START)}$), at which the IC operation starts, is decided by R_1 and R_2 utilizing the low start-up current characterisitics of type M51977P, FP.

The input voltage ($V_{IN(STOP)}$), at which the IC operation stops, is decided by the ratio of third winding of transformer.

The $V_{IN(START)}$ and $V_{IN(STOP)}$ are given by following equations.

$$V_{IN(START)} \simeq R_1 \cdot I_{CCL} + \left(\frac{R_1}{R_2} + 1\right) \cdot V_{CC(START)} \quad \cdots\cdots (9)$$

$$V_{IN(STOP)} \simeq (V_{CC(STOP)} - V_F) \cdot \frac{N_P}{N_B} + \frac{1}{2} V'_{IN\ RIP(P\text{-}P)} \quad \cdots\cdots (10)$$

where

I_{CCL} is the operation start-up current of IC

$V_{CC(START)}$ is the operation start-up voltage of IC

$V_{CC(STOP)}$ is the operation stop voltage of IC

V_F is the forward voltage of rectifier diode

$V'_{IN\ (P\text{-}P)}$ is the peak to peak ripple voltage of V_{CC} terminal $\simeq \frac{N_B}{N_P} V_{IN\ RIP(P\text{-}P)}$

It is required that the $V_{IN(START)}$ must be higher than $V_{IN(STOP)}$.

When the third winding is the "fly back winding" or "reverse

polarity", the $V_{IN(START)}$ can be fixed, however, $V_{IN(STOP)}$ can not be settled by this system, so the auxiliary circuit is required.

(3)Notice to the V_{CC}, V_{CC} line and GND line

To avoid the abnormal IC operation, it is recommended to design the V_{CC} is not vary abruptly and has few spike voltage, which is induced from the stray capacity between the winding of main transformer.

To reduce the spike voltage, the C_{VCC}, which is connected between V_{CC} and ground, must have the good high frequency characteristics.

To design the conductor-pattern on PC board, following cautions must be considered as shown in Fig. 26.

(a) To separate the emitter line of type M51977 from the the GND line of the IC

(b) To locate the C_{VCC} as near as possible to type M51977 and connect directly

(c) To separate the collector line of type M51977 from the V_{CC} line of the IC

(d) To connect the ground terminals of peripheral parts of ICs to GND of type M51977 as short as possible

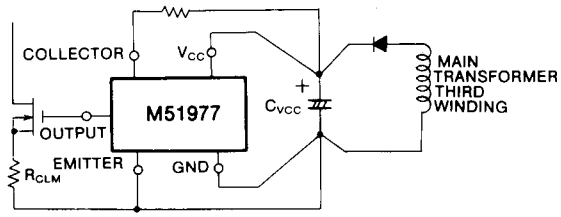

Fig. 26 How to design the conductor-pattern of type M51977 on PC board (schematic example)

(4)Power supply circuit for easy start-up

When IC start to operate, the voltage of the C_{VCC} begins to decrease till the C_{VCC} becomes to be charged from the third winding of main-transformer as the I_{CC} of the IC increases abruptly. In case shown in Fig. 24 and 25, some "unstable start-up" or "fail to start-up" may happen, as the charging interval of C_{VCC} is very short duration; that is the charging does occur only the duration while the induced winding voltage is higher than the C_{VCC} voltage, if the induced winding voltage is nearly equal to the "operation-stop voltage" of type M51977.

In this case the circuit shown in Fig.27 is recommended.

It is recommended to use the 10 to 47μF for C_{VCC1}, and about 5 times capacity bigger than C_{VCC1} for C_{VCC2}.

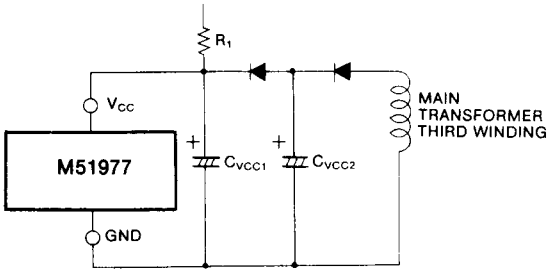

Fig. 27 DC source circuit for stable start-up

OVP circuit

(1)To avoid the miss-operation of OVP

It is recommended to connect the resistor of 12kΩ and capacitor between OVP terminal and GND, and also resistor of 10kΩ in series to the photo-coupler as the input impedance of OVP terminal is very high and the pulsive-displacement-current inclines to make the IC miss-operation when V_{CC} is changed abruptly.

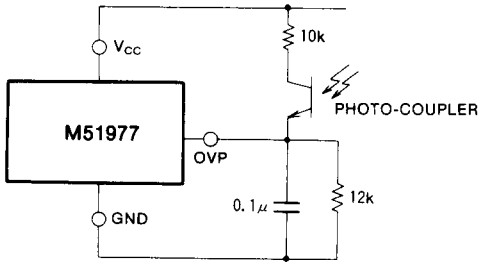

Fig. 28 Peripheral circuit of OVP terminal

(2)Application circuit to make the OVP-reset time fast

The reset time may becomes problem when the discharge time constant of $C_{FIN} \cdot (R_1+R_2)$ is long. Under such the circuit condition, it is recommended to discharge the C_{VCC} forcedly and to make the V_{CC} low value: This makes the OVP-reset time fast.

Similar circuit is used to make the V_{CC} low, when the reset of OVP is done by the external signal.

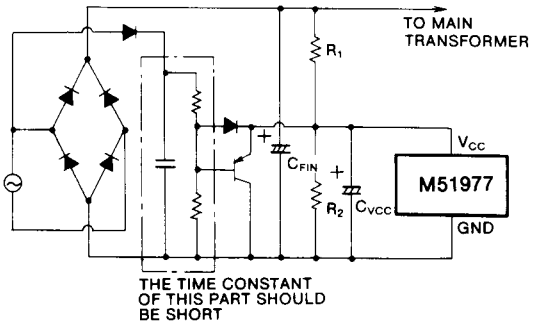

Fig. 29 Example circuit diagram to make the OVP-reset-time fast

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(3)OVP setting method using the induced third winding voltage on fly back system

For the over voltage protection (OVP), the induced fly back type third winding voltage can be utilized, as the induced third winding voltage depends on the output voltage. Fig. 30 shows one of the example circuit diagram.

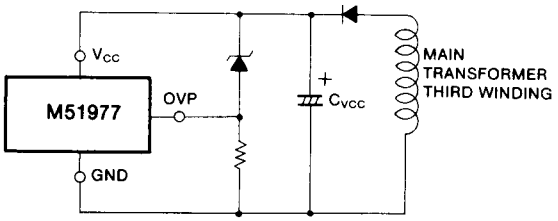


Fig. 30 OVP setting method using the induced third winding voltage on fly back system

Current limitting circuit

(1)Peripheral circuit of CLM+, CLM− terminal

Fig.31 and 32 show the example circuit diagrams around the CLM+ and CLM− terminal. It is required to connect the low pass filter, in oder to reduce the spike current component, as the main current or drain current contains the spike current especially during the turn-on duration of MOS-FET.

1,000pF to 22,000pF is recommended for C_{NF} and the R_{NF1} and R_{NF2} have the functions both to adjust the "current-detecting-sensitivity" and to consist the low pass filter.

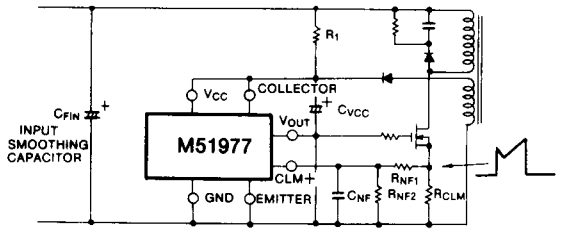


Fig. 31 Peripheral circuit diagram of CLM+ terminal

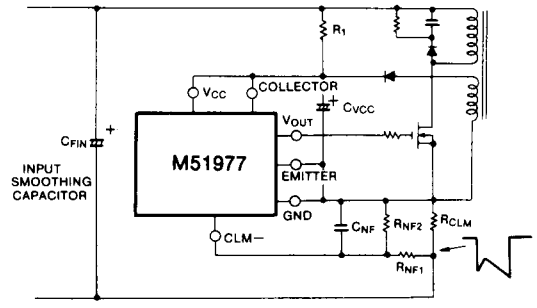


Fig. 32 Peripheral circuit diagram of CLM− terminal

To design the R_{NF1} and R_{NF2}, it is required to consider the influence of CLM terminal source current (I_{INCLM+} or I_{INCLM-}), which value is in the range of 90 to 270μA.

In order to be not influenced from these resistor paralleled value of R_{NF1} and R_{NF2}, ($R_{NF1}//R_{NF2}$) is recommended to be less than 100Ω.

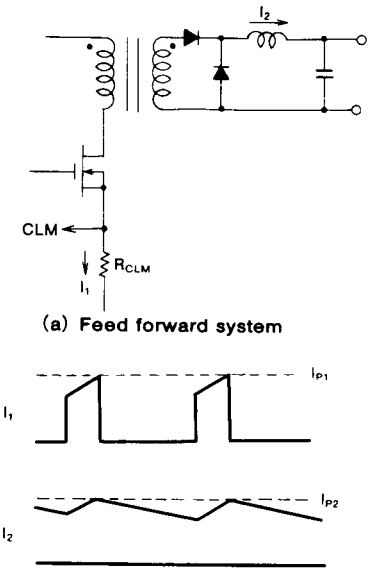
The R_{CLM} should be the non-inductive resistor.

(2)Over current limitting curve

(a)In case of feed forward system

Fig. 33 shows the primary and secondary current waveforms under the current limitting operation.

At the typical application of pulse by pulse primary current detecting circuit, the secondary current depends on the primary current. As the peak value of secondary current is limitted to specified value, the characteristics curve of output voltage versus output current become to the one as shown in Fig. 34.



(a) Feed forward system

(b) Primary and secondary current

Fig. 33 Primary and secondary current waveforms under the current limitting operation condition on feed forward system

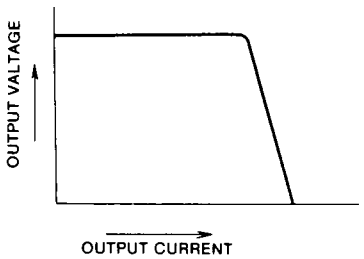


Fig. 34 Over current limitting curve on feed forward system

The demerit of the pulse by pulse current limitting system is that the output pulse width can not reduce to less than some value because of the delay time of low pass filter connected to the CLM terminal and propagation delay time T_{PDCLM} from CLM terminal to output terminal of type M51977. The typical T_{PDCLM} is 150ns.

As the frequency becomes higher, the delay time must be shorter. And as the secondary output voltage becomes higher, the dynamic range of on-duty must be wider; it means that it is required to make the on-duration much more narrower. So this system has the demerit at the higher oscillating frequency and higher output voltage applications.

To improve these points, the oscillating frequency is set low using the characteristics of VF terminal. When the current limitting circuit operates under the over current condition, the oscillating frequncy decreases in accordance with the decrease of VF terminal voltage, if the VF is lower than 3.5V. And also the dead time becomes longer.

Under the condition of current limitting operation, the output current I_2 continues as shown in Fig. 33. So the output voltage depends on the product of the input primary voltage V_{IN} and the on-duty.

If the third winding polarity is positive, the V_{CC} depends on V_{IN}, so it is concluded that the smoothed voltage of V_{OUT} terminal depends on the output DC voltage of the SMPS.

So the sharp current limitting characteristics will be got, if the V_{OUT} voltage is feed back to VF terminal through low pass filter as shown in Fig. 35.

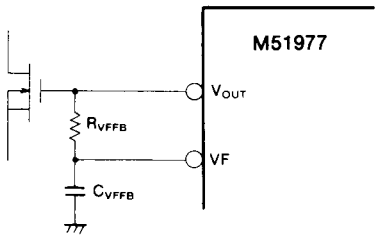


Fig. 35 Feed back loop through low pass filter from V_{OUT} to VF terminal

It is recommended to use 15kΩ for R_{VFFB}, and 10,000pF for C_{VFFB} in Fig.35.

Fig. 36 shows how to control the knee point where the frequency becomes decrease.

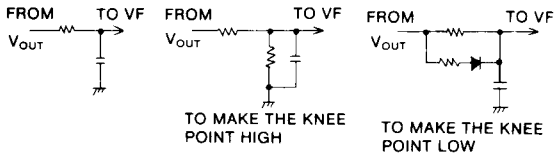


Fig. 36 How to control the knee point

(b) In case of fly back system

The DC output voltage of SMPS depends on the V_{CC} voltage of type M51977 when the polarity of the third winding is negative and the system is fly back. So the operation of type M51977 will stop when the V_{CC} becomes lower than "Operation-stop voltage" of M51977 when the DC output voltage of SMPS decreases under specified value at over load condition.

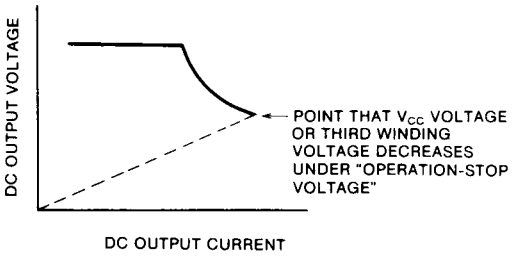


Fig. 37 Over current limitting curve on fly back system

However, the M51977 will non-operate and operate intermittently, as the V_{CC} voltage rises in accordance with the decrease of I_{CC} current.

The fly back system has the constant output power characteristics as shown in Fig. 37 when the peak primary current and the operating frequency are constant.

To control the increase of DC output current, the operating frequncy is decreased using the characteristics of VF terminal when the over current limitting function begins to operate.

The voltage which made by dividing the V_{CC} is applied to VF terminal as shown in Fig.38, as the induced third winding voltage depends on the DC output voltage of SMPS.

15kΩ or less is recommended for R_2 in Fig. 38, it is noticed that the current flows through R_1 and R_2 will superpose on the $I_{CC(START)}$ current.

If the R_1 is connected to C_{VCC2} in Fig. 27, the current flows through R_1 and R_2 is independent of the $I_{CC(START)}$.

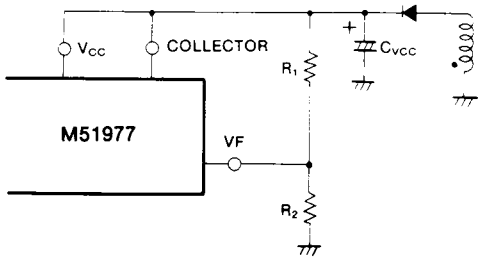


Fig. 38 Circuit diagram to make knee point low on fly back system

(c) Application circuit to keep the non-operating condition when over load current condition will continue for specified duration

The CT terminal voltage will begin to rise and the capacitor connected to CT terminal will be charged-up, if the current limitting function starts and VF terminal voltage decreases below V_{THTIME}(≃3V).
If the charged-up CT terminal voltage is applied to OVP terminal through the level-shifter consisted of buffer transistor and resistor, it makes type M51977 keep non-operating condition.

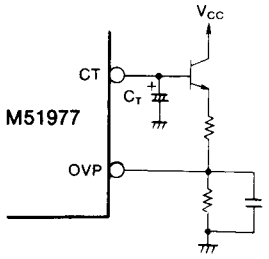


Fig. 39 Application circuit diagram to keep the non-operating condition when over load current condition will continue for specified duration

Output circuit

(1)The output terminal characteristics at the V_{CC} voltage lower than the "Operation-stop" voltage

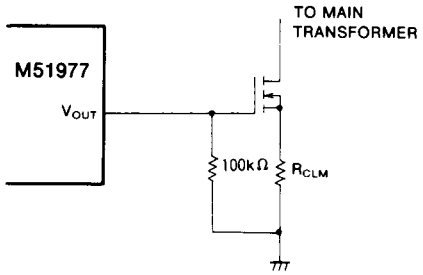


Fig. 40 Circuit diagram to prevent the MOS-FET gate potential rising

The output terminal has the current sink ability even though the V_{CC} voltage lower than the "Operation-stop" voltage or $V_{CC(STOP)}$. (It means that the terminal is "Output low state" and please refer characteristics of output low voltage versus sink current.)
This characteristics has the merit not to damage the MOS-FET at the stop of operation when the V_{CC} voltage decreases lower than the voltage of $V_{CC(STOP)}$, as the gate charge of MOS-FET, which shows the capacitive load characteristics to the output terminal, is drawn out rapidly.
The output terminal has the draw-out ability above the V_{CC} voltage of 2V, however, lower than the 2V, it loses the ability and the output terminal potential may rise due to the leakage current.
In this case, it is recommended to connect the resistor of 100kΩ between gate and source of MOS-FET as shown in Fig. 40.

(2)MOS-FET gate drive power dissipation

Fig. 41 shows the relation between the applied gate voltage and the stored gate charge.
In the region ①, the charge is mainly stored at C_{GS} as the depletion is spread and C_{GD} is small owing to the off-state of MOS-FET and the high drain votage.
In the region ②, the C_{GD} is multiplied by the "mirror effect" as the characteristics of MOS-FET transfers from off-state to on-state.
In the region ③, both the C_{GD} and C_{GS} affect to the characteristics as the MOS-FET is on-state and the drain voltage is low.

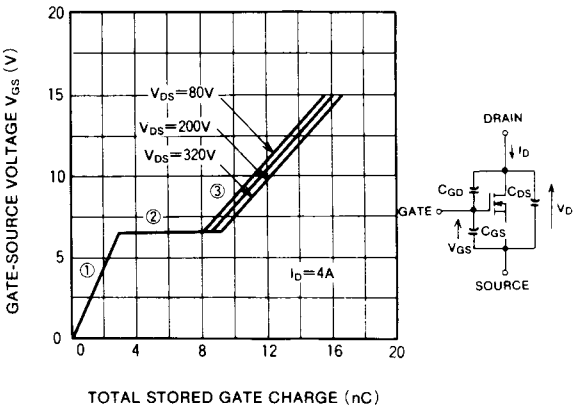


Fig. 41 The relation between applied gate-source voltage and stored gate charge

The charging and discharging current caused by this gate charge makes the gate power dissipation. The relation between gate drive current I_D and total gate charge Q_{GSH} is shown by following equation;

$$I_D = Q_{GSH} \cdot f_{OSC} \quad \cdots\cdots (1)$$

Where

f_{OSC} is switching frequency

As the gate drive current may reach up to several tenths milliampere at 500kHz operation, depending on the size of MOS-FET, the power dissipation caused by the gate current can not be neglected.
In this case, following action will be considered to avoid heat up of type M51977.

(1) To attach the heatsink to type M51977
(2) To use the printed circuit board with the good thermal conductivity
(3) To use the buffer circuit shown next section

(3)Output buffer circuit

It is recommended to use the output buffer circuit as shown in Fig. 42, when type M51977 drives the large capacitive load or bipolar transistor.

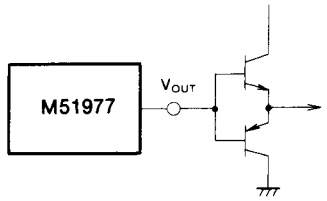


Fig. 42 Output buffer circuit diagram

DET

Fig. 43 shows how to use the DET circuit for the voltage detector and error amplifier.

For the phase shift compensation, it is recommended to connected the CR network between DET terminal and F/B terminal.

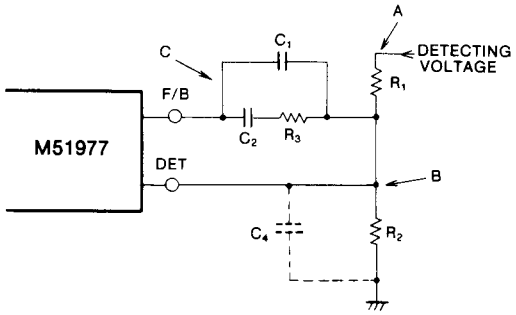


Fig. 43 How to use the DET circuit for the voltage detector

Fig. 44 shows the gain-frequency characteristics between point B and point C shown in Fig. 43.

The G_1, ω_1 and ω_2 are given by following euqations;

$$G_1 = \frac{R_3}{R_1 // R_2} \quad \cdots\cdots (11)$$

$$\omega_1 = \frac{1}{C_2 \cdot R_3} \quad \cdots\cdots (12)$$

$$\omega_2 = \frac{C_1 + C_2}{C_1 \cdot C_2 \cdot R_3} \quad \cdots\cdots (13)$$

At the start of the operation, there happen to be no output pulse due to F/B terminal current through C_1 and C_2, as the potential of F/B terminal rises sharply just after the start of the operation.

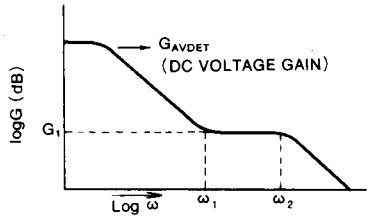


Fig. 44 Gain-frequency characteristics between point B and C shown in Fig. 43

Not to lack the output pulse, is recommended to connect the capacitor C_4 as shown by broken line.

Please take notice that the current flows through the R_1 and R_2 are superposed to $I_{CC(START)}$. Not to superpose, R_1 is connected to C_{VCC2} as shown in Fig. 27

How to get the narrow pulse width during the start of operation

Fig. 45 shows how to get the narrow pulse width during the start of the operation. If the pulse train of forcedly narrowed pulse-width continues too long, the misstart of operation may happen, so it is recommended to make the output pulse width narrow only for a few pulse at the start of operation. 0.1μF is recommended for the C.

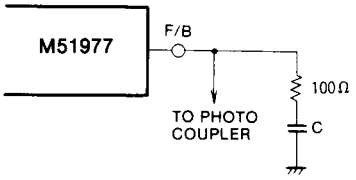


Fig. 45 How to get the narrow pulse width during the start of operation

How to synchronize with external circuit

Type M51977 has no function to synchronize with external circuit, however, there is some application circuit for synchronization as shown in Fig. 46. If this circuit is used, the synchronization may be out of order at the overload condition when the current limitting function starts to operate and VF terminal voltage becomes lower than 3V.

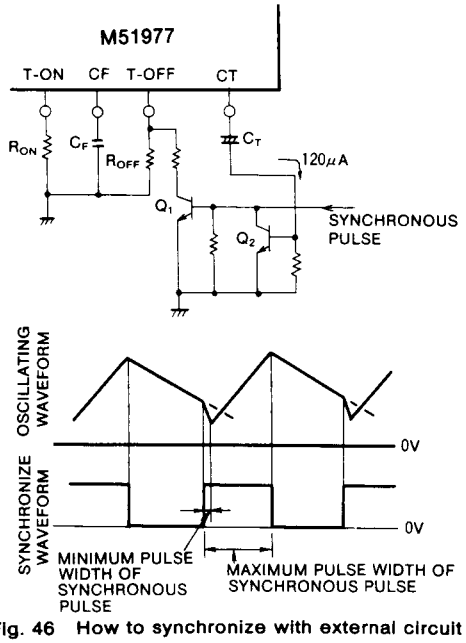


Fig. 46 How to synchronize with external circuit

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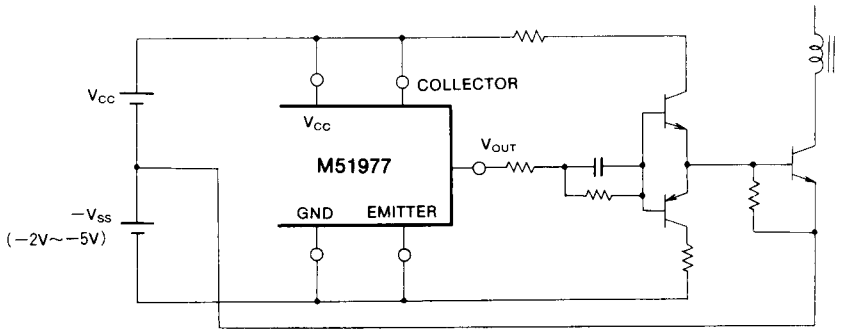


Fig. 47 Driver circuit diagram (1) for bipolar transistor

Driver circuit for bipolar transistor

When the bipolar transistor is used instead of MOS-FET, the base current of bipolar transistor must be sinked by the negative base voltage source for the switching-off duration, in order to make the switching speed of bipolar transistor fast one.

In this case, over current can not be detected by detecting resistor in series to bipolar transistor, so it is recommended to use the CT(current transformer).

For the low current rating transistor, type M51977 can drive it directly as shown in Fig. 48.

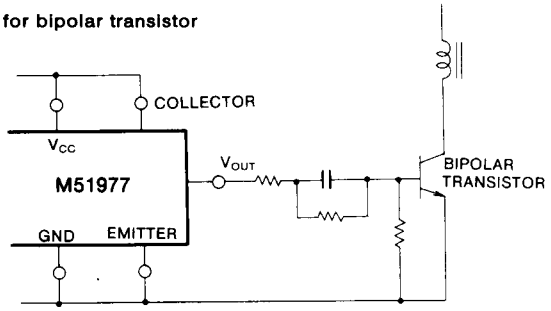


Fig. 48 Driver circuit diagram (2) for small bipolar transistor

Attention for heat generation

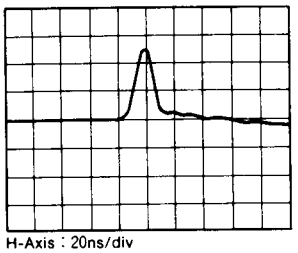
The maximum ambient temperature of type M51977 is + 85°C, however, the ambient temperature in vicinity of the IC is not uniform and varies place by place, as the amount of power dissipation is fearly large and the power dissipation is generated locally in the switching regulator.

So it is one of the good idea to check the IC package temperature. The temperature difference between IC junction and the surface of IC package is 15°C or less, when the IC junction temperature is measured by temperature dependency of forward voltage of pn junction, and IC package temperature is measured by "thermo-viewer", and also the IC is mounted on the "phenol-base" PC board in normal atmosphere.

So it is concluded that the maximum case temperature (surface temperature of IC) rating is 120°C with adequate margin. It is noticed that the minimum thermal protection operating temperature is 120°C.

As type M51977 has the modified totempole driver circuit, the transient through current is very small and the total power dissipation is decreased to the reasonable power level.

Fig. 49 shows the transient rush (through) current waveforms at the rising and falling edges of output pulse, respectively.



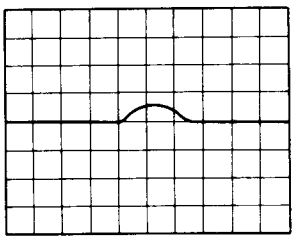


Fig. 49 Through current waveforms of totempole driver circuit at no-load and V_{CC} of 18V condition

APPLICATION EXAMPLE

Feed forward types SMPS with multi-output.