AN316
Application note

Transil™ clamping protection mode

Introduction

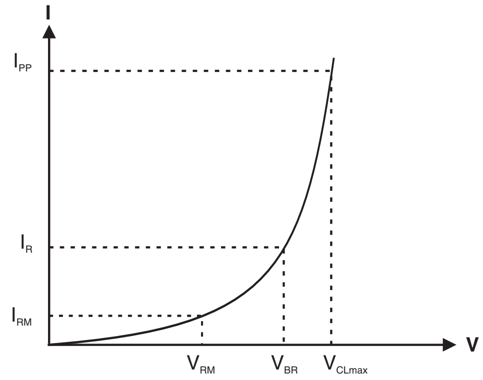
The Transil[a] is an avalanche diode specially designed to clamp over voltages and dissipate high transient power. A Transil has to be selected in two steps:

- Check that the circuit operating conditions do not exceed the specified limit of the component.
  - For non-repetitive surge operation,
  - For repetitive surge operation,
  - For normal operation.
- Check that the maximum value of the clamped voltage under the worst conditions corresponds to the specification of the circuit.

a. Transil is a trademark of STMicroelectronics

1 Review of the Transil characteristics

Figure 1. Main characteristics of a Transil



1.1 Stand off voltage

V_{RM} is the voltage that the Transil can withstand in normal operation.

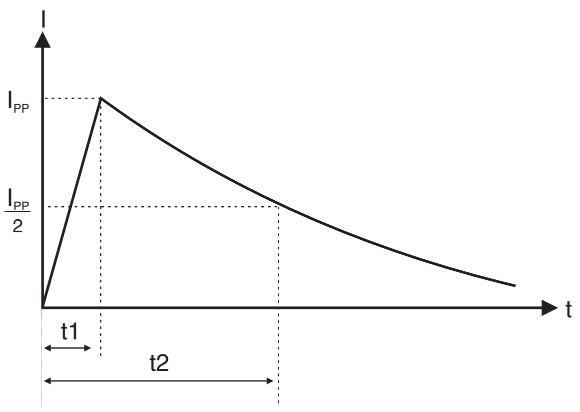
1.2 The breakdown voltage or knee voltage

V_{BR} is the voltage value above which the current in the Transil increases very fast for a slight increase in voltage. The breakdown voltage V_{BR} is specified at 25 °C and its temperature coefficient is positive.

1.3 The clamping voltage

V_{CL} as specified in the data-sheets is the maximum value for a "*standard*" current pulse with a peak value of I_{PP}, specified for any type of Transil (*Figure 2*). If the Transil is subjected to a different pulse, the value of V_{CL} can be calculated using the application note "*Calculation of Transil apparent dynamic resistance*". The clamping factor is represented by V_{CL}/V_{BR}. This ratio between the maximum value of over voltage for a given current and the maximum voltage that the diode can withstand in normal operation characterizes the degree of protection.

Figure 2. Standard exponential pulse



	t1	t2
Wave “8/20µs”	8	20
Wave “10/1000µs”	10	1000

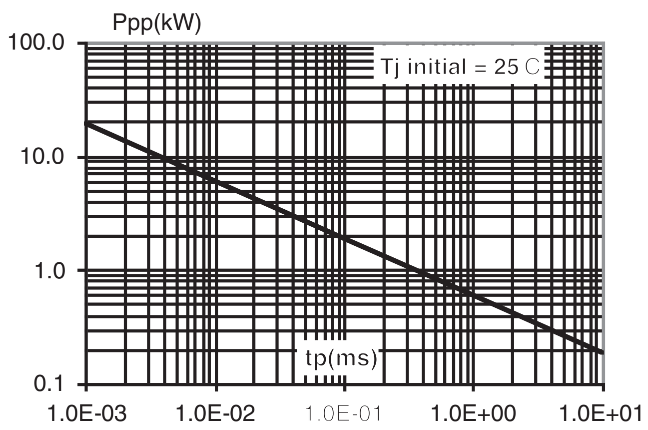
This type of pulse corresponds to most of the standards used for the protection device.

2 Transil peak power dissipation

One of the goals of the Transil is to protect equipment against transient disturbances. The duration of these transients is linked to the application where the Transil operates. For example electrostatic discharges (ESD) are in the range of tens of ns while industrial strikes are within tens of µs, telecom over-voltages, hundreds of µs and automotive surges tens of ms.

The performance of the Transil are given in the datasheet for both 8/20 µs and 10/1000 µs waves (V_{CL}, I_{PP}), otherwise the curve peak pulse power versus pulsed duration (see *Figure 3*) allows the designer to choose the right Transil for his application.

Figure 3. Peak pulse power versus exponential pulse duration for SMCJ series



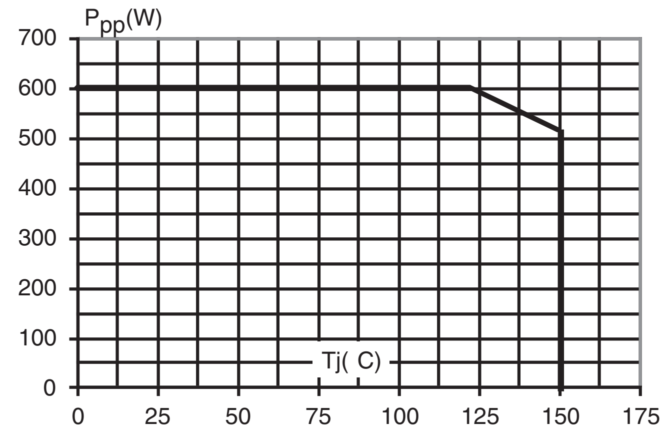
Equation 1Peak pulse power versus exponential pulse duration for SMCJ series

$$P_{PP} = V_{CL} \times I_{PP}$$

This maximum corresponds to non-repetitive operation. If the pulse has a different duration, a curve similar to *Figure 3* is provided in the datasheets and enables the specifications of the Transil to be determined.

If the initial temperature exceeds 25 °C, the power (P_{PP}) should be reduced in accordance with the curve of *Figure 4*, which is the same for all Transils.

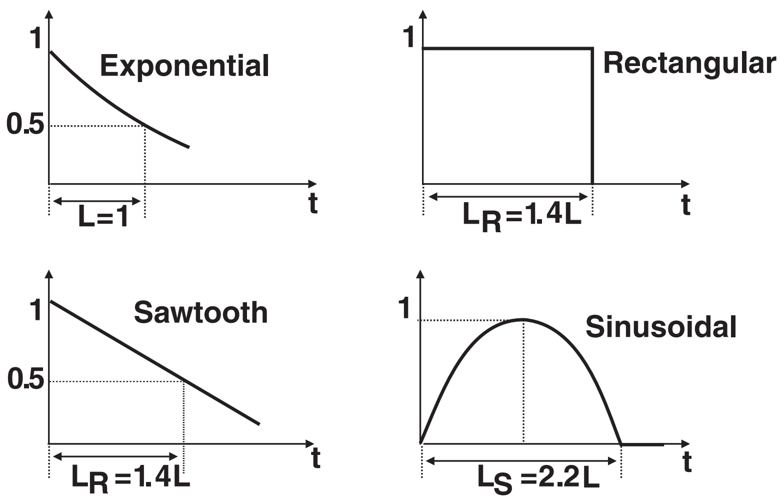
Figure 4. Variation of peak power as a function of the initial Temperature



If the current through the Transil is not exponential, the diagrams of *Figure 5* should enable the equivalent exponential pulse to be calculated.

For example, the rectangular pulse, which gives the same dissipation as the exponential pulse of the same peak value, is 1.4 times longer.

Figure 5. Curves giving the same dissipation



3 Transil average power dissipation

In repetitive operation, the specification to be considered is mean power.

Equation 2

$$P_{AV} = f \times W$$

(f: frequency, W: energy dissipated at each pulse)

The junction temperature calculated from this power should never exceed the specified maximum junction temperature. This temperature is calculated from the thermal resistance, exactly like for a diode.

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Equation 3

$$T_j = T_{amb} + R_{th(j\text{-}a)} \times P_{AV}$$

4 Speed

4.1 Component technology effect

In the world of clamping protection, there are two major kinds of devices: varistors and Transils. *Table 1* gives some differences between both families. Please note that the chosen varistor family is the most performant one, which is based on multilayer technology.

Table 1. Differences between varistor and Transil

	Varistor	Transil
Topology	Bidirectional	Uni or Bidirectional
Leakagecurrent	< 5 µA	< 1 µA
8/20µs Clamping factors (= Vcl / Vbr)	2.00	1.5
ESD ruggedness	> 30 kV	> 30 kV
ESD clamping voltage	See *Figure 6*	See *Figure 6*
Ageing	Yes, see *Figure 7*	Yes, see *Figure 7*

Figure 6. ESD behavior for both varistor and Transil

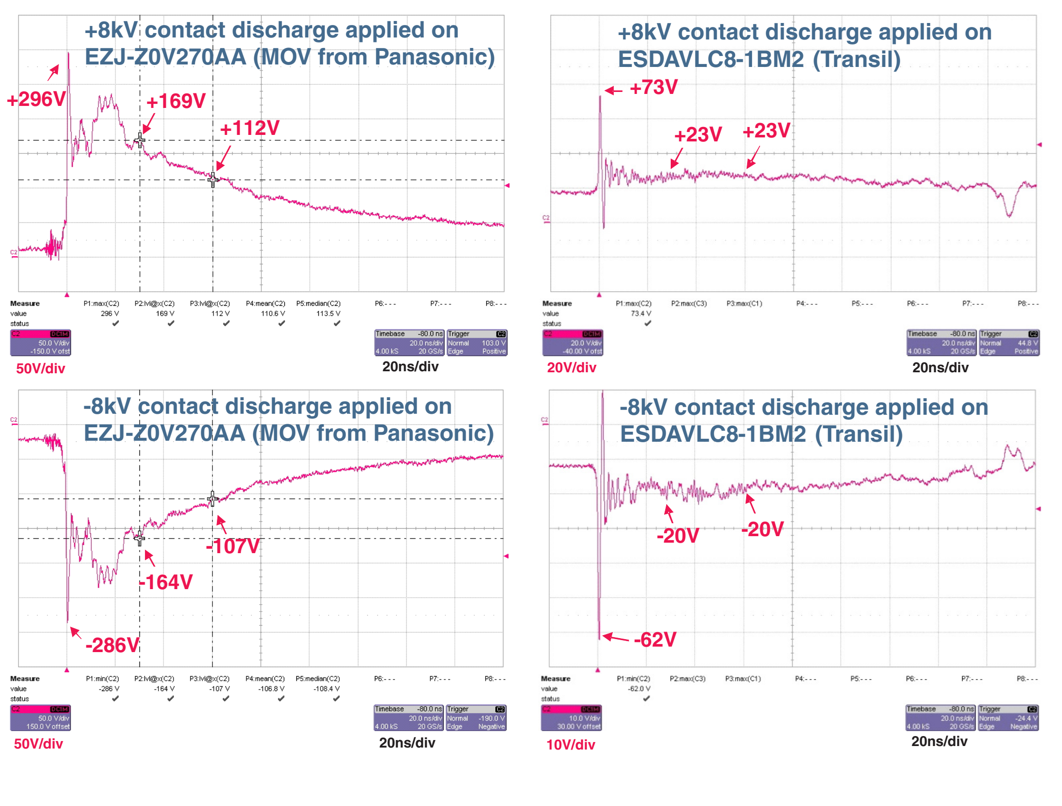


Figure 6 shows the remaining voltage comparison between varistor and Transil when they are submitted to *ESD IEC 61000-4-2 level 4* contact discharge surge. The remaining peak value is smaller and shorter in duration for Transil than for varistor.

Figure 7. Aging effect on both varistor and Transil characteristics

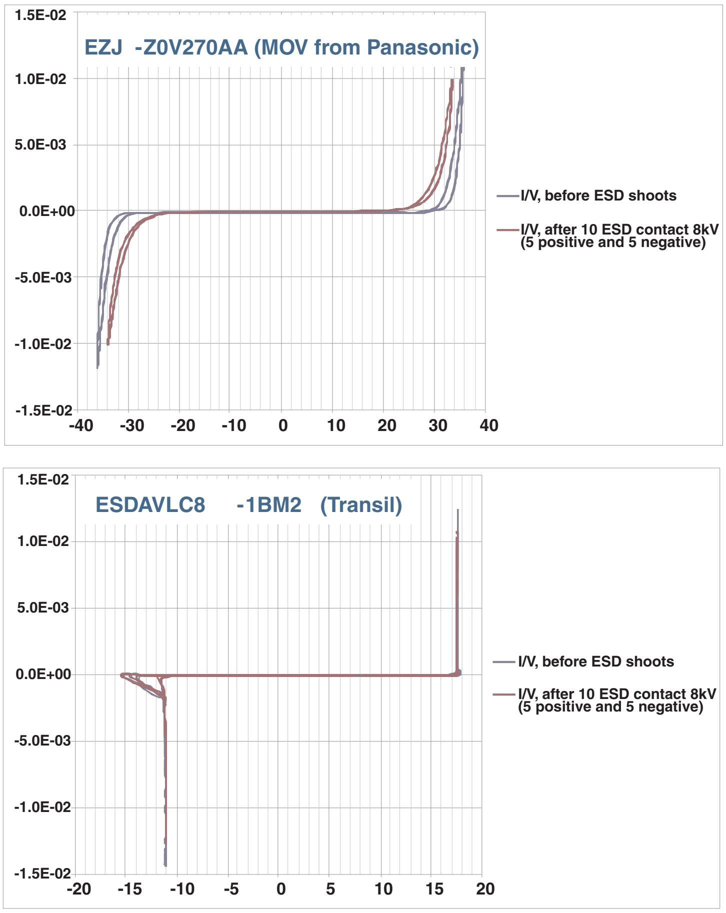


Figure 7 shows the impact of repetitive ESD IEC 61000-4-2 level 4 contact discharge surges. After 10 surges, the I/V characteristics of the varistor changed while the Transil one presents no change.

4.2 Connection effect

Figure 8. Example of PCB Layout

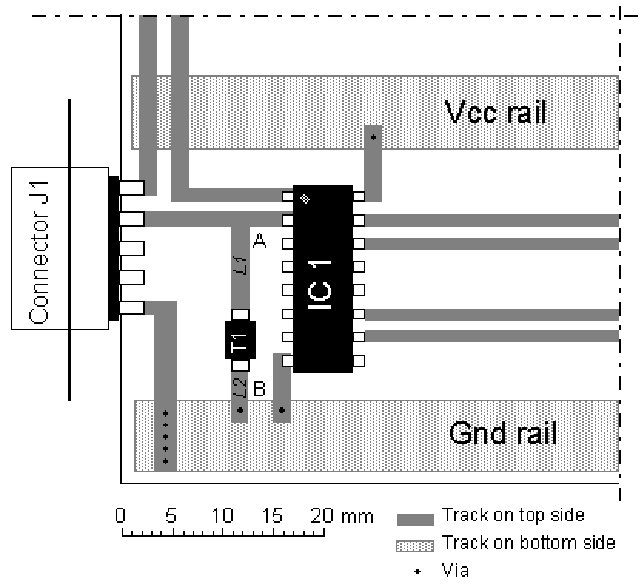


Figure 8 gives an example of a PCB Layout. On this portion of PCB, an integrated circuit (IC1) is connected to outside equipment through the connector J1. A cable can be hot plugged in J1 and then causes ESD on all the lines linked to J1. In this case the pin 2 of IC1 is connected to the pin 2 of the connector J1 and the Transil T1 assumes the protection of this line.

When a surge occurs on pin 2 of the connector, this is clamped by T1. During the surge, the remaining voltage at the pin 2 level of IC1 is the potential difference between both points A and B.

In case of ESD, the rise time of the surge is within 1 ns and we have to take into account the parasite inductances located between A and T1 (L1) and T1 and B (L2). So the remaining voltage seen by the protected circuit is equal to the sum of the clamping voltage V_{CL} of T1 and the voltage induced by L1 and L2.

In case of *Figure 8*, the Track length between A and T1 is 10mm and between T1 and B is 5 mm. We can estimate the parasitic inductance of the track at 1 nH/mm, so L1 ≈ 10 nH and L2 ≈ 5 nH. The remaining voltage between A and B is equal to:

Equation 4

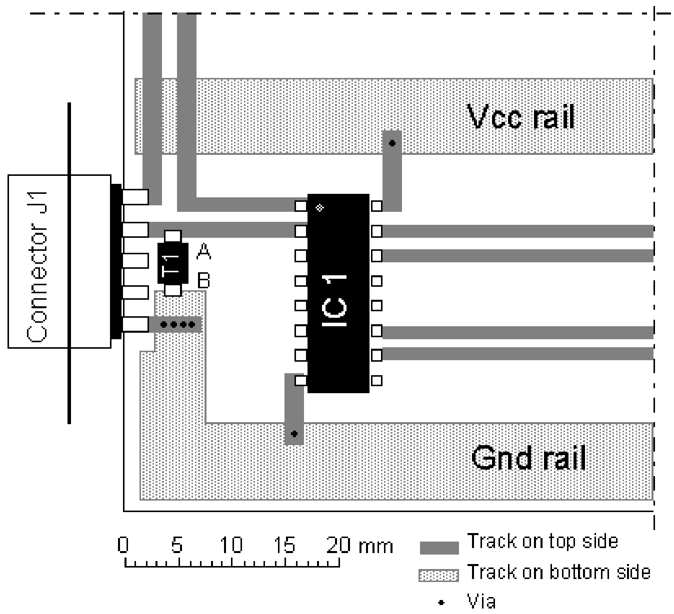
$$V_{CL} + (L1 + L2) \times \frac{di}{dt} = V_{CL} + (10 + 5) \times 10^{-9} \times \frac{20}{10^{-9}} V$$

$$= V_{CL} + 300V$$

With $\frac{di}{dt} = 20\ A/ns$ value measured during IEC 61000-4-2 8 kV contact discharge ESD Test.

In this case an extra voltage of 300 V is due to the PCB tracks. *Figure 9* gives a solution to this problem.

Figure 9. Solution of parasitic inductance's problem



In this PCB configuration, the parasitic inductance can be estimated as for the T1 package, let say roughly 0.5 nH. So the extra voltage now becomes 10 V instead of 300 V.

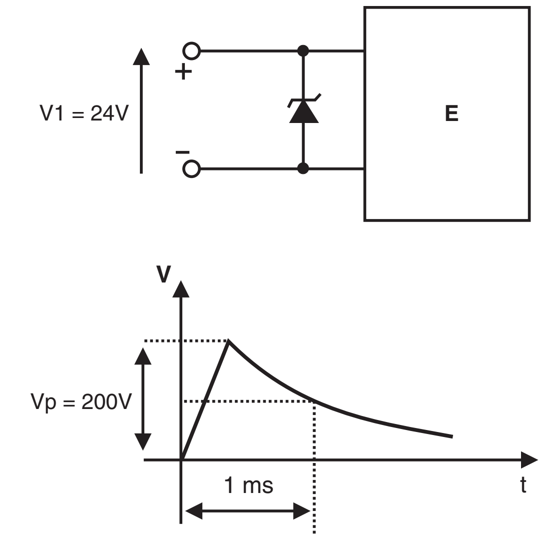
5 Calculation example

5.1 Non-repetitive surges

A source (V1) with a rated voltage of 24 V supplies equipment E, which has to be protected against over voltages. This source is subjected to random non-repetitive exponential over voltage with amplitude of 200 V and a duration of 1 ms at 50% (standard wave) (see *Figure 10*). The equivalent internal impedance Z of the source with respect to 1 ms exponential waves is 13 Ω.

The maximum ambient temperature is 75 °C. In no circumstances should equipment E be subjected to a voltage higher than 50 V.

Figure 10. Protected equipment and surge



5.1.1 Selection of the protection voltage

In the absence of specific information, we assume that voltage V1 varies by ± 20%, i.e. between 20 V and 29 V.

The protection voltage V_{RM} of the Transil should then be greater than or equal to 29 V.

5.1.2 Predetermination of the peak power P_P

Equipment E cannot withstand a voltage above 50 V → $V_{CL} \leq 50$ V.

Assuming that there is a Transil that meets this criterion, an initial calculation of the Transil power can be made:

Equation 5

$$P_P = V_{CL} \times I_P \text{ where } I_P = \frac{V_P - V_{CL}}{Z}$$

$$I_P = \frac{+200\ V - 50\ V}{13\ \Omega} = 11.5\ A$$

$$P_P = 50\ V \cdot 11.5\ A = 575\ W$$

This power corresponds to an operating temperature of 75 °C. The data sheets indicate the power at 25 °C, so we have to correct the power according to the curves of admissible power versus initial temperature (see *Figure 4*).

Equation 6:Thus we obtain

$$P_P(25\,°C) = \frac{P_P(75\,°C)}{0.8}$$

$$P_P(25\,°C) = \frac{575\ W}{0.8} = 719\ W$$

5.1.3 Selection of the Transil

We can now establish an initial specification of the Transil to use.

Equation 7:

$$V_{RM} \geq 29\ V$$

$$V_{RM} \leq 50\ V \text{ for } I_P = 11.5\ A$$

$$P_P(25°C) = 719\ W\ /1ms$$

The ST product type corresponding to these characteristics is the *SMCJ30A*.

Equation 8:

$$V_{RM} = 30\ V$$

$$V_{BRmin} = 33.3\ V$$

$$V_{CLmax} = 48.4V\ ;\ I_{PP} = 32\ A$$

$$P_P = 1500\ W/1ms$$

$$\alpha_T = 9.9 \times 10^{-4}/°C$$

5.1.4 Determination of the clamping voltage V_{CL}

To determine the voltage V_{CL} at 11.5 A, let us use the I_{PP}/V_{CL} parameters included in the SMCJ30A datasheet.

Equation 9

$$V_{CLmax}(at\ I_P) \approx V_{BRtyp} + R_D \times I_P$$

$$R_D \leq \frac{V_{CL} - V_{BR}}{I_{PP}}$$

$$V_{CL}(at\ 11.5A) \approx 35.05 + \frac{48.4 - 35.05}{32} \times 11.5\ (V)$$

$$= 39.84V$$

Where $V_{BRtyp} = V_{BRmin} / 0.95 = 34.05$ V

5.1.5 Temperature correction

The voltage at 75 °C is:

Equation 10

$$V_{CL}(T_j) = V_{CL}(25\,°C) \times [1 + \alpha T \times (T_j - 25°C)]$$

$$V_{CL}(75°C) = 39.84 \times [1 + 9.9 \times 10^{-4} \times (75°C - 25°C)]\ (V)$$

$$V_{CL}(75°C) = 41.81\ V$$

This value is below the 50 V limit. This Transil ensures the protection.

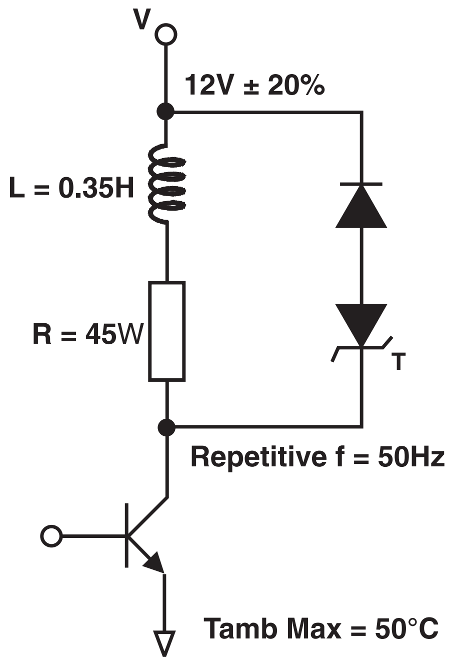
5.2 Repetitive surges

We have to protect the transistor shown in*Figure 11* with a Transil having its clamping voltage, V_{CL} which does not exceed 85 V.

5.2.1 Calculation method

To avoid a long calculation we assume that $V_{CL} \approx V_{BR}$, which is true only in the case of repetitive surges.

Figure 11. Transistor protection



Experience shows that this hypothesis is confirmed in most cases with a Transil. Therefore the Transil should be initially selected according to its thermal characteristics.

P_{AV}

An approximate value can be obtained by supposing that the Transil absorbs the energy contained in the inductance. This hypothesis is close to reality when the ratio:

$\frac{V_{BR}}{V}$ is significant.

Equation 11:

$$P_{AV} = \frac{1}{2} \times L \times I^2 \times f = \frac{1}{2} \times 0.35 \times \left[\frac{12 + 2.4}{45}\right]^2 \times 50 (W)$$

$$= 0.9 W$$

5.2.2 First choice

We choose ST product type SMCJ70A.

Equation 12

$$V_{BRmax} = 85.58 V$$
$$R_{th} = 75 °C / W$$
$$\alpha_T = 10.5 \times 10^{-4} / °C$$

With V_{BRmax} = 1.1 x V_{BRmin}= 85.58V.

5.2.3 T_j calculation

Equation 13

$$T_j = T_{amb} + P_{AV} \times R_{th} = 50 + 67.5\,(°C) = 117.5°C$$

This value is compatible with the Transil characteristics.

5.2.4 Determination of V_{CL}

We see on the data sheets that for such a low current level $V_{CL} \approx V_{BRmax}$.

5.2.5 Temperature correction

Equation 14

$$V_{CL}(117.5°C) = V_{CL}(25°C) \times [1 + \alpha T \times (117.5° - 25°)]$$

$$V_{CL}(117.5°C) = 93.9V$$

This value is too high.

5.2.6 Second choice

Equation 15

$$\text{SMCJ 58 A} \quad V_{BRmax} = 70.84\,V$$

$$\alpha_T = 10.4 \times 10^{-4} / °C$$

$$V_{CL}(117.5°C) = 77.65V$$

The *SMCJ58A* Transil is suitable for this application.

6 Revision history

Table 2. Document revision history

Date	Revision	Changes
Oct-2001	3	Previous version
29-Jul-2014	4	Updated for new products.

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