

Design: F. Rimatzki
This circuit was originally designed to control the brightness of an electric torchlight, but may find many other applications because of its high efficiency, ease of operation and ability to control (lamp) loads drawing several amps. The dimmer offers brightness control from nil to maximum in 16 steps by means of a small push-button. When the push-button is released, the selected brightness is retained. One of the most remarkable things about this circuit is that it hardly adds to the battery load, its own current consumption amounting to no more than about 4 mA (at a battery voltage of 3.5 V ).
The 16 discrete brightness values are obtained by comparing two counter states. One of these actually determines the lamp brightness, while the other performs a cyclic count from 0 to 15. The lamp current is then only switched on if the second value is smaller than or equal to the first. To make sure the switching losses remain as small
as possible, a power MOSFET with a very low on-resistance is used. The BUZ10 used here does, however, call for a drive voltage of at least 6 V , so that an additional voltage step-up converter is required.
Counter IC2b only acts as a bistable to allow the circuit to be switched on by means of the lamp brightness push-button, Sl. The circuit is switched off (current consumption: less than $5 \mu \mathrm{~A})$ if output Q0 of IC2b (pin 11) supplies a logic high level. The $27-\mathrm{kHz}$ (approx.) oscillator built from gates ICla, IClb and IClc is then disabled, so that the outputs of ICla and IClb are logic high. The ICs in the circuit are then powered via choke Ll and the output transistors of ICla and IClb. This is unusual but possible because these transistors can also pass a voltage level at the IC outputs to the supply connection, instead of the other way around (which is far more usual). Because of the logic-high level at the reset inputs of counters IC3 and IC2a, comparator IC4 receives input


data which causes it to pull its $\mathrm{P}<\mathrm{Q}$ output (pin 12) logic high. The result is that inverter IClf pinches off the BUZ10 MOSFET, and the lamp remains off. When the push-button is actuated for the first time, the bistable in IC2b receives a clock pulse from switch debouncing circuit IClc-ICld. Next, the counters and the oscillator are enabled. The duty factor of the oscillator signal is determined by resistors R1 and

R2. The oscillator output signal is filtered by R3 and C1. Although the step-up converter is only capable of supplying a few mA , that is sufficient for the CMOS ICs and the BUZ10 MOSFET. For battery voltages between 3 and 6 V , the indicated values of R1 and R2 enable a voltage of 8.5 V to about 16 V to be created for powering the ICs and driving the BUZ10.
As long as the push-button is held depressed, the level at the

| COMPONENTS LIST | L1 $=10 \mathrm{mH}$ choke |
| :--- | :--- |
|  |  |
| Resistors: | Semiconductors: |
| R1 $=39 \mathrm{k} \Omega$ | D1,D2 $=1$ NN148 |
| R2 $\mathrm{R} 4=120 \mathrm{k} \Omega$ | T1 $=$ BUZ10 (Siemens) |
| R3 $=10 \Omega$ | IC1 $=4049$ |
| R5 $=47 \mathrm{k} \Omega$ | IC2 $=4520$ |
|  | IC3 $=4060$ |
| Capacitors: | IC4 $=4585$ |
| C1,C2 $=2 \mu$ F2 63 V radial | Miscellaneous: |
| C3 $=270 \mathrm{pF}$ ceramic | S1 = push-button, 1 make |
| C4 $=4 \mathrm{nF7} 7$ | contact |
| C5-C8 $=100 \mathrm{nF}$ | Bt1 $=$ torchlight battery, 3-6V |
| Inductor: | La $1=$ torchlight lamp |

cascading input of IC4, pin 4, causes the $\mathrm{P}>\mathrm{Q}$ output, pin 13, to be enabled, so that IC3 is clocked. The counter slowly increases the value at the ' P ' inputs of the comparator, thereby controlling the duty factor (mark/space ratio) of the signal at the comparator's $\mathrm{P}<\mathrm{Q}$ output, pin 12. As soon as IC3 reaches its maximum counter state, the signal at pin 13 of IC4 no longer changes, so that the counter is not started at 0 again. The $\mathrm{P}<\mathrm{Q}$ output then also remains at 0 , so that Tl is driven hard and the lamp lights at maximum brightness. If the push-button is released before the maximum brightness is reached, counter IC3 no longer receives clock pulses and 'freezes' at the current state,
causing the lamp to light at the selected brightness. The next action on Sl resets the entire circuit and switches the lamp off If so desired, the brightness control rate may be reduced by doubling or trebling the value of C3. To compensate the resultant drop in the IC supply voltage, the value of choke L1 then has to be increased proportionally. The IC supply voltage should always be between 8 V and 16 V (maximum value of 4000 series CMOS ICs).
The circuit is best built on a printed circuit board of which the templates are shown here. Unfortunately this board is not available ready-made through the Publishers.
(984075-1, Gb)

## 응

 battery-charging indicatorfor mains adaptor

Design: J. Gonzalez
Although you may well be the proud owner of the very latest NiCd battery charger, you may still come across the odd 'incompatible' battery, for example, one having a rare voltage or requiring a much higher charging current than can be supplied by your off-the-shelf charger. In these cases, many of you will resort to an adjustable mains adaptor (say, a $500-\mathrm{mA}$ type) because that is probably the cheapest way of providing the direct voltage required to charge the battery. Not fast and not very efficient, this 'rustic' charging system works, although subject to the following restrictions:

1. You should have some idea of the charging current. In case you use an adaptor

which is adjustable but of the unregulated, low output current type, you can adjust the current by adjusting the output voltage.
2. You have to know if the current actually flows through the battery. A current-detecting indicator is therefore
much to be preferred over a voltage indicator.
3. To prevent you from forgetting all about the charging cycle, the indicator should be visible from wherever you pass by frequently.

Using the circuit shown here,
the LED lights when the baseemitter potential of the transistor exceeds about 0.2 V . Using a resistor of $1 \Omega$ as suggested this happens at a current of about 200 mA , or about 40 mA if $\mathrm{R}_{1}$ is changed to $4.7 \Omega$.

The voltage drop caused by this indicator can never exceed the base-emitter voltage ( $\mathrm{U}_{\mathrm{BE}}$ ) of the transistor, or about 0.7 V . Even if the current through $\mathrm{R}_{1}$ continues to increase beyond the level at which $\mathrm{U}_{\mathrm{BE}}=0.7 \mathrm{~V}$, the base of the transistor will 'absorb' the excess current. The TO-220 style BU406 transistor suggested here is capable of accepting base currents up to 4 A.

Using this charging indicator you have overcome the restrictions 2 and 3 mentioned above.

What remains is the problem of knowing the required current. As long as $\mathrm{U}_{\mathrm{BE}}$ remains below 0.6 V or so, the voltage across $R_{1}$ is a faithful indication of the charging current. Alternatively, you may insert an ammeter to find out about the charging currents produced at different out-
put voltage settings on the adaptor. Next, you choose between reasonably fast charging, say, in about 5 hours using $\mathrm{C}(\mathrm{Ah}) / 5$, or slower, say, 10 hours at $\mathrm{C}(\mathrm{Ah}) / 10 . \mathrm{C}(\mathrm{Ah})$ is the battery capacity in (milli-) amperehours, which is usually printed on the battery. In general, the
lower the charging current, the smaller the risk of damage to the battery if you forget to switch off the charger.

In some cases it will be possible to incorporate the circuit into the mains adaptor. That may be dangerous, however, because of the presence of the mains volt-
age in the adaptor housing. A safer alternative is to install the circuit in a remote control box.

The circuit is not protected against reversal of the battery polarity. If such protection is required, a fuse or circuit breaker should be added.
[984083]

##  playback amplifier for cassette deck

## Design: T. Giesberts

For some time now, there have been a number of tape cassette decks available at low prices from mail order businesses and electronics retailers. Such decks do not contain any electronics, of course. It is not easy to build a recording amplifier and the fairly complex magnetic biasing circuits, but a playback amplifier is not too difficult as the present one shows.

The stereo circuits in the diagram, in conjunction with a suitable deck, form a good-quality cassette player. The distortion and frequency range (up to 23 kHz ) are up to good standards. Moreover, the circuit can be built on a small board for incorporation with the deck in a suitable enclosure.

Both terminals of coupling capacitor $\mathrm{C}_{1}$ are at ground potential when the amplifier is switched on. Because of the symmetrical $\pm 12 \mathrm{~V}$ supply lines, the capacitor will not be charged. If a single supply is used, the initial surge when the capacitor is being charged causes a loud click in the loudspeaker and, worse, magnetizes the tape.

The playback head provides an audio signal at a level of $200-500 \mathrm{mV}$. The two amplifiers raise this to line level, not linearly, but in accordance with the RIAA equalization characteristic for tape recorders. Broadly speaking, this characteristic divides the frequency range into three bands:

- Up to 50 Hz , corresponding to a time constant of 3.18 ms , the signal is highly and linearly amplified.
- Between 50 Hz and 1.326 kHz , corresponding to a time constant of $120 \mu \mathrm{~s}$, for normal tape, or 2.274 kHz ,

corresponding to a time constant of $70 \mu \mathrm{~s}$, for chromium dioxide tape, the signal is amplified at a steadily decreasing rate.
- Above 1.326 kHz or 2.274 kHz , as the case may be, the signal is slightly and linearly amplified.

This characteristic is determined entirely by $A_{1}\left(A_{1}{ }^{\prime}\right)$. To make the amplifier suitable for use with chromium dioxide tape, add a double-pole switch (for stereo) to connect a $2.2 \mathrm{k} \Omega$ resistor in parallel with $R_{3}\left(R_{3}\right)$.

The output of $A_{1}\left(A_{1}{ }^{\prime}\right)$ is applied to a passive high-pass
rumble filter, $\mathrm{C}_{3}-\mathrm{R}_{5}\left(\mathrm{C}_{3}{ }^{\prime}-\mathrm{R}_{5}{ }^{\prime}\right)$ with a very low cut-off frequency of 7 Hz . The components of this filter have exactly the same value as the input filter, $C_{1}-R_{1}$ $\left(\mathrm{C}_{1}{ }^{\prime}-\mathrm{R}_{1}{ }^{\prime}\right)$.

The second stage, $\mathrm{A}_{2}\left(\mathrm{~A}_{2}{ }^{\prime}\right)$ amplifies the signal $\times 100$, that is, to line level (1 V r.m.s.).

Capacitor $\mathrm{C}_{4}$ limits the upper frequency range to avoid r.f. interference and any tendency of
the amplifier to oscillate.
The amplifier needs a symmetrical $\pm 12 \mathrm{~V}$ power supply
that can provide a current of up to 0.5 A . The greater part of this current is drawn by the motor of
the deck; the electronic circuits draw only 15 mA .
[984113] memory change-over tip

## Design: L. Lemmens

When the contents of two existing memory address have to be interchanged for one reason or an other, there is usually a need for an additional address or variable:

MOV dummy, var1
MOV var1,var2
MOV var2,dummy

This dummy variable is not always necessary:

XOR var1,.var2
XOR var2,var1
XOR var1,var2
This tip may well be of use when the memory space is limited. It may also be used with
higher programming languages to save having to declare an additional variable.

## 9 improved power-down for the 8051

Design: G. Kleine
Members of the 8051 family of microcontrollers (MCS51) are well-known and widely used. The controllers have a powerdown mode in which the program processing is suspended by the clock oscillator and ended with a power-down instruction. To reduce the current drain, the supply voltage is reduced to a minimum of 2 V after the powered-down mode has been selected. This mode can only be disabled by a reset, for which the supply voltage needs to be returned to 5 V .

In simple applications of the 8051, the EPROM containing the program to be executed is enabled by making $\overline{\text { PSEN }}$ (program storage enable) active via its $\overline{\mathrm{OE}}$ (output enable) terminal. There are also circuits where $\overline{\text { PSEN }}$ acts on the $\overline{C S}$ (chip select) terminal of the EPROM.

Use of the power-down mode has a drawback: line ALE (address latch enable), like PSEN, remains low during the power-down mode and so holds the EPROM active. It occupies the address/data bus with the accidentally same addressed byte.

This drawback can be removed by the circuit in the diagram. A retriggerable monostable evaluates the low and

high edges of the ALE signal, which after a power-down and before a reset has a clock pulse. The output of the monostable sets a high on the CS input of
the EPROM when the powerdown mode is selected (and when, consequently, the disabled quartz oscillator can no longer generate an ALE
pulse).This arrangement ensures that the EPROM can also be switched to the power-down mode.

Moreover, the monostable
output may also be set on the address decoder of the system, or the combined $\overline{\mathrm{CS}}$ lines of other peripheral equipment, so that these are also in the powerdown mode.

Note that with component values as specified, the monostable has a time constant of about $4.5 \mu \mathrm{~s}$.
[984127]

Elektor Electronics, March 1998, ‘80C32-BASIC control computer'.

Elektor Electronics, September 1997, 'Data acquisition system'

Elektor Electronics, June 1997, 80C537 microcontroller board'

## general-purpose alarm



## Design: K. Syttkus

The alarm may be used for a variety of applications, such as frost monitor, room temperature monitor, and so on.

In the quiescent state, the circuit draws a current of only a few microamperes, so that, in theory at least, a 9 V dry battery (PP3, 6AM6, MN1604, 6LR61) should last for up to ten years. Such a tiny current is not possible when ICs are used, and the circuit is therefore a discrete design.

Every four seconds a measuring bridge, which actuates a Schmitt trigger, is switched on for 150 ms by a clock generator. In that period of 150 ms , the resistance of an NTC thermistor, $\mathrm{R}_{11}$, is compared with that of a fixed resistor. If the former is less than the latter, the alarm is set off.

When the circuit is switched on, capacitor $\mathrm{C}_{1}$ is not charged and transistors $\mathrm{T}_{1}-\mathrm{T}_{3}$ are off. After switch-on, $\mathrm{C}_{1}$ is charged gradually via $R_{1}, R_{7}$, and $R_{8}$, until the base voltage of $\mathrm{T}_{1}$ exceeds the threshold bias.

Transistor $\mathrm{T}_{1}$ then comes on and causes $\mathrm{T}_{2}$ and $\mathrm{T}_{3}$ to conduct also. Thereupon, $\mathrm{C}_{1}$ is charged via current source $\mathrm{T}_{1}-\mathrm{T}_{2}-\mathrm{D}_{1}$, until the current from the source becomes smaller than that flowing through $\mathrm{R}_{3}$ and $\mathrm{T}_{3}$ (about $3 \mu \mathrm{~A}$ ). This results in $\mathrm{T}_{1}$ switching off, so that, owing to the coupling with $\mathrm{C}_{1}$, the entire circuit is disabled.

Capacitor $\mathrm{C}_{1}$ is (almost) fully charged, so that the anode potential of $D_{1}$ drops well below 0 V . Only when $\mathrm{C}_{1}$ is charged again can a new cycle begin.

It is obvious that the larger part of the current is used for charging $\mathrm{C}_{1}$.

Gate $\mathrm{IC}_{1 a}$ functions as impedance inverter and feedback stage, and regularly switches on measurement bridge $\mathrm{R}_{9}-\mathrm{R}_{12}-\mathrm{C}_{2}-\mathrm{P}_{1}$ briefly. The bridge is terminated in a differential amplifier, which, in spite of the tiny current (and the consequent small transconductance of the transistors) provides a large amplification and, therefore, a high sensitivity.

Resistors $\mathrm{R}_{13}$ and $\mathrm{R}_{15}$ provide through a kind of hysteresis a Schmitt trigger input for the differential amplifier, which results in unambiguous and fast measurement results.

Capacitor $\mathrm{C}_{2}$ compensates for the capacitive effect of long cables between sensor and circuit and so prevents false alarms.

If the sensor $\left(\mathrm{R}_{11}\right)$ is built in the same enclosure as the remainder of the circuit (as, for instance, in a room temperature monitor), $\mathrm{C}_{2}$ and $\mathrm{R}_{13}$ may be omitted. In that case, $\mathrm{C}_{3}$ will absorb any interference signals and so prevent false alarms.

To prevent any residual charge in $\mathrm{C}_{3}$ causing a false alarm when the bridge is in equilibrium, the capacitor is discharged rapidly via $D_{2}$ when this happens.

Gates $\mathrm{IC}_{1 \mathrm{c}}$ and $\mathrm{IC}_{1 \mathrm{~d}}$ form an oscillator to drive the buzzer (an a.c. type).

Owing to the very high impedance of the clock, an epoxy resin (not pertinax) board must be used for building the
alarm. For the same reason, $\mathrm{C}_{1}$ should be a type with very low leakage current.

If operation of the alarm is required when the resistance of $\mathrm{R}_{11}$ is higher than that of the fixed resistor, reverse the connections of the elements of the bridge and thus effectively the inverting and non-inverting inputs of the differential amplifier.

An NTC thermistor such as $\mathrm{R}_{11}$ has a resistance at $-18{ }^{\circ} \mathrm{C}$ that is about ten times as high as that at room temperature. It is, therefore, advisable, if not a must, when precise operation is required, to consult the data sheet of the device or take a number of test readings.

For the present circuit, the resistance at $-18{ }^{\circ} \mathrm{C}$ must be $300-400 \mathrm{k} \Omega$. The value of $\mathrm{R}_{12}$ should be the same. Preset $\mathrm{P}_{1}$ provides fine adjustment of the response threshold.

Note that although the prototype uses an NTC thermistor, a different kind of sensor may also be used, provided its electrical specification is known and suits the present circuit. [984078]

