CIRCUIT DESCRIPTION

Technical Paper
STP 99-10

STACKED FLYBACK CONVERTERS WITH LOW POWER OUTPUTS FROM INPUT VOLTAGES OVER 500 VOLTS

by Paul Greenland and Bruce Carsten

FOREWORD

Low power (5 W to 50 W) converters are required for housekeeping or auxiliary applications in high power converters operating off of high-voltage AC mains (e.g., 480 VAC) or for low power instrumentation with similar power sources. Flyback converters have a simplicity and cost advantage at low power levels. Various multi-chip and monolithic devices are used for 120/240 Vrms inputs, but their typical maximum voltage rating of 700 V prevents their use at rectified line voltages much over 400 V.

A practical answer is to stack two or more flyback converters in series, using smaller MOSFETs with lower voltage ratings. All of the converters share a common transformer core and output, with a separate primary winding and power MOSFET for each. A single low-side controller and MOSFET driver is required, with capacitors to level shift the drive to the other MOSFETs. Several flyback voltage-clamping techniques will be introduced, each with its own advantages. Practical design drawbacks and their solutions will be discussed. A complete schematic for a practical converter using this approach will be supplied, with information specific to the design.

INTRODUCTION

Motor drives, UPS, and instrumentation require low power, low output voltage-isolated converters operating from high AC potentials. These converters are used as housekeeping supplies, or to provide floating supplies for high power switch drives. Single-ended topologies are preferable in terms of cost and simplicity. Forward converters are subject to transformer reset problems under these conditions. Flyback converters seem to offer the best compromise between component count and performance in the application. However, the voltage stress on the switch has to be taken into account. This can be mitigated by the use of two transistor converters that require a floating drive for the high-side switch. Alternatively, high-voltage deflection transistors such as the ubiquitous BU508 may be used in single-switch implementations. If a high-voltage MOSFET is used for the switch, the part cost, output capacitance, and field termination structure reliability are factors for consideration. Furthermore, once the power switch is selected, transformer design and construction have to account for parasitics which are more troublesome at high potentials. Partial discharge effects occur when high AC voltage potentials exist between adjacent turns and successive layers.

Studying secondary rectifier configurations in high-voltage power supplies is particularly useful when considering primary solutions for low power supplies operating from high potentials. Stacked secondary rectifier configurations and diode-split transformer construction have been used to reduce referred secondary capacitance, and allow the use of fast-recovery diodes for high-voltage outputs. When this technique is adopted on the primary side, the result is the stacked flyback converter (SFC).

Basic SFC Concepts

The simplest implementation of the the SFC is shown in Figure 1. C1 and C2 split the input voltage. Q1 is directly connected to the primary return referenced drive circuit. The high-side switch Q2 is driven through a capacitor and dc restoration circuit. The two primary windings are on a common core. A three-stage SFC with active-clamped reset, capacitively coupled to all stages, is

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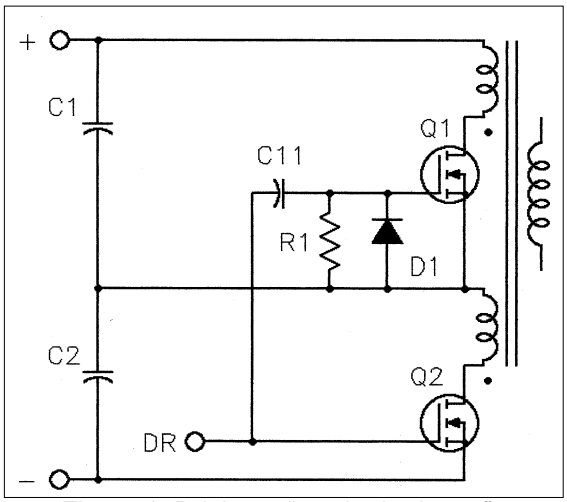

Figure 1: Driving a “stacked primary” FET with a capacitor and a dc restoration circuit

shown in Figure 2. In this case, the drive to the high-side MOSFETs is level shifted through a tertiary winding on the power transformer. As each drain is referenced to AC ground, capacitive coupling of noise into grounded or floating heat sinks is minimized.

The leakage inductance in the power transformer causes a spike in the drain voltage waveform at the instant of turn-OFF, as the energy stored in the core commutates to the secondary. Figure 3 illustrates two options for dealing with this phenomenon in the SFC.

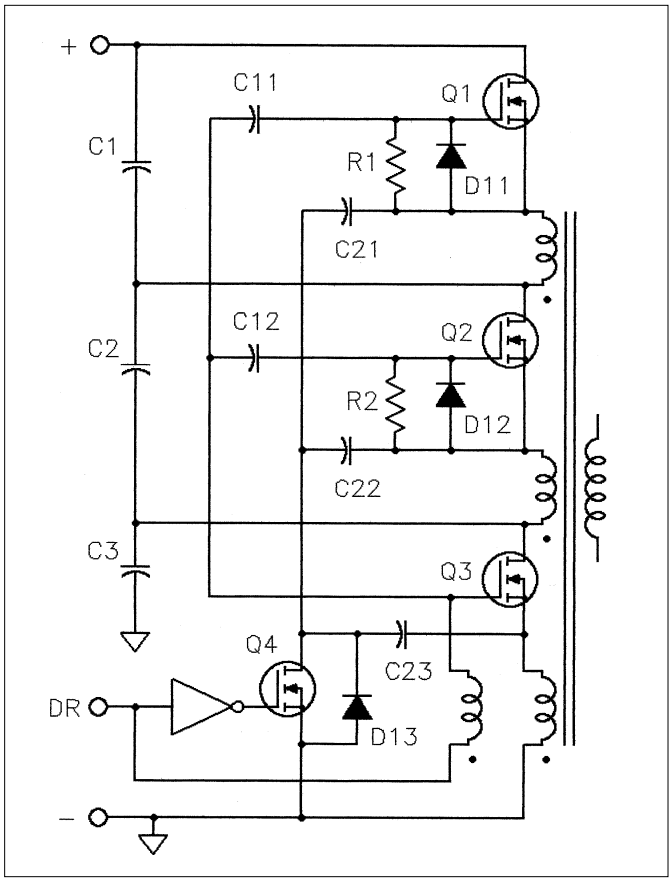

Figure 2: Level shifted drive to high-side FETs through a tertiary winding, and using active clamp reset

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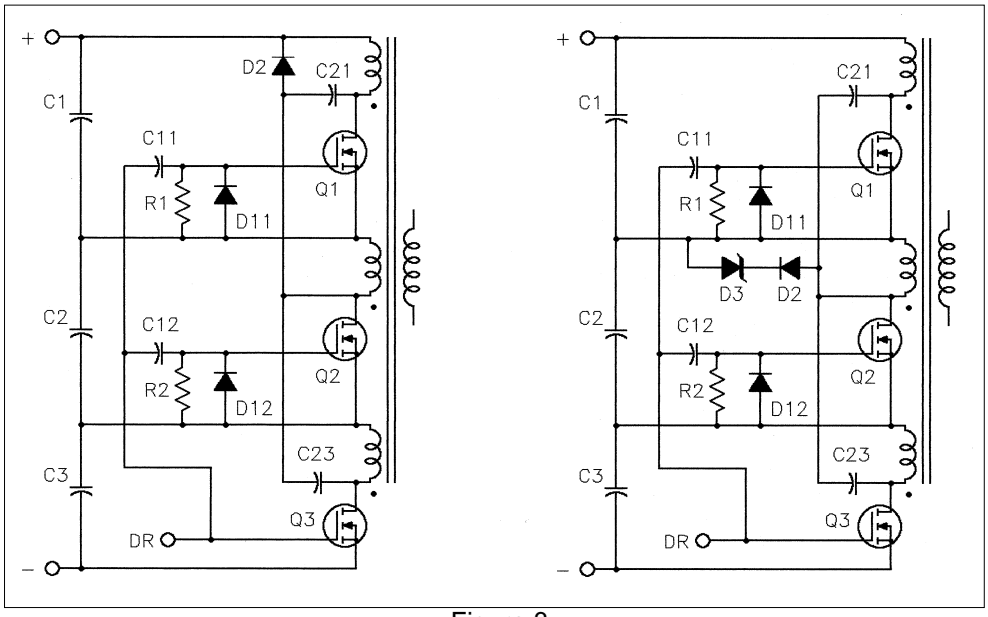

Figure 3

Leakage spike clamping with a diode to the next higher stage supply voltage

Leakage spike clamping with a dissipative Zener clamp

PRACTICAL SFC DESIGN CONSIDERATIONS

A schematic diagram for the high-voltage SFC built to explore this concept is shown in Figure 4. At first sight, this implementation appears complex. However, additional circuitry has been added, as this is a stand-alone prototype rather than an element of a larger system. A series string of bypass capacitors is required on the input to define the working voltage for each primary section, but these capacitors need not be very large if there is an external reservoir capacitor to supply most of the energy for each switching cycle. The three electrolytic capacitors C1 – C3 are not required if there is a similar or larger energy reservoir on the input.

The inrush-limiting thermistor R1 may be removed if the external source is inrush limited, or has an otherwise controlled voltage rise time of less than about 15 V/µs. Nonetheless, a fixed-input resistor of 10 ohms or so, or a small filter inductor, is still useful to reduce high-frequency input ripple currents. The input diodes D5 and D6 prevent destructive discharge currents in the stacked MOSFET drive circuits if the input is short-circuited, and their use is optional but advised.

Stacked FET Drive Capacitors

The drive capacitance to the stacked MOSFETs is constrained by two conflicting requirements. They must be large enough to supply the gate drive charge (Q_{GS}) without significant voltage droop, or the gate voltage swing available will be inadequate. On the other hand, excessively large gate drive capacitors will overburden the gate driver and/or the dc restoration/gate voltage clamping circuits. The drive capacitor voltage drop due to the gate charge (= Q_{GS}/C_{drive}) should be in the range of 500 mV – 2 V. The MTP1N60 MOSFET has about a 6 nC gate charge, for a voltage drop of 1.3 V with the 4.7 nF drive capacitors in this circuit.

Stacked FET Drive Clamping

The drive voltage to the MOSFETs uses a Zener, Schottky, and resistor to provide dc restoration and well defined gate voltage drive levels. With a V_{CC} of 12 V, the control and drive IC (U1) has only about a 9 V high current drive swing (less at lower temperatures), which is further reduced by the Q_{GS}/C_{drive} voltage droop. A 7.5 V Zener (D15, D17) is used to provide at least incipient voltage clamping at MOSFET turn-ON, which is more important than it might seem.

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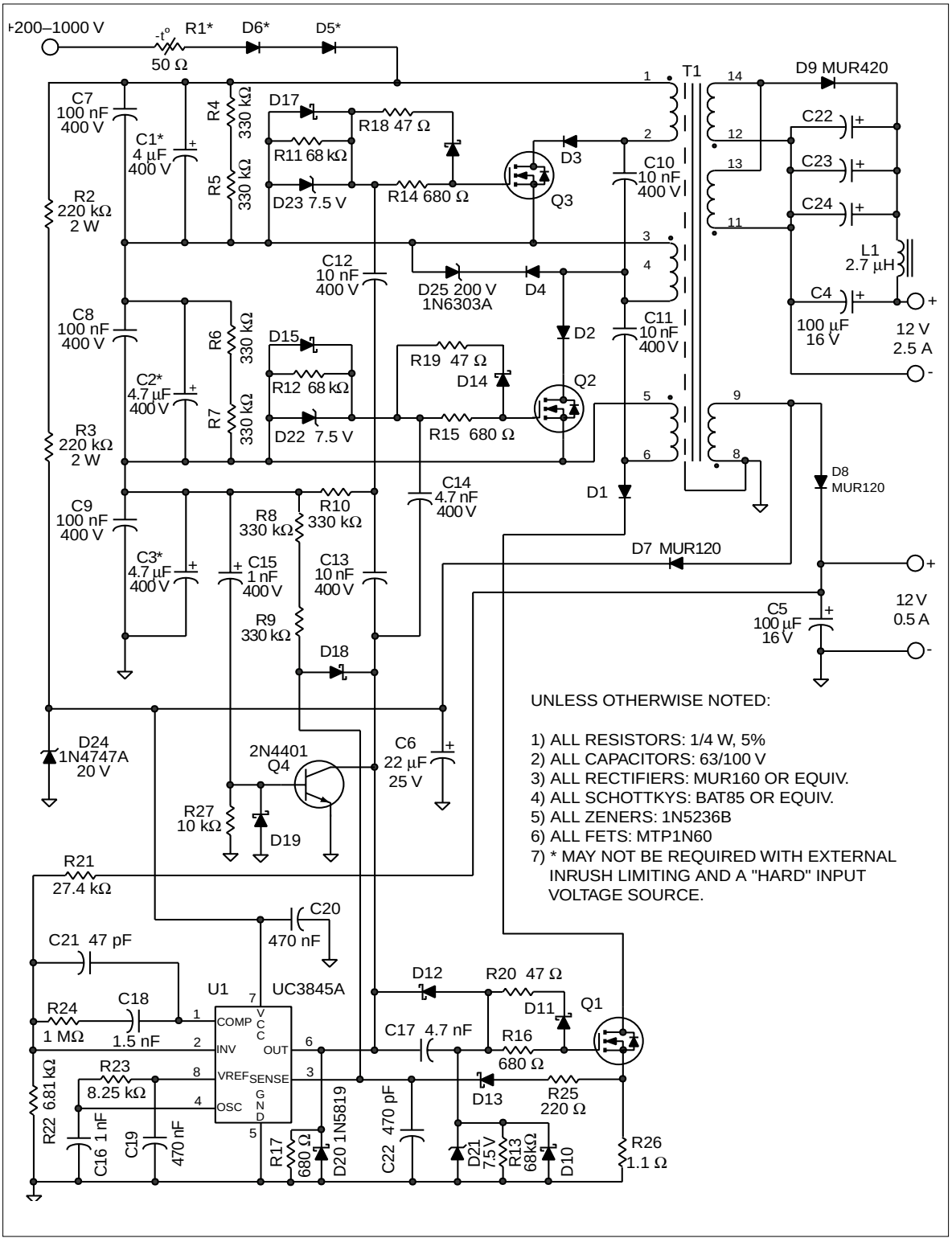

Figure 4: Schematic diagram – high input voltage stacked flyback dc-dc converter

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BILL OF MATERIALS

U1	UC3845A
L1	7 Turns #22 AWG on Micrometals: T26-26
T1	See Figure 5
Q1-Q3	MTP1N60 FET, 600 V, 12 W, TO-220
Q4	2N4401 NPN BJT, 40 V, 600 mA, hfe > 40 @ 500 mA
D1-D6	MUR160 PN EPI Rect., 600 V, 1 A, 75 ns t_{rr}
D7-D8	MUR120 PN EPI Rect., 200 V, 1 A, 35 ns t_{rr} or 11DQ10 Schottky, 100 V, 1 A
D9	MUR420PN EPI Rect., 200 V, 4 A, 35 ns t_{rr} or 50SQ100 Schottky, 100 V, 5 A
D10-D19	BAT85 Schottky, 30 V, 200 mA
D20	1N5819 Schottky, 40 V, 1 A
D21-23	1N5236B Zener, 7.5 V, 5%, 500 mW
D24	1N4747A Zener, 20 V, 5%, 1 W
D25	1N6303A TVS, 200 V, 5%, 1.5 kWpk or General Semiconductor 1.5KE200
C1-C3	4.7 μF, 400 V, 20% Electrolytic Capacitor, 105ºC, Mallory SEK4R7M400ST or Equivalent
C4-C5	100 μF, 16 V, 20% Electrolytic Capacitor, 105ºC, Sanyo 16SA100M, Rubycon ZA Series, or Nippon Chemi-Con 16FA100M
C6	22 μF, 25 V, 20% Electrolytic Capacitor, 105ºC, Mallory SEK220M025ST or Equivalent
C7-C9	100 nF, 400 V, 5% Plastic Capacitor
C10-C13	10 nF, 400 V, 5% Plastic Capacitor
C14	4.7 nF, 400 V, 5/10% Plastic Capacitor
C15	1 nF, 400 V, 5/10% Plastic Capacitor
C16	1.0 nF, 63/100 V, 5% Plastic Capacitor
C17	4.7 nF, 63/100 V, 5% Plastic Capacitor
C18	1.5 nF, 63/100 V, 5% Plastic Capacitor
C19-C20	470 nF, 63/100 V, 5/10% Plastic Capacitor
C21	47 pF, 50/63/100 V, 5% Ceramic Capacitor
C22	470 pF, 50/63/100 V, 5% Ceramic Capacitor
C23-24	100 μF, 16 V, 20% Electrolytic Capacitor, 105ºC, Sanyo 16SA100M, Rubycon ZA Series, or Nippon Chemi-Con 16FA100M
R1	50 Ω NTC Thermistor, Keystone CL150 or Equivalent
R2-R3	220 kΩ, 2 W, 5% Resistor
R4-R10	330 kΩ, 1/4 W, 5% Metal-Film Resistor
R11-R13	68 kΩ, 1/4 W, 5% Metal-Film Resistor
R14-R17	680 Ω, 1/4 W, 5% Metal-Film Resistor
R18-R20	47 Ω, 1/4 W, 5% Metal-Film Resistor
R21	27.4 kΩ, 1/4 W, 1% Metal-Film Resistor
R22	6.81 kΩ, 1/4 W, 1% Metal-Film Resistor
R23	8.25 kΩ, 1/4 W, 1% Metal-Film Resistor
R24	1.0 MΩ, 1/4 W, 5% Metal-Film Resistor
R25	220 Ω, 1/4 W, 5% Metal-Film Resistor
R26	1.1 Ω, 1/4 W, 5% Metal-Film Resistor
R27	10 kΩ, 1/4 W, 5% Metal-Film Resistor

The current the MOSFETs draw from the input when ON may cause a significant droop in the input voltage (perhaps volts to even tens of volts) with limited input energy storage. This input droop lowers the MOSFETs source voltage relative to the gate, and tries to turn the MOSFETs ON further. This regenerative drive tendency is not necessarily undesirable in itself (unless the gate is subject to over-voltage; it is certainly better than having the opposite effect), but in practice it cannot be allowed to occur. If the gate voltage were to rise by several volts, for example, there would not be enough gate drive voltage swing available to turn the MOSFETs back OFF. Thus a gate drive voltage clamp is used which is near or just below the available ON drive voltage before any drive regeneration occurs.

A similar problem can occur at MOSFET turn-OFF, where the recovering voltage on the input capacitors will raise the MOSFETs' source voltages and tend to drive V_{GS} negative. If the gate voltage were allowed to go a few volts negative relative to the source, there would not be enough gate drive voltage swing available to turn the MOSFETs fully ON again. Schottky diodes (D22, D23) limit the negative gate voltage to a few 100 mV. For the same reasons, no significant resistance is placed in series with the gate drive capacitors, which would inhibit the tracking of the drive capacitor voltage with changes in input voltage.

FET Reverse Conduction Blocking Diodes

Diodes D1 - D3 are placed in series with the power MOSFETs to block reverse conduction so that, if there is an imbalance in the input voltage division, the power is drawn from the section(s) with the highest voltage(s) until a balance is re-established. If the diodes are not used, there is an attempt to re-establish a balance immediately by delivering a high current from the highest to the lowest voltage section when the MOSFETs turn ON. It was found that a variety of abnormal but stable modes of operation could result without the blocking diodes, from simple minimal duty cycles due to over-current at turn-ON, to staggered turn-OFF with a two-step voltage rise. These abnormal modes were not fully explored when it was found that they could be avoided with the addition of the reverse conduction blocking diodes.

Current Sensing Considerations

Even with the reverse conduction blocking diodes, there is still a tendency for current to 'ring' from one primary circuit to another (presumably due to residual variations in FET switching times), which causes an oscillatory waveform on top of the bottom MOSFET (Q1) current-sensing voltage (on R26). This current sense ringing causes gain variations in the control loop, or even invalid duty cycles if the ringing is great enough. One solution would be to use a current transformer to sense the sum of the current in all of the MOSFETs. The alternative used here is to imitate the ideal current by charging a capacitor (C22 on the U1 current sense input) with a current proportional to the input voltage (from resistors R8 and R9). The C22 voltage is reset to near zero during the MOSFETs' OFF period through Schottky D18 connected to the U1 gate drive output. The actual Q1 current is 'ORed' to the current sense input through D13 (while R25 and C22 provide some immunity to leading-edge current spikes) for default control of maximum current.

Notes on Startup Dynamics

When input voltage is applied, the MOSFET gate drive capacitors C12 - C14 are charged through gate voltage clamp diodes D23 and D22 respectively, which fortunately holds MOSFETs Q3 and Q2 OFF as the Miller capacity (C_{DG}) tries to turn the MOSFETs ON with rising drain voltage. Unfortunately, this also tries to pull the drive output of U1 high before it has sufficient supply voltage V_{CC} to be operational, which can also result in an uncontrolled turn-ON of bottom MOSFET Q1. This is prevented by Q4, which is turned ON when the input voltage dV/dt is greater than about 0.15 - 0.20 V/µs; at lower input dV/dt the gate drive loading resistor R17 is sufficient to prevent turn-ON of Q1.

Capacitors C10 and C11 are used to improve voltage coupling between the several primary windings. Whereas the charging of the gate drive capacitors tends to imbalance the charging of the supply bypass capacitors towards more voltage on the top capacitors, charging of the winding coupling capacitors has the opposite effect. If oversized MOSFETs (with large gate charges) are used, the gate drive capacitors may become comparable in size to the bypass capacitors; in this case, it is desirable to

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make the primary winding coupling capacitors the same value as the gate drive capacitors to minimize supply voltage bypass capacitor imbalances during application of the input voltage.

Input Under-Voltage Lock-out

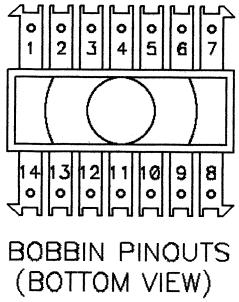
The input Under-Voltage Lock-Out (UVLO) function is crude but present. The control IC U1 will not start until the V_{CC} voltage reaches a nominal 16 V. With a typical start-up current drain of 0.3 mA, this requires about 132 V input, or 220 V at the maximum drain of 0.5 mA. The minimum input voltage to maintain regulation depends on load power, and is about 200 V at full load. At some low input voltage, the 12 V outputs will come out of regulation, and at nominal 10 V output, the controller UVLO will trip. A more sophisticated UVLO could be designed with micropower comparators and a voltage reference operating from the supply rail for U1.

An Over-Voltage Lock-Out (OVLO) may also be desirable to allow for more input-voltage headroom during high-energy input-voltage transients. The input-bypass capacitors' rating would limit the peak input to 1.2 kV, but capacitors can generally tolerate over-voltages for short durations. The most basic limitation is the MOSFET $V_{(BR)DS}$ rating, which increases the transient input capability to 1.8 kV or so.

Prototype Performance

The circuit shown in Figure 4 was constructed and tested to prove the SFC concept. This converter delivers 36 watts, with an input range of 200 to 1000 volts dc. Extra care was taken to preserve creepage and clearance distances, as high potentials are present. The power transformer in Figure 5 was wound on an ETD34 core in 3C85 material. A switching frequency of 100 kHz was chosen to keep the third harmonic below 450 kHz. A

Transformer Details
Core: Philips ETD34-3C85-G200
Total Primary Inductance Lp = 1.073 mH
Np1 = Np2 = Np3 = 15 Turns
Ns1 = Ns2 = 3 Turns



WINDING SEQUENCE:

SECT.:	START PIN:	FINISH PIN:	WIRE GAUGE, INS. & TURNS	
1	8	9	#24 W.W.W.	3 Turns
2	11	13	#26 3–INS	3 x 3 Turns
3	5	6	#26 W.W.W.	15 Turns
4	3	4	#26 W.W.W.	15 Turns
5	1	2	#26 W.W.W.	15 Turns
6	12	14	#26 3–INS	3 x 3 Turns
7	8	9	#24 W.W.W.	3 Turns

Figure 5:
Basic Transformer Construction

slotted coil former of the type popular in low-cost consumer applications was employed, at the expense of higher leakage inductance, which is evident by the drain voltage waveforms in Figure 6 that exhibit the characteristic high-frequency ringing at switch-OFF, in addition to the level shifting for the two high-side switches. The current in each drain is shown in Figure 7. The mismatch between the current ramps is due primarily to small differences in the gate drive signals, in spite of the identical drive circuitry for each device. In Figure 8, the anode voltage and current in the output rectifier are close to ideal without excessive overshoot caused by secondary leakage inductance ringing with the rectifiers' junction capacity.

CONCLUSION

The design of low power auxiliary converters in high power applications should be a simple task in comparison to the design of the system itself. However, in the case of systems running off of high-voltage sources, auxiliary converter design is not trivial. The stacked flyback converter described herein represents a timely solution to some of the problems of running from high-voltage. The practical example detailed in this paper represents the first step in establishing a minimum compromise solution. Further work on this topology and extensions of this technique to other converters will be the subject of future publications.

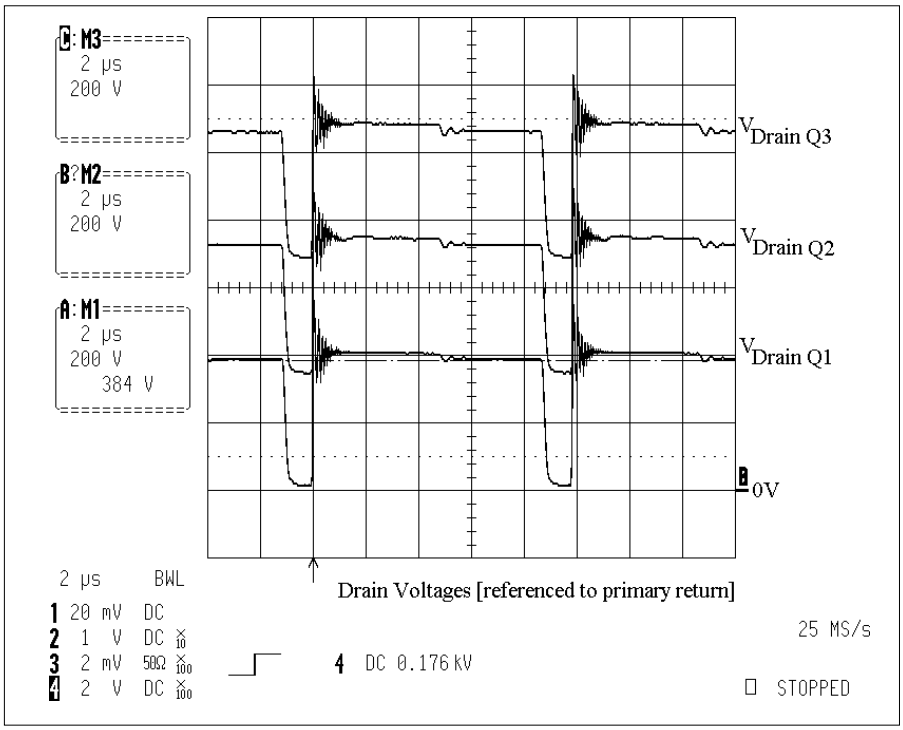


Figure 6

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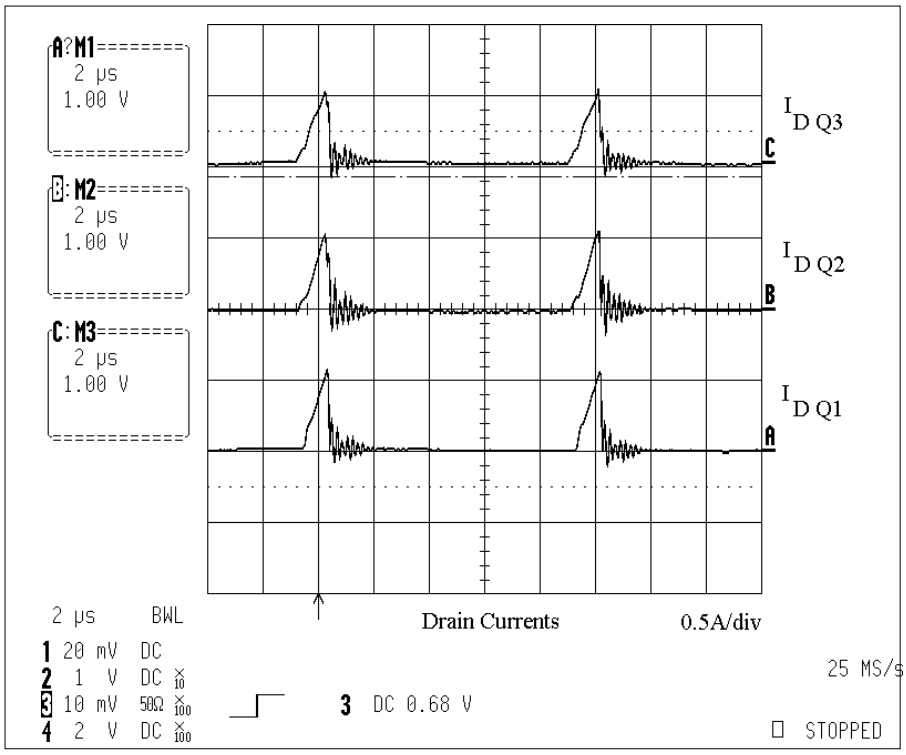

Figure 7

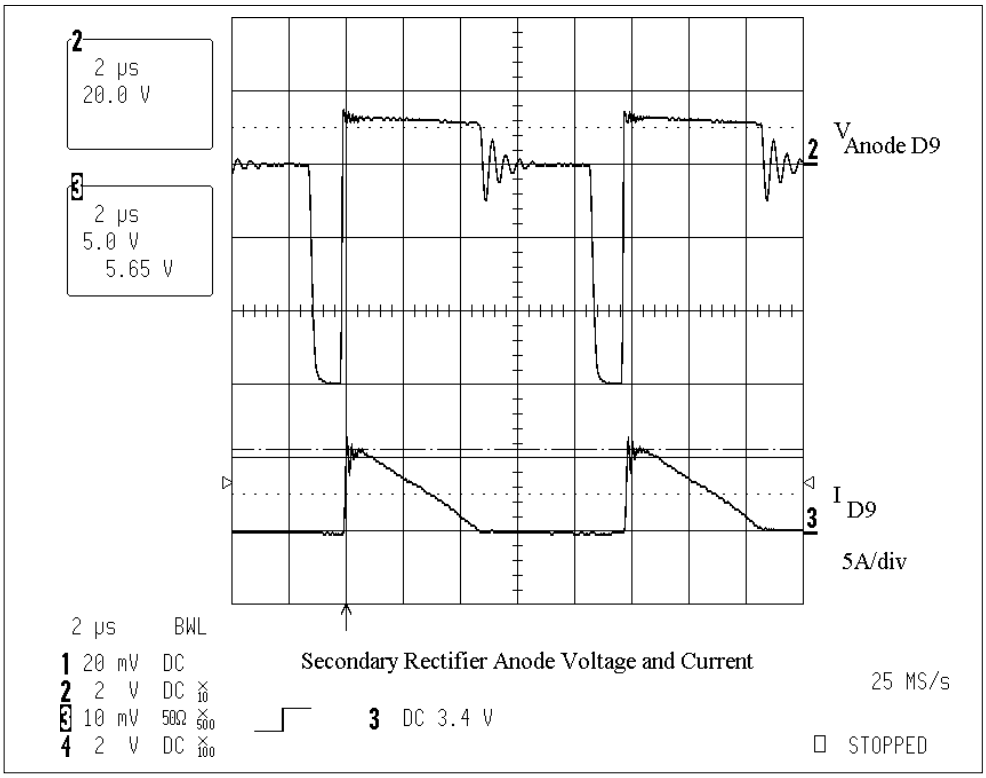

Figure 8

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The technology described here was constructed for proof of concept only. Modifications may be required for mass production.

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