High Temperature (>200°C) Isolated Gate Drive Topologies for Silicon Carbide (SiC) JFET

S. Waffler, S.D. Round and J.W. Kolar
Power Electronic Systems Laboratory
ETH Zurich
8092 Zurich, Switzerland
Email: waffler@lem.ee.ethz.ch

***Abstract*—Volume and weight limitations for components in hybrid electrical vehicle (HEV) propulsion systems demand highly-compact and highly-efficient power electronics. The application of Silicon Carbide (SiC) semiconductor technology in conjunction with high temperature (HT) operation allows the power density of the DC-DC converters and inverters to be increased. Elevated ambient temperatures of above 200°C also affects the gate drives attached to the power semiconductors. This paper focuses on the selection of HT components and discusses different gate drive topologies for SiC JFETs with respect to HT operation capability, limitations, dynamic performance and circuit complexity. An experimental performance comparison of edge-triggered and phase-difference HT drivers with a conventional room temperature JFET gate driver is given. The proposed edge-triggered gate driver offers high switching speeds and a cost effective implementation. Switching tests at 200°C approve an excellent performance at high temperature and a low temperature drift of the driver output voltage.**

I. Introduction

High temperatures in the propulsion system of Hybrid Electrical Vehicles (HEV) provide a harsh environment for power electronic systems such as DC-DC converters and inverters. The same environmental conditions also apply for military, space exploration or energy exploration applications [1] and demand High Temperature (HT) capable electronics. Silicon Carbide (SiC) semiconductors are especially valuable in these fields of application due to the SiC material properties.

In comparison to silicon, SiC has a larger band gap and thus allows higher junction temperature operation, which minimizes heat sink volume or provides the possibility to integrate the power electronics with the engine and the engine coolant of a HEV [2]. The higher saturated electron drift speed increases switching speed [1] and thus allows a reduction of the size and weight of the converter's passive components.

The only available SiC switch is the normally-on JFET that offers larger forward current ratings and lower on resistance [3], whereas normally-off devices like SiC-BJT, SiC-MOSFETs and IGBTs are being researched by semiconductor manufacturers for future application.

Since it is necessary to place the gate drive physically close to a SiC-JFET, operation at elevated ambient temperature of above 200°C is required and a switching frequency of approximately 250kHz is desired to benefit from the SiC dynamic properties. Furthermore, for a DC-DC converter application a large duty range is essential and the capability to statically turn off the normally-on device is required for protection reasons.

A typical JFET gate drive circuit for room temperature operation that provides these requirements is shown in Fig. 1. A digital isolator *IC1* is applied to electrically isolate the PWM signal from the high voltage and feeds a subsequent integrated driver circuit *IC2* that generates the JFET gate voltage u_{gs}. *IC1* and *IC2* are connected to a transformer-isolated auxiliary power supply. Circuit extensions can provide better switching performance [4] or protection functionality [5].

The optical or integrated magnetic couplers that are typically utilized for *IC1* as well as the integrated circuit *IC2* are not operable at high temperature because of aging effects and/or other material limitations like maximum junction temperature. Only a small number of components fulfills the requirements for operating temperature range.

Therefore, high temperature operation of gate drivers that also have high performance poses a significant challenge in both component and topology selection. Section II of this paper deals with materials and components for HT operation. Different drive topologies that utilize this component portfolio are evaluated in Section III. Comparative experimental results for the selected drive topologies are presented in Section IV.

II. Component Selection

A. Passive components

HT resistors are standard components with the maximum allowable power dissipation as the limiting factor. Since power dissipation decreases with temperature, resistors with higher power rating must be chosen. The influence of the temperature coefficient (TC) is considerably low for a gate drive application.

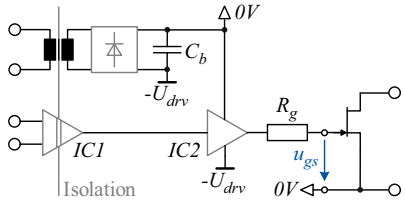

Fig. 1. Typical gate driver design using an isolated power supply, a digital isolator *IC1* and an integrated driving circuit *IC2*.

This is different for capacitors where the temperature characteristics of ceramic dielectrics like X7R or Y5U are very unstable [6] and induce a capacitance drop of 50% or more at the desired temperature. The selected HT SMT capacitors by Advanced Monolithic Capacitors (AMC) with temperature stable NPO dielectric are rated for 200°C.

Furthermore, suitable magnetic materials are required for the isolating transformers. The maximum operation temperature for coated powder, ferrite or strip-wound cores is in the range of 125 - 200°C [7] because of the epoxy coating. That is why uncoated toroidal ferrite cores with high Curie temperature T_c are preferred. The transformers used for the gate drivers are constructed from Magentics L material [8] cores, which have a $T_c > 300$°C and relatively good magnetic and core loss characteristics, and the windings are made with Polyamidimid coated grade 2 magnet wire. An alternative is to avoid magnetic materials by the application of coreless transformers.

B. Active components

Increasing substrate leakage currents limit the maximum allowable junction temperature for silicon integrated circuits. Alternatives for HT active components are SiC or Silicon On Insulator (SOI) technology that provide significant reliability and performance advantages.

There is a wide variety of SiC diodes, also for low power applications like a HT gate drive but on the contrary, no discrete small signal transistors or integrated circuits.

However, a very restricted assortment of SOI products is available. This includes operational amplifiers, gate logic and discrete components. A promising part for the HT gate driver is a 1A SOI MOSFET by Honeywell (HTNFET).

C. Mechanical

From a mechanical point of view, there are two major concerns. These are the HT substrate and the packaging of the active components.

Firstly, epoxy resins are characterized by their glass transition temperature T_g above which the material becomes soft. This is one of the reasons why ceramic substrates like Al_2O_3 or AlN are preferred to standard FR-4 ($T_g \approx 130$°C) or High-Tg FR-4 ($T_g \approx 170$°C). A further reliability-related material property is the coefficient of thermal expansion (CTE). The CTE of the base material should be similar to that of the conductor material otherwise unequal expansion of substrate and conductor will crack tracks or vias. The FR-4 materials show a large CTE in z-direction and can not be used.

However, there are special laminates like Arlon 85N, Isola IS410 or Rogers RO4530B that can be handled with a cost-saving standard PCB process and provide high T_g and low CTE at the same time such as $T_g > 280$°C and $CTE(z) = 35$ppm/°C for the selected RO4530B substrate.

Secondly, as conventional epoxy packages do not withstand the temperature, usually a Multi-Chip Power Module (MCPM) is the packaging technique of choice. As a matter of costs and handling, HT MOSFETs in a HT ceramic package and SiC components in standard packages are to be placed on RO4530B substrate in a first step.

III. Topology Evaluation

For a cost-optimized gate driver design the number of HT components, especially of non-standard active components like MOSFETs needs to be minimized. Purely passive drives, simple active drives and more advanced active drives are evaluated in respect to their suitability for application to SiC JFETs employed in DC-DC converters.

A. Transformer Coupled Gate Drive Circuits

A simple gate driver with an isolation transformer but without active components is depicted in Fig. 2 (a). Since the volt seconds product of positive and negative half-wave of the transformer secondary voltage u_{gs} are forced to be equal, the circuit output is bipolar.

The bipolar signal is the cause of two problems, firstly, at low duty cycles the amplitude of the negative half-wave drops and will turn on the JFET when u_{gs} exceeds the threshold voltage U_{th}. Secondly, the positive JFET gate voltage should be kept below the threshold of the gate junction to avoid its destruction when no further current limitation is provided.

An additional capacitor C_c and a diode D_c extends the circuit to the DC Restore Circuit (Fig. 2 (b)) with output voltage either 0V or $u_{p,pk-pk}$ for a turns ratio of 1:1.

A constant voltage at the transformer primary saturates the core. To prevent saturation, a PWM signal $u_p(t)$ must be applied. Unfortunately, this fact disqualifies both circuits since the normally-on JFET cannot be turned off permanently.

B. High-Frequency Carrier

To overcome the drawback of the above circuits and to provide the possibility of a permanent JFET turn-off, a high frequency (HF) carrier could be modulated with the PWM signal. In order to turn the JFET off, the HF carrier is applied to the primary of a isolating transformer T_1 and rectified at its secondary side to provide a negative gate bias at C_1 (Fig. 3).

Whereas C_1 is charged quickly after the HF carrier is applied, C_1 has to be discharged by R_1 to turn the JFET on,

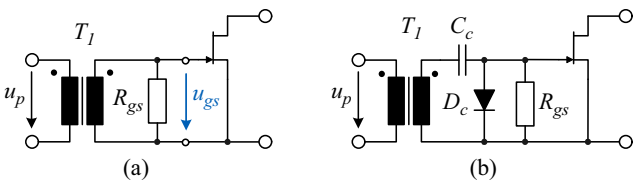

Fig. 2. Transformer Coupled circuits: (a) Simple, (b) DC Restore Circuit

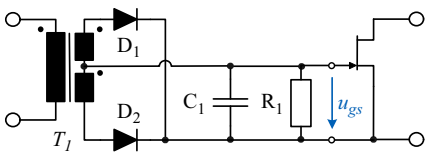

Fig. 3. High-Frequency Carrier Circuit

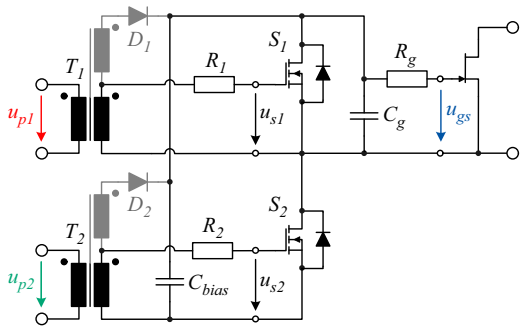

Fig. 4. Phase-Difference Circuit

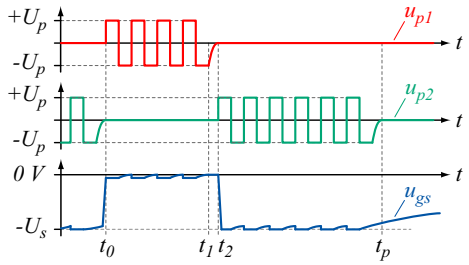

Fig. 5. Timing diagram for Phase Difference Circuit: Either switch S_1 or S_2 are switched to connect C_{bias} or 0V to the output respectively.

which significantly decreases the switching speed. Therefore, additional circuitry is required to actively discharge C_1.

A HF carrier gate driver with a resonantly operated coreless transformer (CT) is proposed in [9]. It has been determined by using simulation and measurements that the additional time to build up a steady oscillation at the CT secondary is too long to achieve short rise and fall times of u_{gs} and therefore high switching frequency operation.

Furthermore, it should be noted that the rectification of a very high frequency carrier signal with HT SiC diodes is poor since the available power diodes have large junction capacitances.

C. Phase-Difference Circuit

In order to provide continuous negative gate bias for the JFET, to overcome the duty-cycle limitations that are unavoidable with passive driving circuits and to achieve high switching speeds at the same time, actively controllable switches like MOSFETs are required in the gate driver.

A basic principle that also applies to integrated gate drivers is to use an storage capacitor C_{bias} in connection to a half-bride structure S_1, S_2 connected to the JFET gate (Fig. 4). By applying appropriate control signals to the gates of the two half-bridge switches either zero volts or the bias capacitor voltage U_{bias} is switched to the JFET gate.

When isolation of the control signals u_{gs1} and u_{gs2} is provided by transformers T_1 and T_2 the problem of the duty cycle limitation existing with passive drivers is shifted to the auxiliary switches S_1 and S_2. For an assumed 50% duty cycle that means if u_{p1} is switching and $u_{p2} = 0$ the half bridge output is changing between U_{bias} (S_1 on) and high impedance (S_2 off) and in case that $u_{p1} = 0$ and u_{p2} is switching the half-bridge output is changing between 0V and high impedance. The actual JFET gate voltage u_{gs} is preserved during the high impedance state due to the JFET input capacitance and an optional external capacitor C_g as indicated in Fig. 5. By continuous pulsing of S_2 the circuit is able to generate a static negative gate voltage at the JFET and thus turn the JFET off permanently. Due to the method of operation the drive concept is known as a Phase-Difference Drive [10].

The bias capacitor C_{bias} itself is charged by rectification of the carrier signals u_{p1} or u_{p2} with the diodes D_1 or D_2.

In conclusion, the circuit provides unlimited off-time, has no duty cycle limitation and fast switching transients of the JFET because of the active components S_1 and S_2.

D. Bootstrap Power Supply

To drive a JFET bridge leg, a novel Bootstrap Power Supply concept is proposed for the Phase Difference Driver to simplify the bias voltage generation. Taking the negative output voltage into account, the bootstrap diodes D_{bst} for the high-side JFET driver needs to be connected to a voltage source U_P referenced to the positive DC supply rail and charge the bootstrap capacitors C_{bst}. The capacitors C_{bias} of the low-side JFET drives are connected to a voltage source U_N referenced to the negative DC supply rail.

E. Edge-Triggered Circuit

A driving circuit of less complexity that provides the same functionality as the Phase-Difference Circuit is the proposed Edge-Triggered Drive Circuit depicted in Fig. 7. The circuit basically consists of a single pulse transformer T_1, an auxiliary MOSFET switch S_1, the diode D_2 and the capacitor C_g and

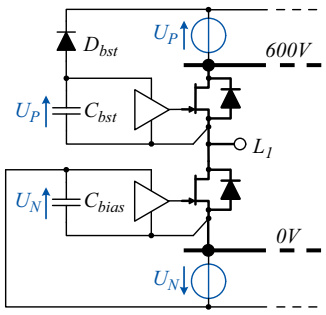

Fig. 6. Bootstrap Power Supply for the Phase Difference Driver

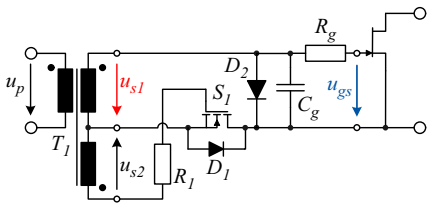

Fig. 7. Edge-Triggered Circuit

thus only needs half the components compared to the Phase-Difference drive without loss of performance as will be shown in Section IV.

The number of turns on the secondary winding 1 is selected to achieve a peak output voltage U_{s1} of at least the JFET threshold voltage U_{th} and the number of turns on the secondary winding 2 to provide an appropriate gate voltage to S_1.

To turn the JFET off, a short negative voltage pulse of width T_{PW} is applied to the transformer primary. In this case S_1 is turned off because of the negative gate voltage u_{s2}. The secondary voltage u_{s1} causes D_2 to block, D_1 conducts and C_g is charged to $-U_{s1} < U_{th}$ (Fig. 8 (b)). At the end of the pulse ($u_p = u_{s1} = u_{s2} = 0$V) S_1 turns off, isolates the JFET from the pulse transformer and thus prevents C_g discharging through the transformer secondary winding (Fig. 8 (c)). Continuous negative pulses can be used to permanently turn off the JFET like depicted in Fig. 9 for $t_a < t < t_0$.

To turn the JFET on, a positive pulse of width T_{PW} is applied to the transformer primary. Since $u_{s2} > 0$, S_1 is turned on and C_g is discharged. The positive voltage is clamped by D_2 so that the circuit output voltage is u_{gs} = 0V (Fig. 8 (a)).

For high-speed operation care must be taken with the selection of the components. The capacitance of C_g is a critical parameter because large values increase the rise and fall time of the drive output voltage. On the other hand, the output capacitance C_{oss1} of S_1 must be taken into account: Once the voltage u_{p1} returns to zero after a negative pulse that previously turned off the JFET, charge is drawn from C_g in order to charge C_{oss1} (Fig. 8 (c)). Therefore, low C_g values would cause an unintentional drop of the drive output voltage.

The short pulse width T_{PW} is a further advantage that results in a low volt seconds product for the transformer and thus a minimal transformer core size. This is important for minimal transformer parasitics like leakage inductance L_σ and primary to secondary coupling capacitance C_c. Small L_σ leads to high switching speeds and a small C_c ensures low common-mode currents resulting from the high dv/dt levels of the JFET Drain-Source voltage u_{ds}.

Furthermore, it should be noted that in practice a voltage overshoot U_{ov} (Fig. 15) at turn-off of the JFET is observed due to the resonant circuit formed by the secondary-side leakage inductance L_σ of the transformer T_1 and the storage capacitor C_g. This behavior also has a positive effect on the switching speed as will be shown later on.

IV. Experimental Results

As purely passive drivers or DC restore circuits cannot turn off the JFET permanently and the HF carrier circuits lack switching performance, the Phase-Difference and Edge-Triggered drivers are considered as candidate topologies in spite of the higher component effort.

For further investigation different versions of these two circuits and a standard low temperature gate driver (Fig. 1) were built and tested by switching an inductive load L with a SiCED SiC JFET (1300V, 4A, U_{th} = -25V) and a Cree CSD10060 SiC Schottky diode (1200V, 10A) that are connected to a DC link capacitor C_{DC} (Fig. 10).

A. Topology Comparison

For a first performance comparison, the different drivers were built with standard components and operated at room temperature. To ensure identical measurement conditions, each gate drive topology is routed on a separate interchangeable PCB. Furthermore, the transformers T_1 and T_2 of the Phase-Difference Circuit and T_1 of the Edge-Triggered Circuit share the same core and winding geometry. Gate resistors of R_g = 10Ω, Cree SiC diodes CSD04060 in a TO-252-2 package and Zetex ZVN4206G MOSFETs with gate resistors of R_1 = R_2 = 47Ω are used in each topology. The PWM and different drive control signals are generated by a DSP and a FPGA.

IC1 and *IC2* of the Standard Drive are an Analog Devices ADuM1100BR magnetic coupler and an IXYS IXDN404SI MOSFET driver respectively. A capacitor C_g = 2.2nF is utilized in the Edge-Triggered Circuit as a compromise between switching speed, gate drive losses and the voltage drop in u_{gs} that is encountered when C_{oss1} is charged. A pulse width T_{PW} of 130ns was found to be the minimum value to transfer the necessary gate charge. The carrier frequency for the Phase Difference Drive is set to 1MHz with a dead time of 250ns when switching between the two carrier signals u_{p1} and u_{p2} to prevent a short circuit of the half-bridge S_1, S_2 and oscillations in the drive output u_{gs}. The transformers of Phase Difference and Edge-Triggered Circuit are interfaced to the PWM FPGA by IXYS IXDN404SI driver ICs.

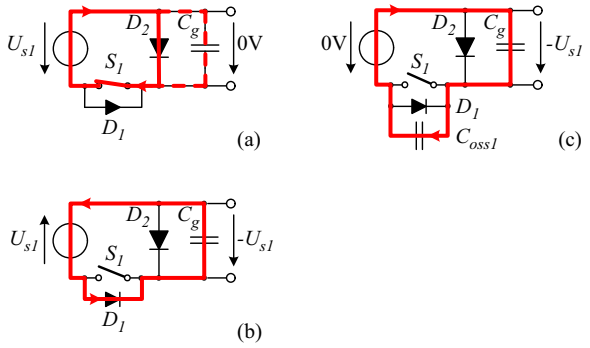

Fig. 8. Modes of Operation of edge-triggered drive circuit: (a) positive voltage pulse applied to the transformer primary, (b) negative voltage pulse applied, (c) no voltage applied to the transformer primary.

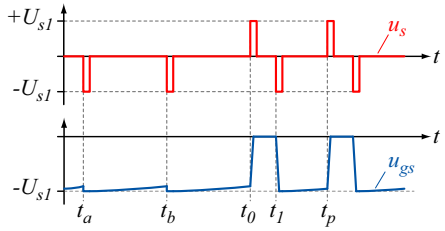

Fig. 9. Timing diagram for Edge-Triggered Circuit: Short pulses are applied to charge or discharge the output capacitor C_g.

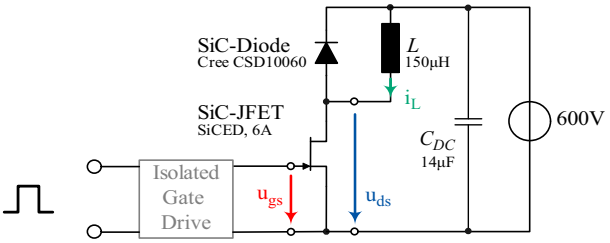

Fig. 10. Test setup with gate drive and power stage consisting of a SiC JFET, a SiC diode, DC-link capacitor C_{DC} and inductor L.

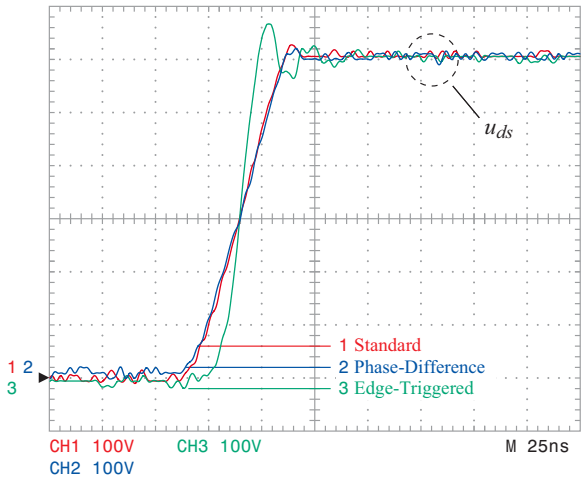

Fig. 11. Comparison of the JFET Drain-Source voltage u_{ds} rise times (JFET turn-off) for different driver topologies at room temperature.

The inductive load L is constructed using three E30 cores, each with a single layer winding to minimize the parasitic capacitance and C_{DC} consists of four 3.3µF film capacitors in parallel with two 220nF HV ceramic capacitors.

For each driver a switching cycle with i_L = 5A at turn-on of the JFET to i_L = 6A at turn-off (Fig. 14) was initiated at a DC link voltage of 600V. The fall time t_f and rise time t_r (Fig. 11) measurements of the drain source voltage u_{ds} show no drop in switching performance for the two HT topologies. On the contrary, the resonant voltage overshoot U_{ov} (Fig. 15) of u_{gs} for the Edge-Triggered Driver improves the voltage slopes.

The resulting rise and fall times are listed in Table I. With the Edge-Triggered Driver, which performed best in the comparison, maximum dv/dt levels of -60.0kV/µs at turn-on and 38.1kV/µs at turn-off are achieved. Therefore, high JFET switching frequencies of 250kHz and above are feasible.

TABLE I
SiC JFET Switching Times at Room Temperature

Topology	Turn on		Turn off	
	t_f (ns)	Slope (kV/µs)	t_r (ns)	Slope (kV/µs)
Standard	17.7	-34.4	35.4	17.2
Phase-Difference	18.4	-32.0	34.9	17.2
Edge-Triggered	10.2	-60.0	16.3	38.1

B. dv/dt Immunity

High dv/dt levels of the JFET Drain-Source voltage result in a common mode current through the parasitic coupling capacitance C_c of the electrical isolators of a gate drive. A robust gate drive should provide a good immunity to this current and therefore a low C_c. The transformers for the presented drives (15:15:7 turns on a R9.5 toroid) have a C_c of 12pF. The common mode rejection of the Edge-Triggered drive is verified with a switched voltage (600V, dv/dt = -60kV/µs) that is applied between the shorted primary winding of T_1 and the source connector at the output of the drive.

A disturbance of no more than 50mV is measured at the drive output voltage during the switching instants during non-switching of the driver (S_1 is blocking, C_c connected in series with C_{oss1}). Further measurements during the time a control pulse is applied to the transformer primary (S_1 is conducting) will be conducted.

C. High Temperature Operation

Due to the promising performance of the Edge-Triggered Driver at room temperature the circuit was built with HT components, including the transformer T_1 (Magnetics L material, HT wire), S_1 (Honeywell HTNFET), D_1 (SiC diode Cree CSD04060, standard package), C_g (AMC NPO capacitors) and HT resistors (Fig. 12). The components are assembled on RO4530B substrate with HMP solder. The resistors R_p, R_{s1} and a suppressor diode were added for protection of the HTNFET, but are not required for nominal operation.

The driver PCB is plugged onto a test circuit according to Fig. 10 that was built with X7R HV ceramic capacitors C_{DC} and a inductive load L made of an air-gapped Metglas AMCC 25 core and silicon wire and is operated inside a heating oven as shown in Fig. 13. An FPGA outside the oven and IXYS diver ICs that are enclosed inside a box and cooled with air from outside the oven generate the control pulses.

The operation of the driver was verified with switching cycles as shown in Fig. 14 for a temperature of 200°C. At 200°C and a load current of i_L = 6A the measured u_{ds} rise and fall times were t_r = 10.7ns and t_f = 14.3ns according to dv/dt levels of -57.1kV/µs and 41.7kV/µs.

As shown in Fig. 15, no significant change in the switching characteristics is observed when the temperature is raised to 200°C. However, due to the temperature dependence of the semiconductor parameters, a minor drop of the gate driver

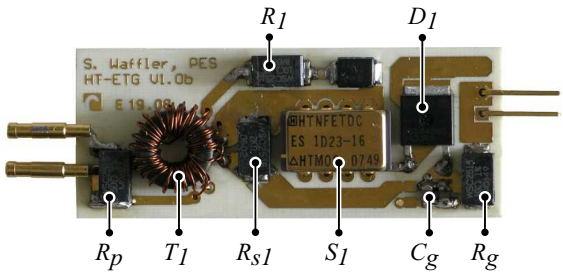

Fig. 12. Prototype PCB of the 200°C Edge-Triggered Driver

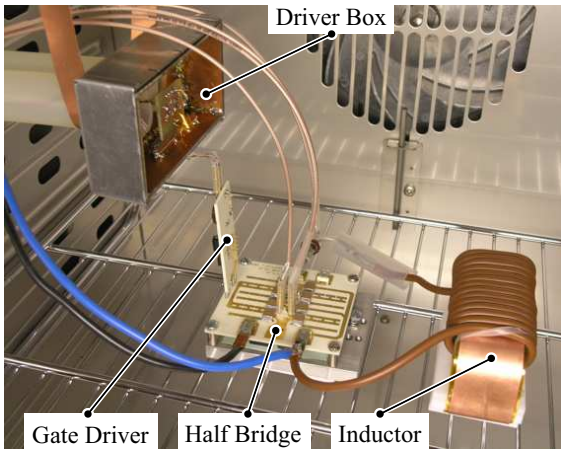

Fig. 13. Test setup inside the heating oven for inductive load switching tests

output voltage from -25.1V at room temperature to -23.8V at 200°C is observed, equivalent to a low temperature drift of 7.4mV/K for the driver circuit.

V. Conclusion

In this paper different SiC JFET gate drive topologies for use in a SiC DC/DC converter and High Temperature (HT) operation are evaluated. The candidate drive circuits are selected considering the aspects of HT component availability and costs, gate drive performance and additional requirements like the ability to permanently turn off a normally-on JFET. Furthermore, the passive and active HT components as well as the magnetic and substrate materials for the construction of these drives are investigated.

A Phase Difference Driver and the proposed Edge-Triggered Driver are compared experimentally with a conventional room temperature driver in regard to performance whereas the Edge-Triggered Driver shows excellent switching speeds and a cost-effective design due to a minimal HT component count.

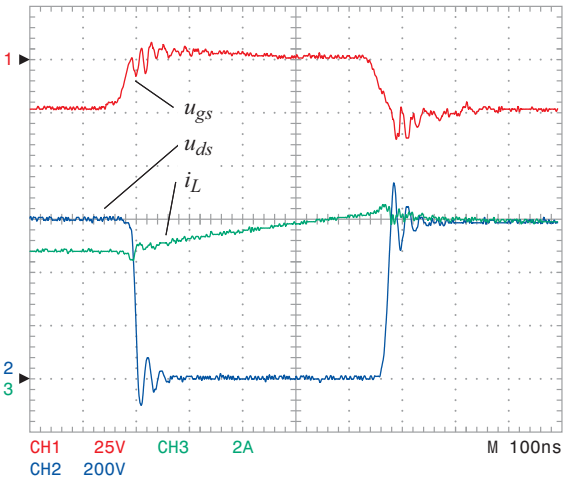

Fig. 14. Switching cycle for the High-Temperature Edge-Triggered Driver at 200°C and U_DC =600V, 5A< i_L < 6A

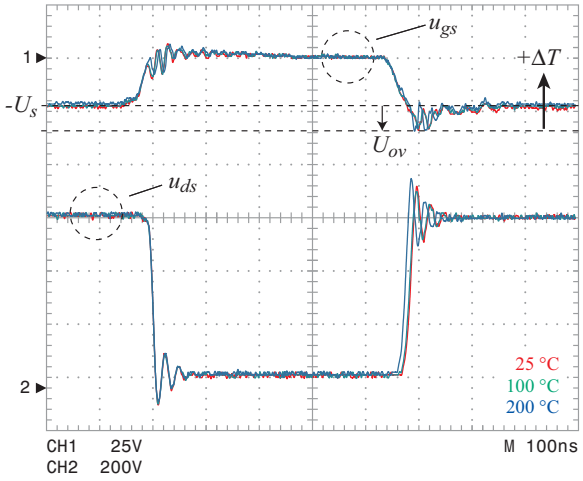

Fig. 15. Temperature dependence of Edge-Triggered circuit output voltage u_{gs} (resonant voltage overshoot U_{ov}) and the JFET drain source voltage u_{ds}.

The HT operation of the proposed Edge-Triggered Driver is verified by switching tests at a maximum temperature of 200°C without a drop in the switching performance. The maximum measured dv/dt levels of the JFET Drain-Source voltage of -57.1kV/µs and +41.7kV/µs demonstrate a very high performance of the HT Edge-Triggered Driver and the usability for high switching frequencies above 250kHz. Furthermore, the driver output voltage shows a low temperature drift of only 7.4mV/K.

References

[1] J. Hornberger, A.B. Lostetter, K.J. Olejniczak, T. McNutt, S.M. Lal, and A. Mantooth, "Silicon-Carbide (SiC) Semiconductor Power Electronics for Extreme High-Temperature Environments," in *IEEE Aerospace Conference*, vol. 4, Mar. 2004, pp. 2538–2555.

[2] F. Renken, G. Ehbauer, V. Karrer, R. Knorr, S. Ramminger, N. Seliger, and E. Wolfgang, "Reliability of High Temperature Inverters for HEV," in *Power Conversion Conference 2007*, Apr. 2007, pp. 563–568.

[3] R. Kelley and M.S. Mazzola, "SiC JFET Gate Driver Design for Use in DC/DC Converters," in *Applied Power Electronics Conference (APEC 2006)*, Mar. 2006, pp. 179–182.

[4] S. Round, M. Heldwein, J.W. Kolar, I. Hofsajer, and P. Friedrichs, "A SiC JFET Driver for a 5 kW, 150 kHz Three-Phase PWM Converter," in *Industry Applications Society Annual Meeting 2005*, vol. 1, Oct. 2004, pp. 410–416.

[5] A. Orellana and B. Piebenbreier, "Fast Gate Drive for SiC-JFET using a Conventional Driver for MOSFET and Additional Protections," in *30th annual Conference of IEEE (IECON)*, vol. 1, Nov. 2004, pp. 938–943.

[6] E. Cilio, J. Garrett, J. Fraley, B. McPherson, J. Hornberger, M. Schupbach, and A. Lostetter, "High Temperature Electronics (>485°C) For Venus Exploration," in *4th International Planetary Probe Workshop*, Pasadena, California, Jun. 2006.

[7] M. Swihart, "Designing High Temperature Magnetics," in *47th European Power Electronics Conference (PCIM)*, May 2003, pp. 223–228.

[8] R. Spyker, J. Huth, I. Mehdi, and A. Brockschmidt, "300C ferrite material for high temperature magnetics," in *Power Electronics Specialists Conference (PESC)*, Jun. 2004, pp. 155–160.

[9] S.Y. Hui, S.C. Tang, and H. Chung, "Optimal Operation of Coreless PCB Transformer-Isolated Gate Drive Circuits with Wide Switching Frequency Range," *IEEE Trans. Power Electron.*, vol. 14, no. 3, pp. 506–514, May 1999.

[10] D. C. Hopkins, D. W. Kellerman, R. A. Wunderlich, C. Basaran, and J. Gomez, "High-temperature, high-density packaging of a 60kW converter for >200°C embedded operation," in *Applied Power Electronics Conference (APEC)*, Mar. 2006, pp. 871–877.