Guidelines for Preventing Boot-to-Phase Stress on Half-Bridge MOSFET Driver ICs

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Introduction

In some cases, the combination of MOSFET selection, printed circuit board (PCB) layout, and VCC offset can cause damaging voltage levels between the BOOT and PHASE pins of half-bridge driver ICs for switching circuit applications. This technical brief provides detailed descriptions of each of these contributing factors and presents design techniques to prevent damage to the driver.

Description

Intersil half-bridge drivers contain a protective ESD device between the BOOT and PHASE pins (Figure 1) that will break down if the differential voltage across these pins is too high. The absolute maximum voltage rating between these two pins is typically around +7VDC (refer to part specific data sheets for accurate values).

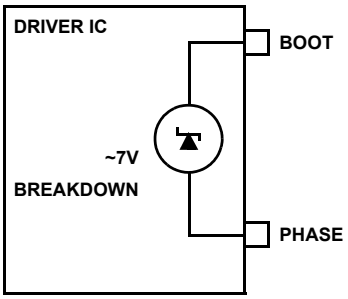

FIGURE 1. BASIC REPRESENTATION OF ESD DEVICE

Figure 2 and Figure 3 show the equivalent half-switching cycle circuits for a synchronous “buck” regulator application. The Boot capacitor is charged from VCC (through an internal Schottky diode to BOOT) to ground (through PHASE) during the second half of the switching cycle. BOOT-to-PHASE voltage is necessary to allow the “floating” hi-side driver to function properly.

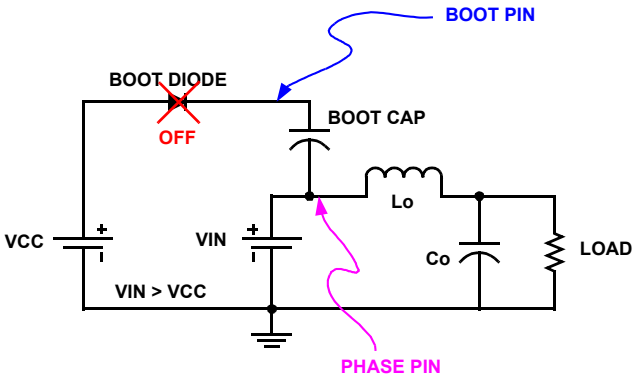

FIGURE 2. BUCK REGULATOR 1ST HALF-CYCLE EQUIVALENT CIRCUIT

During the first half-cycle of switching, the PHASE node is pulled above VCC through the high-side switch (not shown) causing the internal Schottky BOOT Diode to turn off, thus preventing BOOT Capacitance charging.

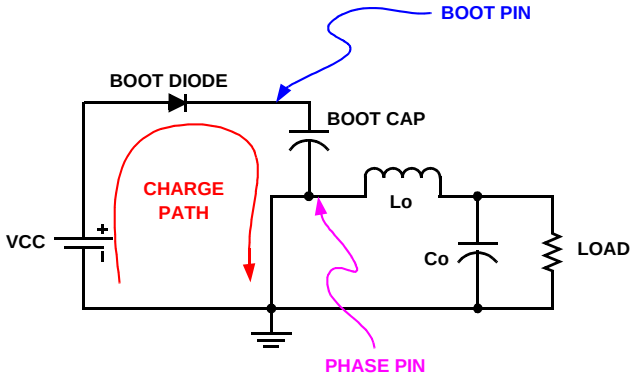

FIGURE 3. BUCK REGULATOR 2ND HALF-CYCLE EQUIVALENT CIRCUIT

Examination of Figure 3 shows that during the second half-cycle of switching, the PHASE node is pulled to ground through the synchronous switch (not shown). This forward biases the BOOT Diode and charges the BOOT Capacitor. By inspection, the BOOT-to-PHASE voltage under normal/steady-state operating conditions will equal VCC minus a Schottky Diode drop (typically 0.5V) or 4.5VDC.

However, the equivalent circuit in Figure 3 is ideal and therefore neglects critical circuit elements that must be taken into consideration when determining the voltage on the BOOT cap. These critical elements include the synchronous switch $r_{DS(ON)}$ during conduction, the forward drop of the synchronous switch body diode, and the parasitic impedances found in the PCB layout and MOSFET package.

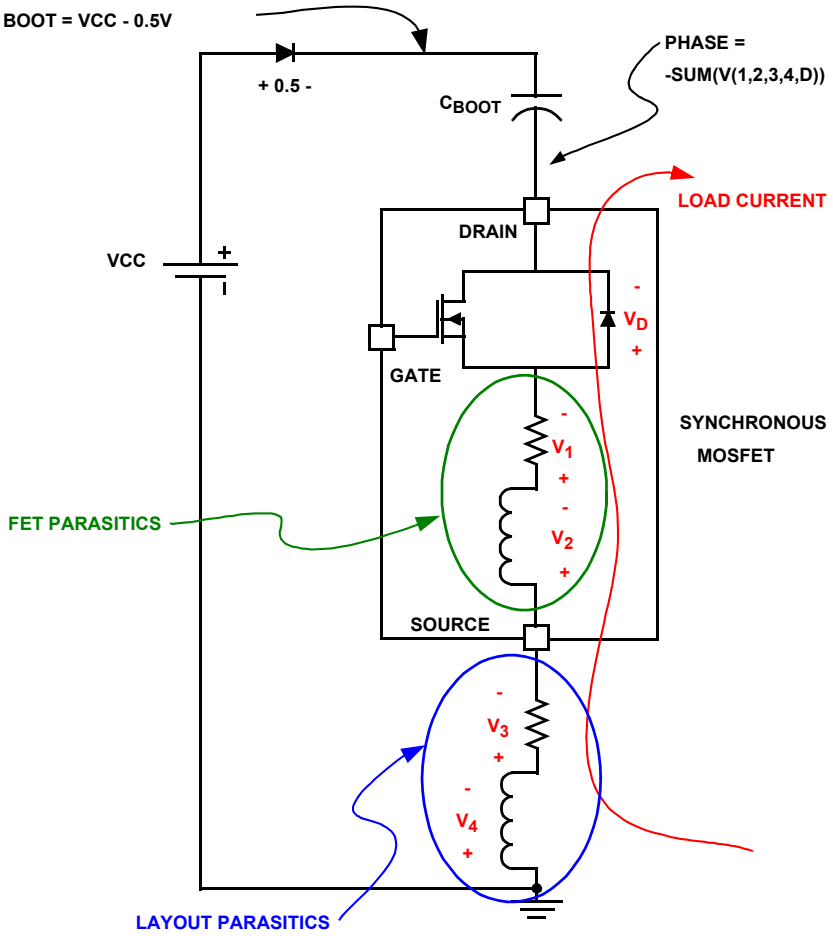

FIGURE 4. BOOT CAPACITANCE CHARGE PATH WITH REAL CIRCUIT ELEMENTS

Figure 4 illustrates a more in-depth circuit schematic for the charge path of the BOOT Capacitor. The parasitic elements serve to lower the PHASE voltage below ground, subsequently increasing the BOOT-to-PHASE voltage. Equation 1 expresses the mathematical equivalent to the circuit in Figure 4.

$$V_{CBOOT} = (VCC - 0.5V) - \Sigma(V(1, 2, 3, 4, D)) \quad \text{(EQ. 1)}$$

Design Recommendations

To avoid stressing the BOOT-to-PHASE ESD device, several design recommendations are listed below and should be reviewed for each new development.

- Lay out the synchronous MOSFET source to minimize impedance between the pin and ground
- Ensure that VCC is tightly regulated within ±10%
- Use MOSFETs with good body diode forward conduction characteristics (low forward voltage drop)
- Design for minimal acceptable dead-time
- Use an external Schottky Diode from PHASE to ground to minimize PHASE drop