PLD, CPLD and FPGA basics

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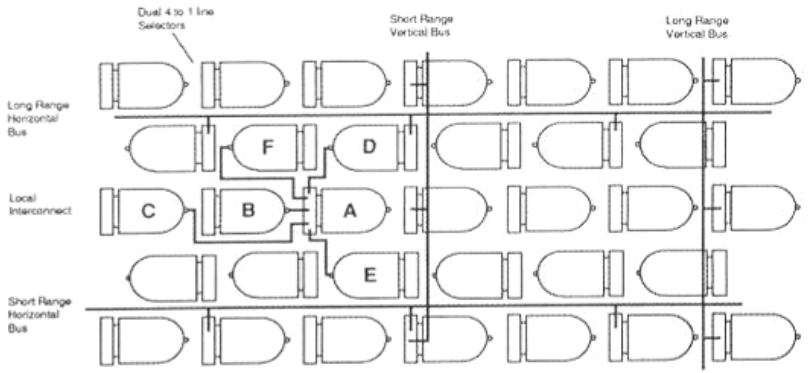
What is programmable logic device (PLD) ?

- A device which comes with some generic (or) configurable hardware whose functionality can be changed as per the application
  - Different than microprocessors and DSPs
  - Useful when hardware solution is required but ASIC is not feasible
  - PALs, CPLDs and FPGAs are popular

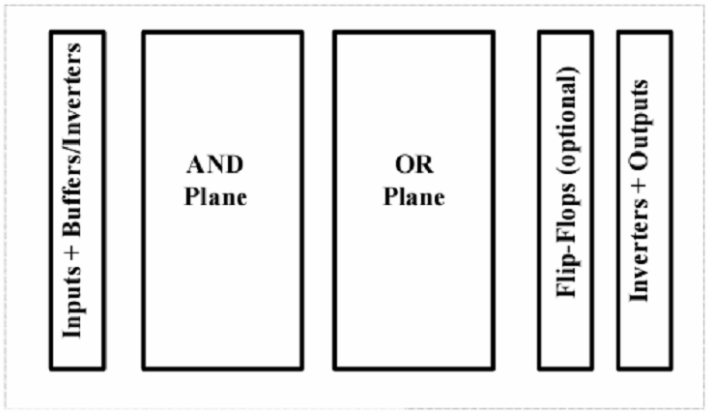
Programmable Logic Devices

- Sea of gates architecture (obsolete today)
- SPLDs (simple PLDs).
- CPLDs (complex PLDs).
- FPGAs (field programmable gate arrays).

Sea of gates architecture

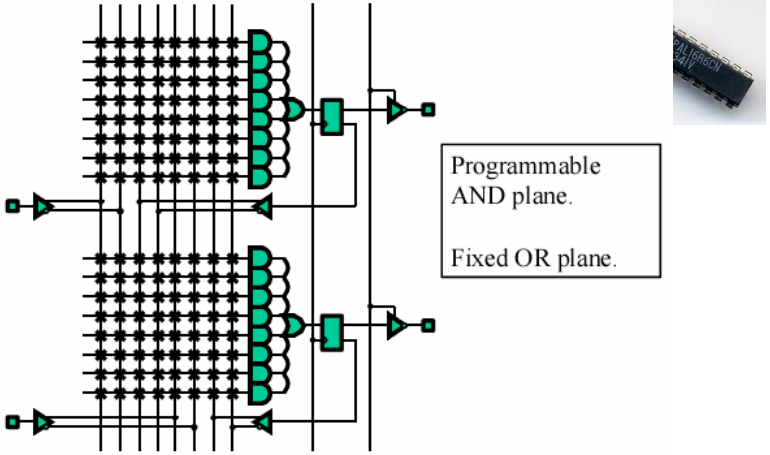


SPLD basic Layout

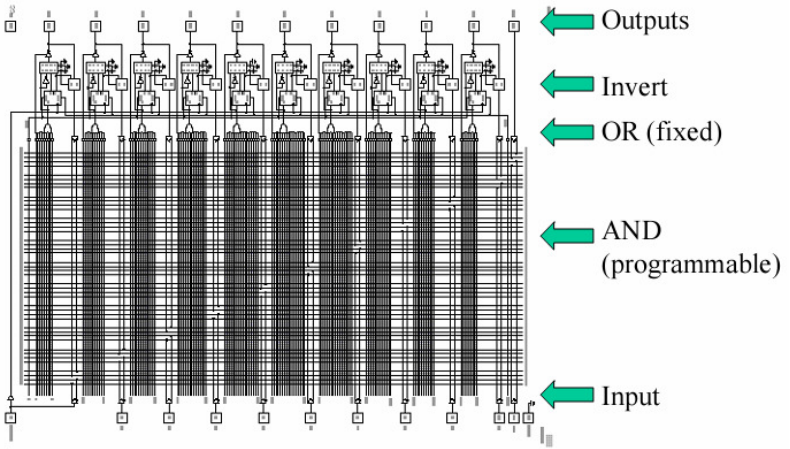


- PAL, PLA and PROM

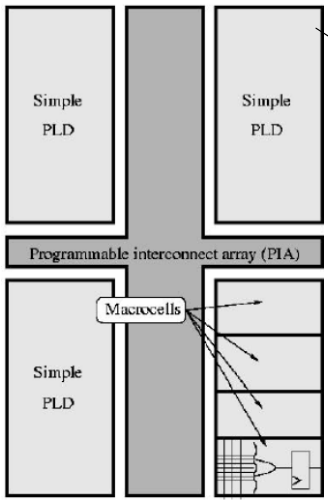
PAL Architecture



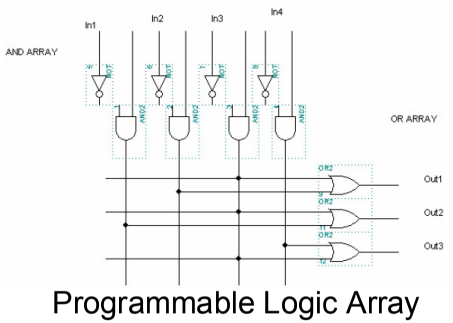
22V10 PAL Logic Diagram



Complex programmable logic device (CPLD)

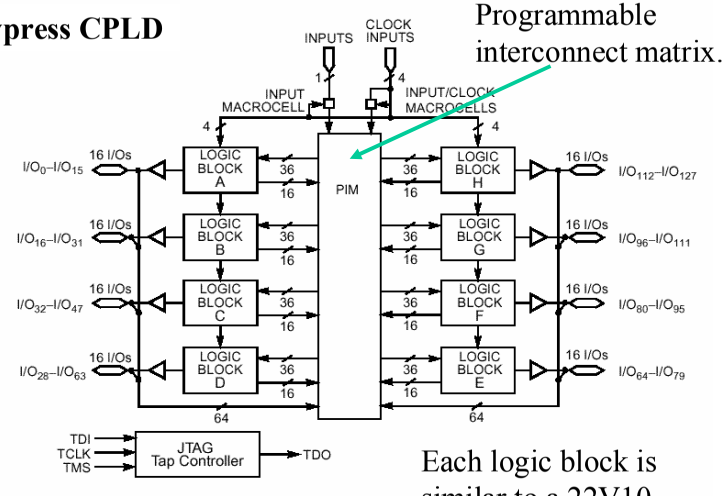


Typically a CPLD consists of 50 SPLDs (An SPLD is a programmable logic array with AND and OR planes)



Programmable Logic Array

Cypress CPLD



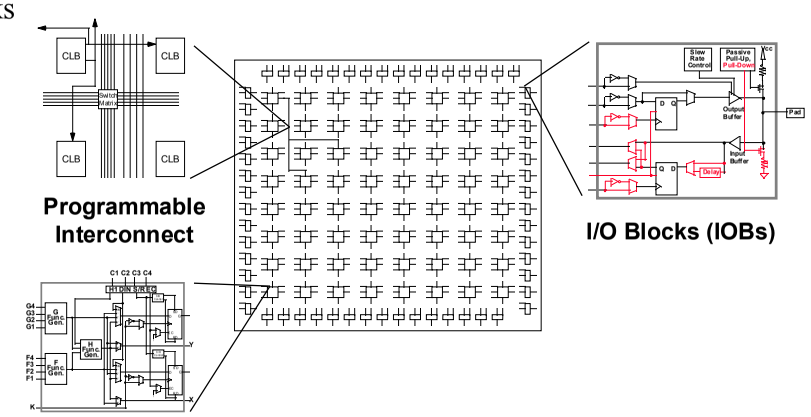
Programmable interconnect matrix.

Each logic block is similar to a 22V10.

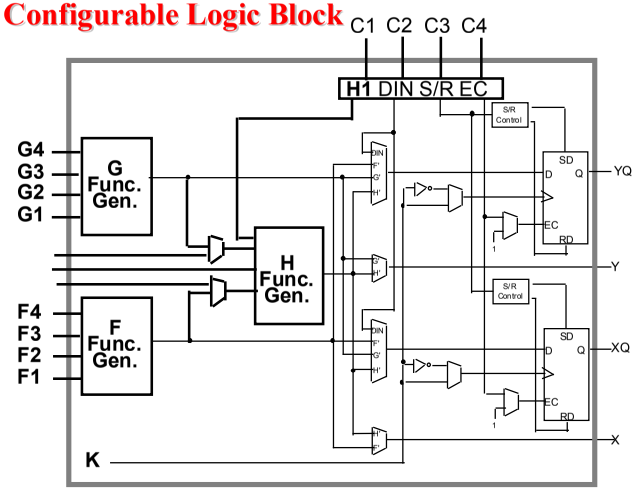
Figure 1. Ultra37128 Block Diagram

FPGA

Programmable devices containing repeated sections of small logic blocks



Xilinx XC4000 Configurable Logic Block



Conceptual difference between PLDs

PLDs - Classification by Granularity

Granularity - What is the logic block size which is being configured

In general three different granularity classes can be found

- Small granularity (sea of gates architecture)
- Medium granularity (FPGA)
- Large granularity (SPLD and CPLD)

If the granularity is less then the effort required to synthesize and complete the wiring between the blocks is high.

If the granularity is high then while implementing a circuit the utilization of available programmable logic is less