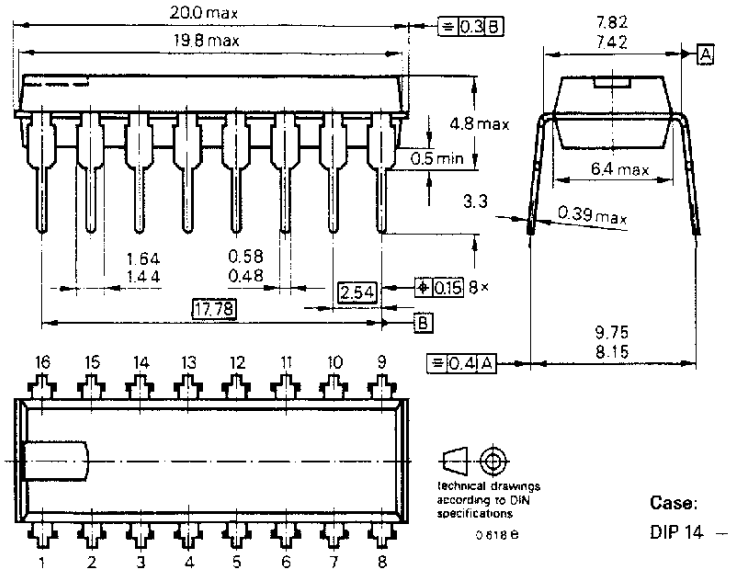
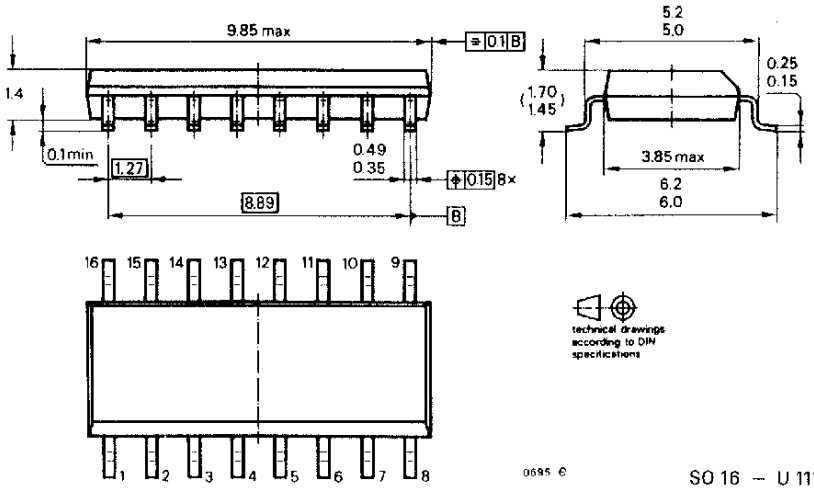
Dimensions in mm



Case:
DIP 14 – U 111 B



SO 16 – U 111 B-FP

We reserve the right to improve technical design

TELEFUNKEN electronic GmbH, P.O.B. 3535, D-7100 Heilbronn

U 111 B · U 111 B-FP

PHASE CONTROL CIRCUIT

General Triac Control with feedback

Technology: Bipolar

Features:

- Additional operational amplifier for optional use
- Ignition pulse disenable
- α_{max} switch
- Temperature compensated reference voltage
- Voltage and current synchronisation
- Triggering pulse typ. 150 mA
- Supply voltage control monitoring
- Current consumption ≦ 2.5 mA

Case: DIP 14, SO 16

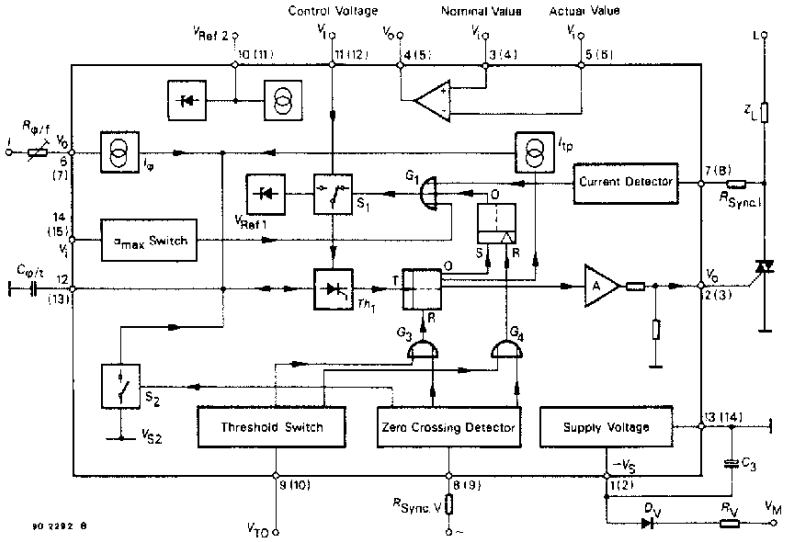


Fig. 1 Block diagram SO 16 in bracket

(1) (16) N.C.

T1.2/696.0491E

Maximum thermal resistance

Junction ambient					
DIP 14		R_{thJA}		170	K/W
SO 16 (P.C.)		R_{thJA}		180	K/W
SO 16 (ceramic)		R_{thJA}		100	K/W

Electrical characteristics			**Min.**	**Typ.**	**Max.**	
Reference point Pin 13, unless otherwise specified						
Mains supply		$-V_S$	13.5		17	V
Current consumption		I_S			2.5	mA
Sync. current	Pin 7	$I_{syncI.}$	0.35			mA
	Pin 8	I_{syncV}	0.65			mA
Output pulse current						
$V_S = 13.5$ V, $R_V = 0$	Pin 2	i_o	90		180	mA
$V_G = 1.2$ V						
Output pulse width						
$C_{\varphi/t} = 3.3$ nF	Pin 2	t_p		8	30	µs
$C_{\varphi/t} = 6.8$ nF		t_p		15	64	µs
Charge current "Phase 1"						
$C_{\varphi/t} = 3.3$ nF	Pin 12	I_φ		2		µA
$C_{\varphi/t} = 6.8$ nF	Pin 12	I_φ		4.3		µA
Charge current "Phase 2"	Pin 12	I_t		1.3		mA
Control current	Pin 11	I_i			0.5	µA
Reference voltage						
$I_o = 10$ µA	Pin 10	V_{Ref1}	8.1	8.7	9.5	µA
Threshold switch	Pin 9					
Logic-off		$-V_{TON}$	1.5		3.7	V
Logic-on		$-V_{TOFF}$	0.7		2.3	V
α_{max}-switch	Pin 14	$-V_{TO}$	0.7		1.1	V
Balance between two half cycles when						
V_{11} = constant		Δ_φ			± 3°	
Operational amplifier						
Input offset voltage	Pin 3, 5	V_{IO}		15		mV
Input offset current	Pin 3, 5	I_{IO}			1	µA
Input bias current	Pin 3, 5	I_{IB}			1	µA
Open loop gain	Pin 4	G_{VO}		70		dB
$f = 50$ Hz						
Common mode rejection ratio	Pin 4	CMR		80		dB
$f = 50$ Hz						
Common mode input range	Pin 4	$-V_{IC}$	1		(V_S-1)	V

In the following zero transition of the mains voltage, the zero transition detector (Input Pin 8) resets the RS flip-flop, discharges $C_{\varphi/t}$ again via S_2, and also insures that the clock flip-flop is in the reset condition. A further part of the basic functions is the current detector with its input at Pin 7 (Fig. 4). When controlling inductive loads, the load current lags behind the mains voltage which means that the circuit could generate an ignition pulse during the period in which current is still flowing with a polarity opposite to that of the mains voltage if the current were not taken into account. This, in turn, would lead, to so-called "gaps" in the load current as the next ignition pulse is generated in the subsequent half-cycle.
In indication as to whether load current is flowing or not is provided by the triac itself. When the triac is ignited, the voltage at electrode H_1 drops from the instantaneous value of the mains voltage to approx. 1.5 V, the value of the forward voltage of the triac. When the load current drops below the hold current of the triac towards the end of the half-cycle, V_{H1} again returns to the instantaneous value of the mains voltage (Fig. 5).
The current detector with its input at Pin 7 now controls this triac voltage and blocks the pulse generator via G_1 and S_1 by increasing the reference voltage as long as the triac is conducting.
As, in the case of a resistive load, the triac may be extinguished shortly before the zero transition of the mains voltage – when the load current drops below the holding current – the RS flip-flop must prevent any possible second ignition pulse from being generated (Fig. 6)

Additional functions

Apart from that there is an internal frequency response compensated operational amplifier (pins 3, 4, 5). It realises complete regulation with well defined time charac. easily.
Pin 14 is the input to a voltage controlled load current limiting circuit. An increase of a control voltage above a specific value, switches the current phase ($=\alpha_{max}$) to the minimum current phase angle preset via Pin 6.
An internal supply voltage control circuit insures that output pulses can be generated only when the supply voltage required for operation of all logical functions is available.
Simultaneously, this block provides the possibility of switching off the pulse generation when the potential at Pin 9 rises above a defined threshold. This permits, for example, simple monitoring of the device temperature by means on an NTC voltage divider.
A temperature compensated voltage of typically 8.6 V is available at Pin 10, whereby the load should not exceed 200 µA ≙ 40 kΩ. With suitable power supplies, the current can be increased to a maximum of 15 mA.

Power supply

Two requirements determine the circuit design of the power supply, namely the functional range of $-V_S = 12 \ldots 14$ V for operation from dc voltage and the typical power dissipation in the series resistor for mains operation of 1.5 Watt. As the ignition pulse with a typical value of 150 mA/50 µs already requires a charging current of 500 µA, only typically 2 mA are available for the complete control logic.

DC supply

The supply voltage can be provided by a separate power supply unit if the outputs of the power supply unit are floating or if the positive pole is connected to ground. The dc voltage $-V_S = 12 \ldots 14$ V is connected directly to Pin 1.

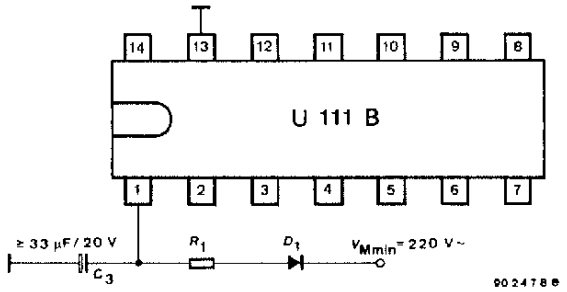


Fig. 7

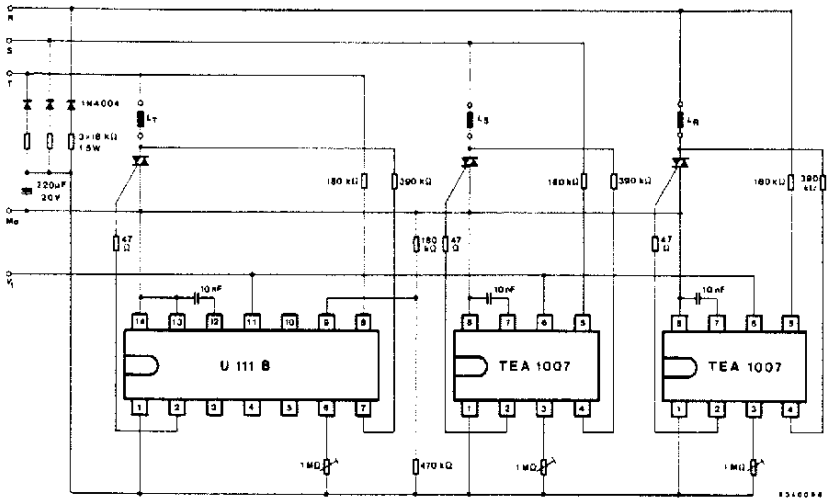


Fig. 12 Three phase power control unit with U 111B and TEA 1007

Dimmer switch

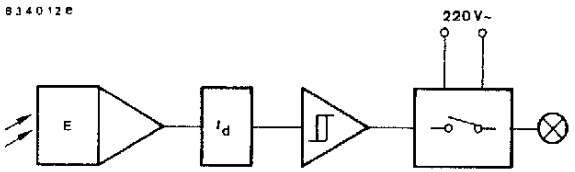


Fig. 13 Block diagram

Using the IC U111B, a twilight-switch requiring few components can easily be realised. The sensitivity and thus also the threshold-level can be adjusted over a wide range. Moreover steps are taken to ensure that short-term fluctuations of the light intensity do not lead to uncontrolled switching action.
The sensitivity of the sensor consisting of phototransistors T_1 and T_2 is adjusted by R_{25} (Fig. 14). The larger the value of R_{25}, the more sensitive the circuit, i.e. it is switched on by relatively lower light intensities. For $R_{25} = 0$ Ohm, only T_1 is effective.
As the brightness decreases, C_5 is charged via R_{17} and D_2 (finally also via R_{16}) to a potential equal to that produced at the collector of T_1 and T_2 by the instantaneous intensity ratios. If the collector voltage falls lower, C_5 is discharged via R_{16} to the new collector potential. The time-constant formed by the component values of R_{16}, R_{17} and C_5 operates to prevent fluctuations of intensity from taking immediate effect on the comparator connected to it.
The comparator, which has a hysteresis adjustable between 0.3 and 3 Volt, operates together with the time-delay just described to prevent undesired switching action. It is composed of R_{11}, R_{12}, R_{13}, R_{15}, R_{24} and the internal operational amplifier.

The power stage, comprising the remaining components of the U 111B, works in the switched mode with a fixed conduction angle and is controlled via Pin 9. The conduction angle is set by the potential applied to Pin 11. The voltage-divider formed by R_3, R_6 and R_9 supplies in addition the reference voltage for the comparator, which is smoothed by C_4. R_4 and R_7 are used for the synchronisation of the circuit. R_{21} should be adjusted so that the lamp being switched does not flicker. (The power-supply is designed to produce only one triac-firing pulse per half-cycle).

General Description

The phase-shift of the ignition point is determined in the usual manner by comparison between a mains synchronized ramp voltage and a predetermined required value. The capacitor $C_{\varphi/t}$ between Pin 12 and the common reference point Pin 13 is discharged at the zero transition of the mains voltage via the V_0 detector and switch S_2. After the end of the zero transition pulse, $C_{\varphi/t}$ is charged from the constant current source I_{φ}, whose value is adjusted externally with R_{φ} at Pin 6 due to the unavoidable tolerance of $C_{\varphi/t}$ (Phase 1).
When the potential at Pin 2 reaches the nominal value predetermined at Pin 11, the thyristor Th_1 – which also functions as a comparator – ignites and sets the following clock flip-flop. The output of the clock flip-flop releases the output amplifier, connects a second constant current source to the capacitor $C_{\varphi/t}$, and switches the reference voltage switch S_1 to an internally generated threshold voltage via an RS flip-flop and the OR gate G_1.
The capacitor $C_{\varphi/t}$ is charged in this second phase by $I_{\varphi} + I_{tp}$ until it reaches the internal reference voltage V_{Ref1}. The duration of this Phase 2 corresponds to the width of the output pulse t_p. When the capacitor voltage reaches the value V_R, thyristor Th_1 ignites again and resets the clock flip-flop to its initial state. The output pulse is thus terminated and the constant current source I_{tp} is switched off. However, the RS flip-flop holds the switch S_1 so that the internal reference voltage remains connected to Th_1. As V_{Ref1} is greater than the maximum permissible control voltage at Pin 11, this prevents more than one ignition pulse from being generated in each half-cycle of the mains voltage. This is particularly important because the energy contents of the output pulse is of the same order as the internal requirements of the circuit for each half-wave.

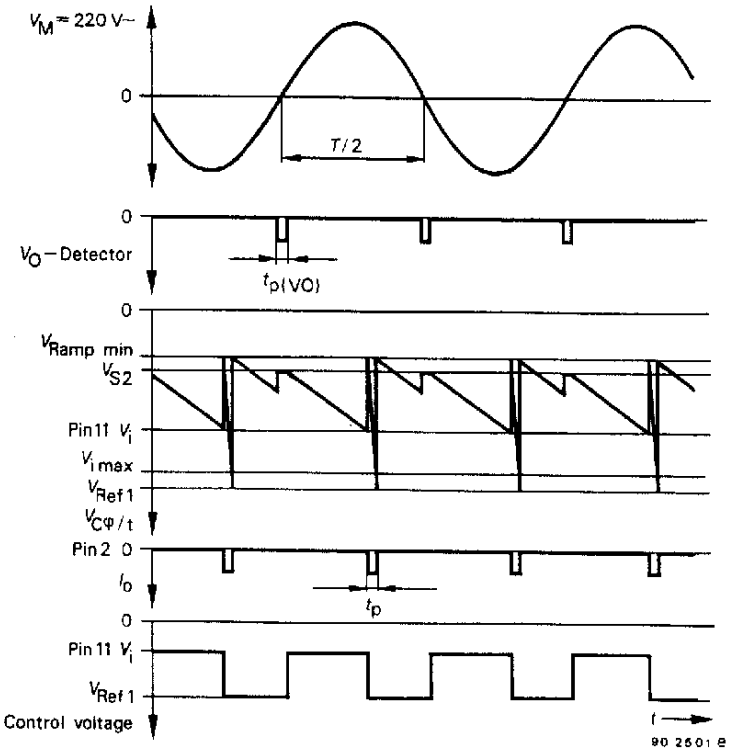


Fig. 3 Basic functional diagram

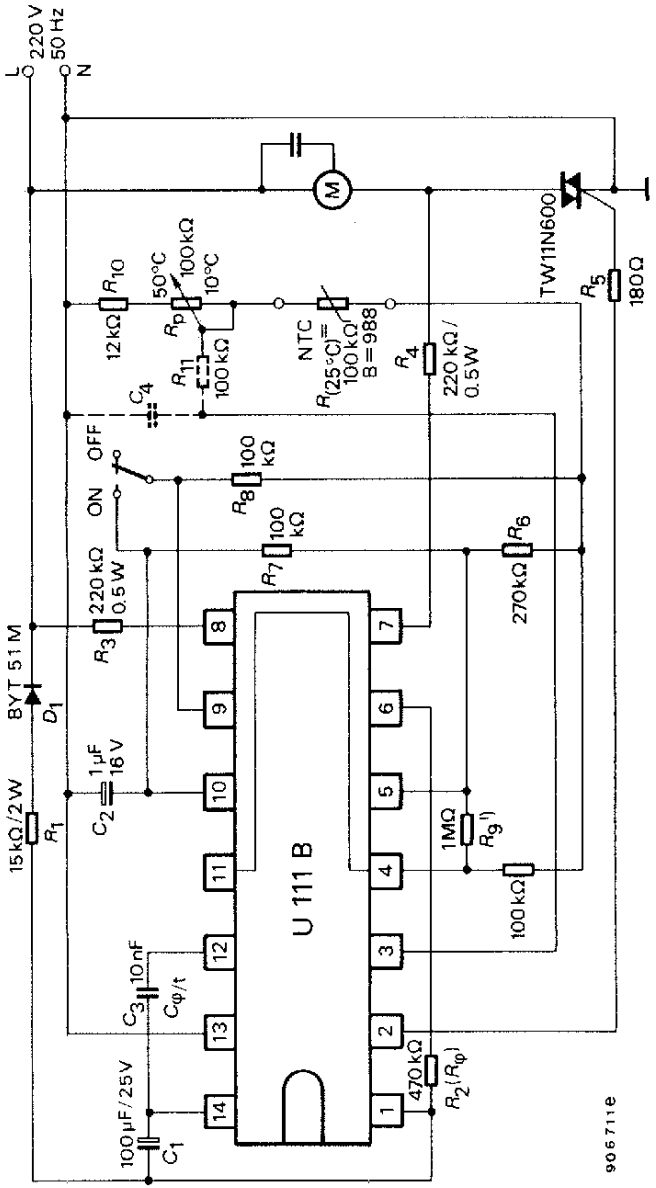


Fig. 2 Application for temperature control (ventilation) with start-stop function, 10 °C ... 50 °C
1) R_g determines proportional amplification

The power supply for the whole circuit is derived direct from the mains supply via D_1 and R_1 in every negative half-cycle. C_3 smooths the operating voltage, which settles at ca. 15.5 Volt.

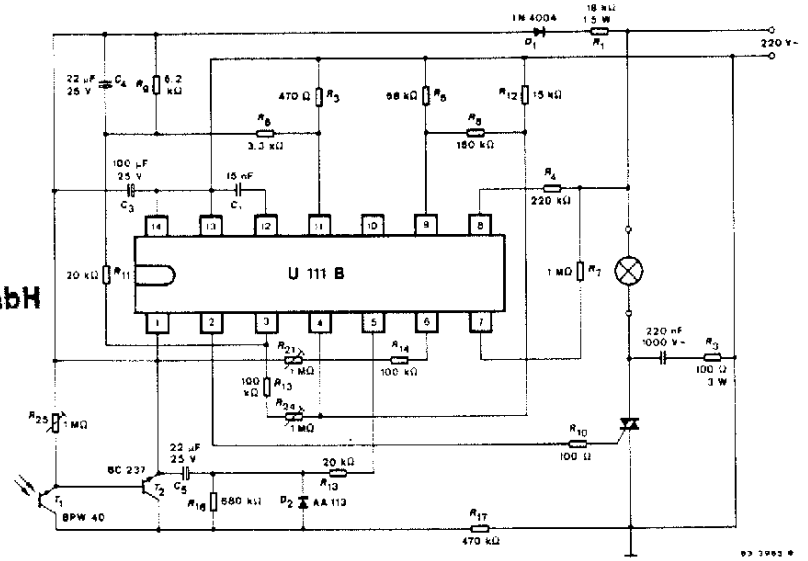


Fig. 14 Dimmer switch with the IC U 111B and phototransistor BPW 40 as sensor

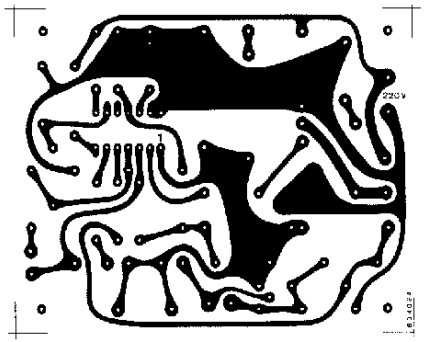


Fig. 15 Circuit board layout

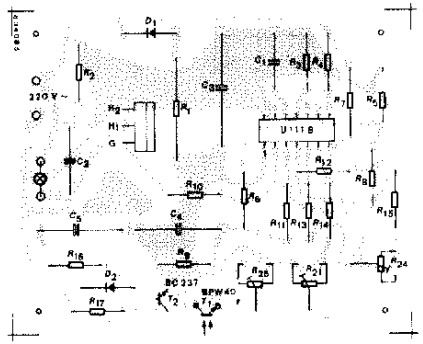


Fig. 16 Printed board with components

Series resistance R_1 can be calculated, approx. as follows:

$$R_{1\,max} = 0.85\ \frac{V_{M\,min} - V_{Smax}}{2\ I_{tot}}$$

$I_{tot} = I_S + I_P + I_x$ whereas

I_{tot} = Total current consumption

I_S = Current requirement of the IC

I_P = Average current requirement of the triggering pulses

I_x = Current requirement of other peripheral components

Appendix gives further informations regarding the design.

Determination of gate series resistance, firing current and pulse width

Firing current requirement depends upon the triac used which can be regulated with series resistances as given below:

$$R_{Gmax} \approx \frac{12.5 - V_{Gmax}}{I_{Gmax}} - 110\ \Omega$$

$$I_P = \frac{I_G}{T} \cdot t_p$$

$$t_P \approx \frac{8\ \mu s}{nF} \cdot C\varphi$$

whereas V_G = Triac's gate voltage

I_G = Triac's gate current

I_P = Gate current requirement – average

T = Mains frequency duration

t_P = (firing) pulse width

C_φ = Ramp capacitor

Adjustment of the constant current I_φ with resistor R_φ.
If the value of the charging current I_φ is known, then the value of the adjusting resistor R_φ is calculated as follows.

$$R_\varphi = \frac{V_R}{I_\varphi}$$

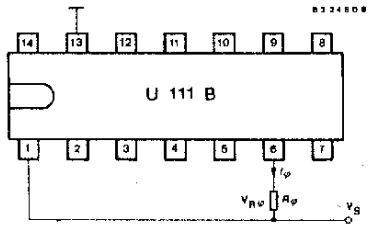


Fig. 8 I_φ adjustment

Determination of constant current I_φ.

The value of the constant current I_φ depends on the charging capacitor $C_{\varphi/t}$ and on the minimum phase angle.

$$I_\varphi = \frac{C_{\varphi/t\,min} \cdot \Delta V_1}{T/2} \qquad \Delta V_1 = V_{S2} - V_{Ref\,1}$$

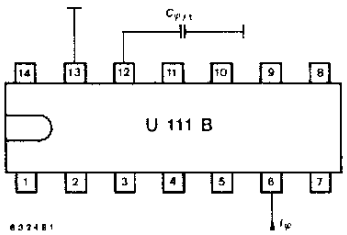
Determination of the charging capacitor $C_{\varphi/t}$

The charging capacitor $C_{\varphi/t}$ is dependent on the required pulse width and on the charging currents I_φ and I_{tp}: When $I_{tp} \gg I_\varphi$: I_φ can be ignored. The charging capacitor is determined as follows:

$$C_\varphi = \frac{t_p \cdot I_{tp}}{\Delta_{V2}} \quad \text{whereas } \Delta V_2 = V_{Ref\,1} - V_{Ramp.\,min}$$

Typical value for $\Delta V_2 = 6$ V, $I_{tP} = 1$ mA

Therefore an approx. pulse width of 6 µs/nF is possible.



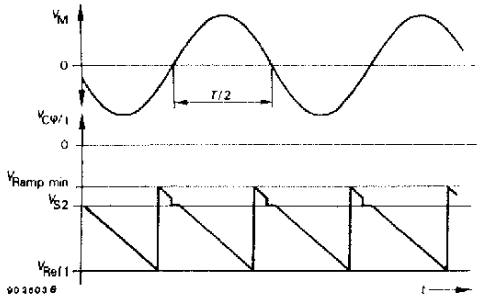
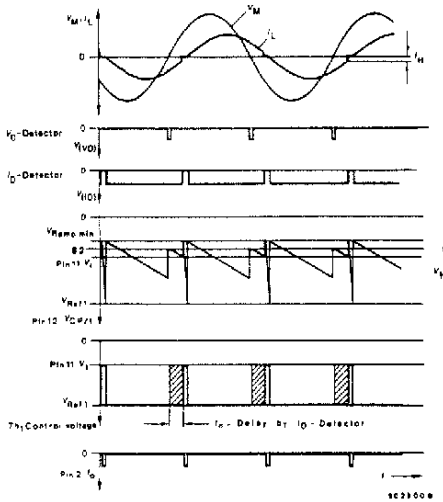


Fig. 9 Pulse width adjustment

Absolute maximum ratings

Reference point Pin 13

Current consumption	Pin 1	$-I_S$	30	mA
Peak current consumption $t<10$ µs	Pin 1	$-I_S$	60	mA
Sync. currents	Pin 7	I_{syncI}	10	mA
	Pin 8	I_{syncV}	60	mA
$t<10$ µs	Pin 7	$\pm I_{syncI}$	60	mA
	Pin 8	$\pm I_{syncV}$	10	mA
Output current	Pin 10	$-I_O$	15	mA
Input current	Pin 6	$-I_I$	5	mA
Input voltages	Pin 2	V_I	$-V_S \leqq V_I \leqq 2$	V
	Pin 11	$-V_I$	$\leqq V_S$	V
	Pin 14	$-V_I$	$\leqq V_S$	V
	Pin 9	$-V_I$	$\leqq V_{Ref}$	V
	Pin 3	$-V_I$	$\leqq V_S$	V
	Pin 5	$-V_I$	$\leqq V_S$	V
Power dissipation		$V_5 - V_3$	$\leqq 7$	V
$T_{amb} = 45$ °C		P_{tot}	470	mW
$T_{amb} = 80$ °C		P_{tot}	265	mW
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	0...80	°C
Storage temperature range		T_{stg}	−40...+125	°C



V_O = Zero cross voltage
I_O = Zero cross current
V_M = Mains voltage
I_L = Load current
I_G = Gate current
V_{H1} = Triac voltage at anode H1

Fig. 4 Functional diagram for inductive load at α_{max}

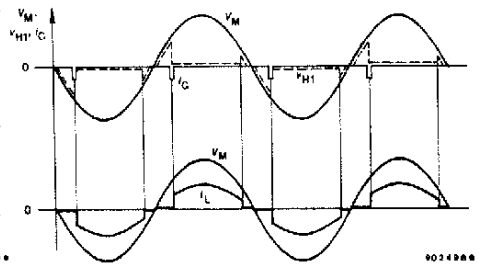


Fig. 5 Triac voltages and currents at resistive load

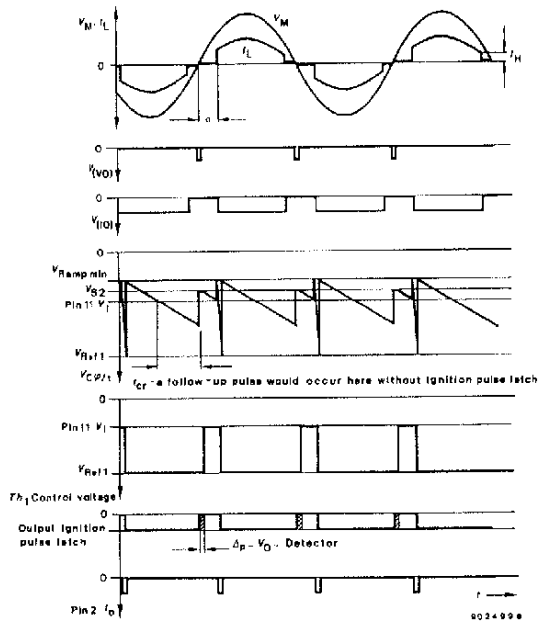


Fig. 6 Functional diagram for resistive load and α_{min}

Applications

Due to further developments of integrated circuit family i.e. U 200 B and U 2000 B, the integrated circuit U 111 B is meant for specified characteristics i.e., single phase ignition and free switchable operational amplifier.
Following are further examples apart from the application given under Fig. 2.

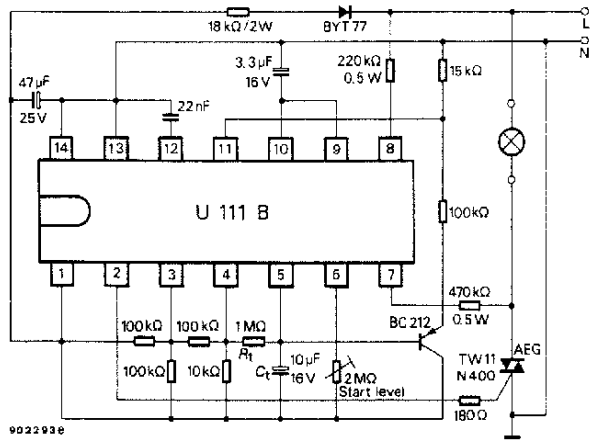


Fig. 10: Dual slope dimmer, cycle time depends upon R_t and C_t

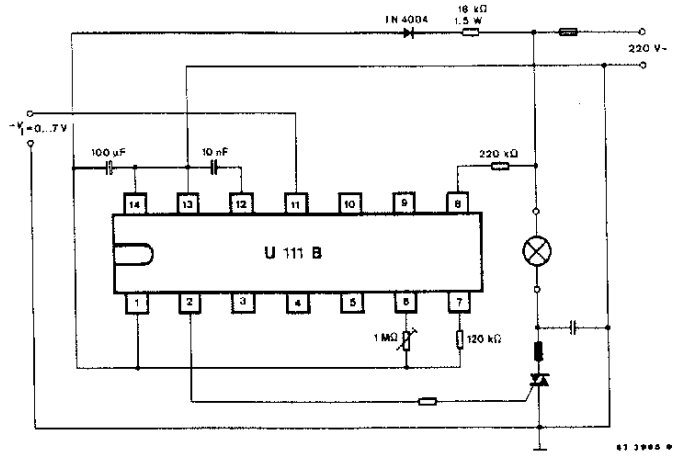


Fig. 11 Light control