

Service Manual

Set Top Box

Model: DST01A

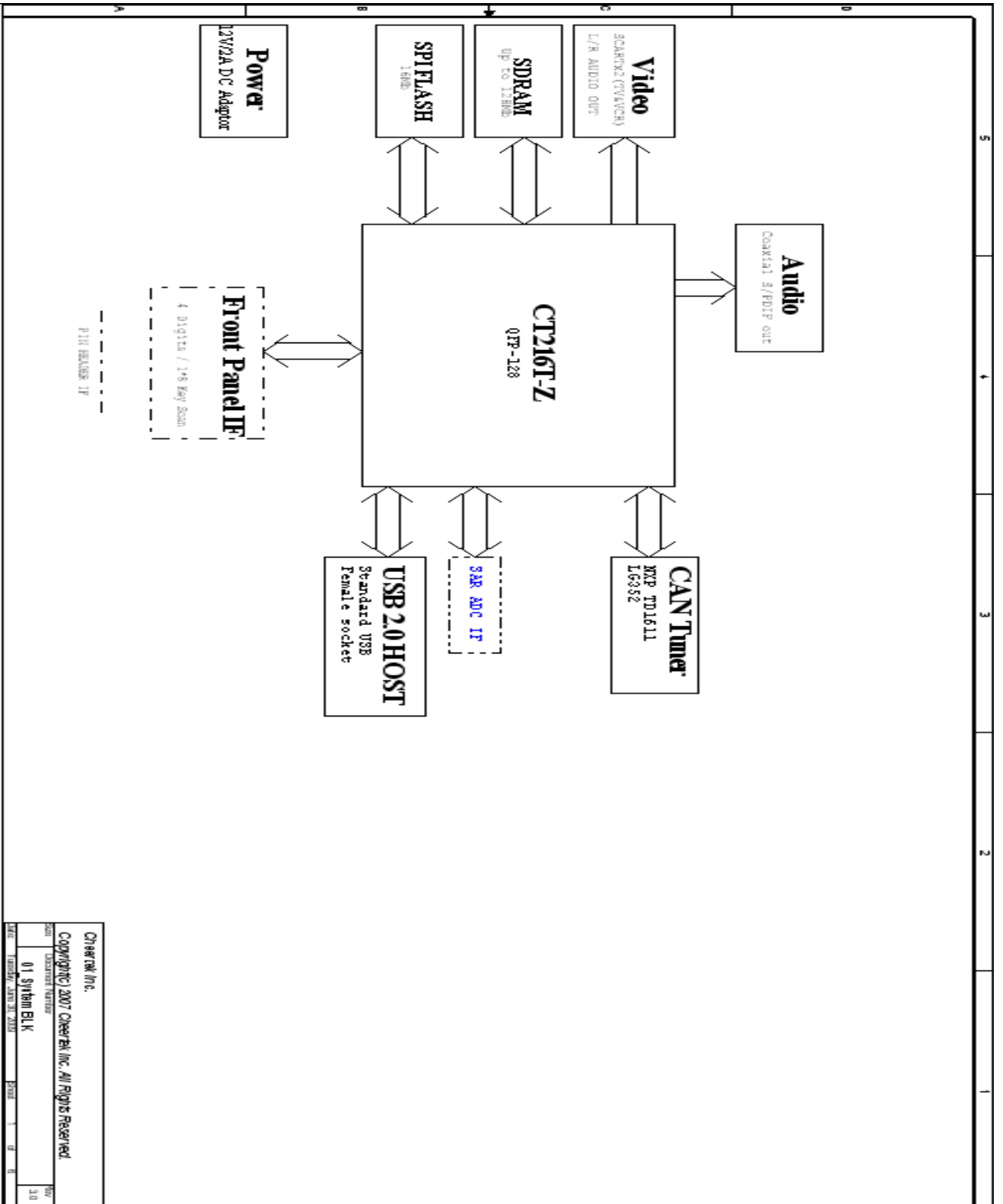


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Troubleshooting

SYMPTOM	CAUSE	REMEDY
1.No power	✂ Check FUSE1, L17,L18,L15,U24	✂ Check FUSE1, L17,L18,L15,U24
2.No picture	✂ Check FB19.Q56 R278	✂ Check FB19,Q56,R278
3.No channel	✂ Check the device around FB22, U22	✂ Replace the device around FB22, U22

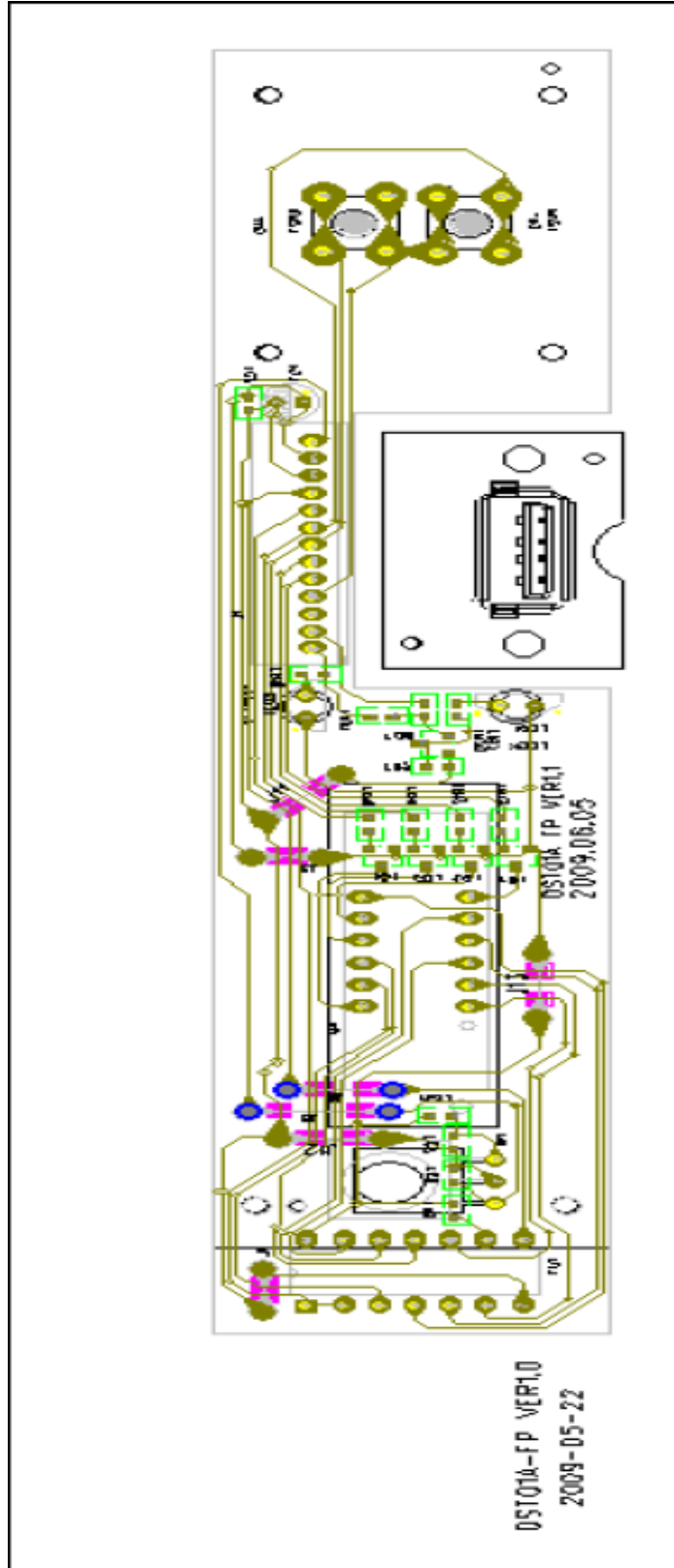
Block diagram



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DATE	DESCRIPTION
01	System BLK
10	

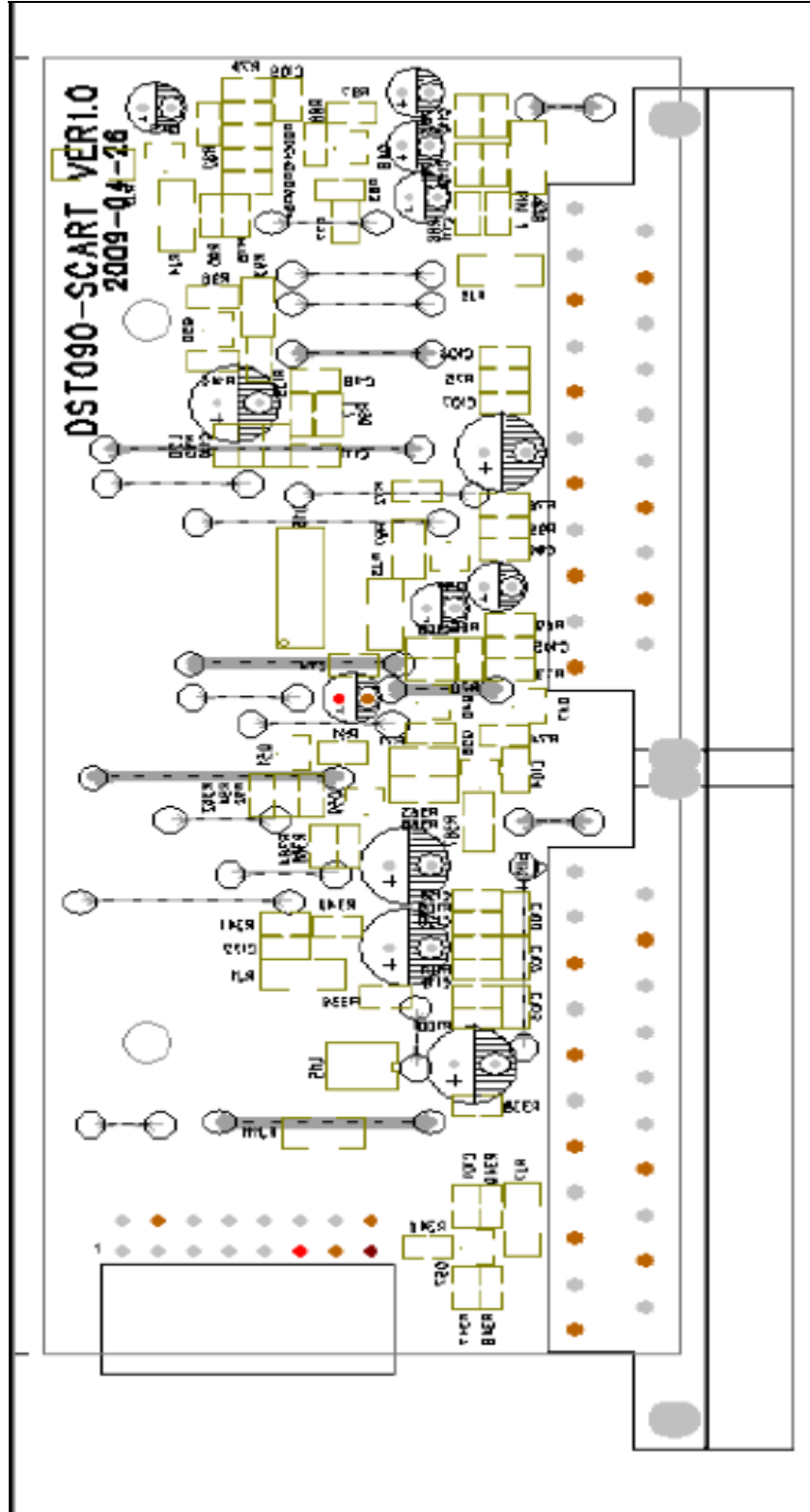
Printed Circuit Board

Front panel

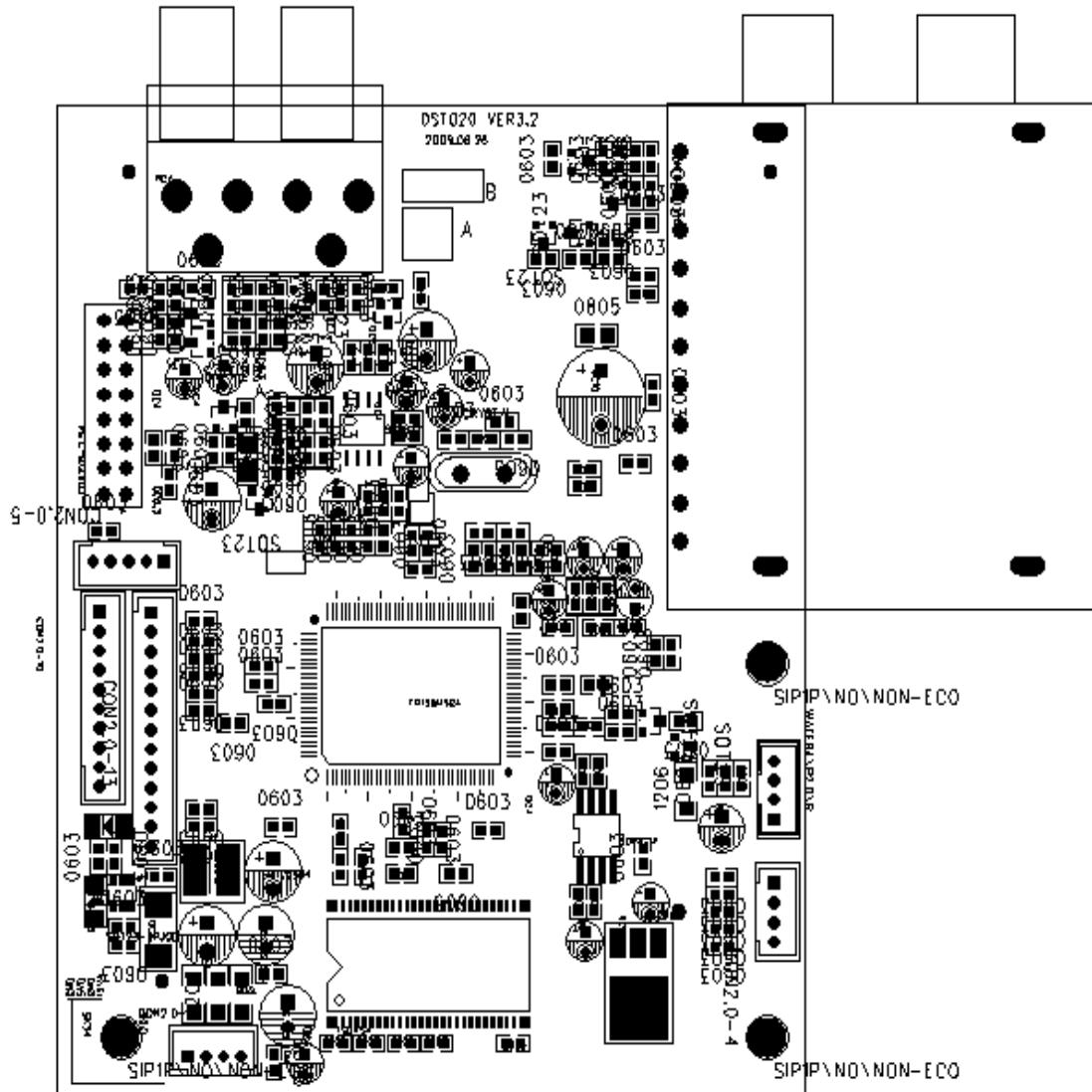


Printed Circuit Board

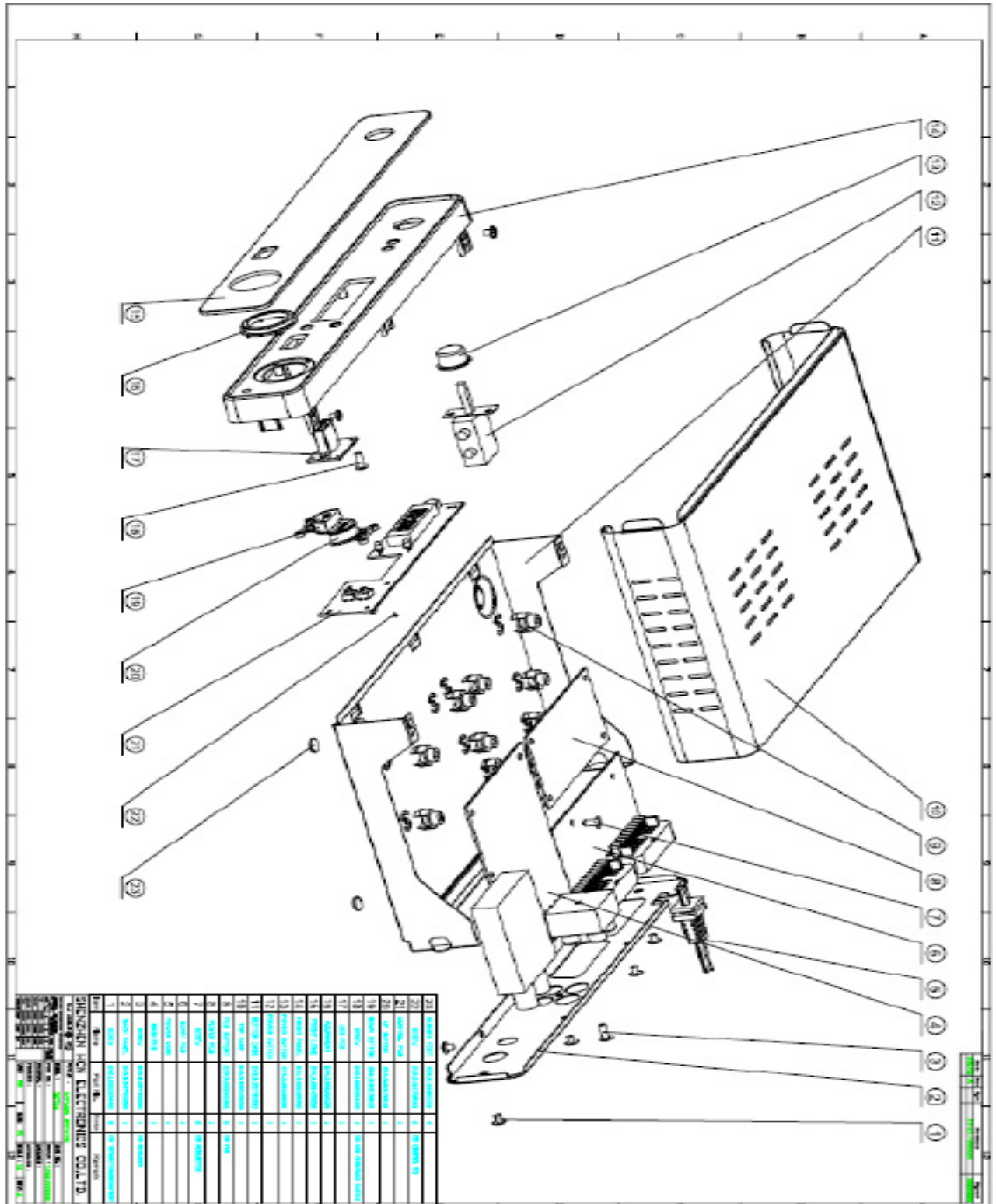
Scart board



Mainboard

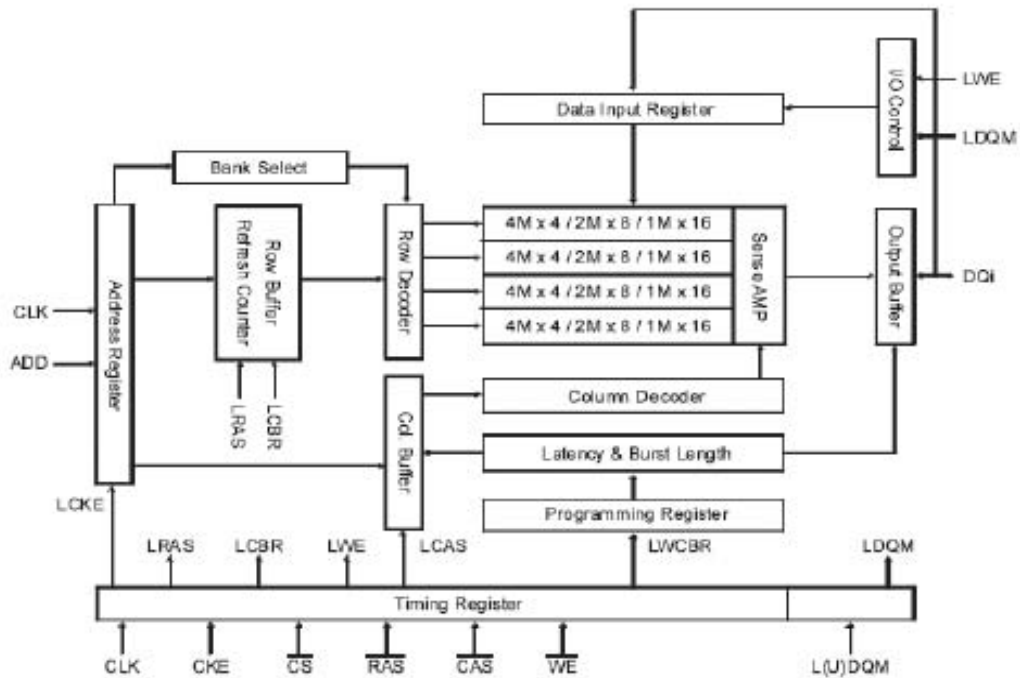


Explosive view



IC function description

IC K4S641632



x16	x8	x4	Pin	Pin	x4	x8	x16
V _{DD}	V _{DD}	V _{DD}	1	54	V _{SS}	V _{SS}	V _{SS}
DQ0	DQ0	N.C.	2	53	N.C.	DQ7	DQ15
V _{DDQ}	V _{DDQ}	V _{DDQ}	3	52	V _{SSQ}	V _{SSQ}	V _{SSQ}
DQ1	N.C.	N.C.	4	51	N.C.	N.C.	DQ14
DQ2	DQ1	DQ0	5	50	DQ3	DQ6	DQ13
V _{SSQ}	V _{SSQ}	V _{SSQ}	6	49	V _{DDQ}	V _{DDQ}	V _{DDQ}
DQ3	N.C.	N.C.	7	48	N.C.	N.C.	DQ12
DQ4	DQ2	N.C.	8	47	N.C.	DQ5	DQ11
V _{DDQ}	V _{DDQ}	V _{DDQ}	9	46	V _{SSQ}	V _{SSQ}	V _{SSQ}
DQ5	N.C.	N.C.	10	45	N.C.	N.C.	DQ10
DQ6	DQ3	DQ1	11	44	DQ2	DQ4	DQ9
V _{SSQ}	V _{SSQ}	V _{SSQ}	12	43	V _{DDQ}	V _{DDQ}	V _{DDQ}
DQ7	N.C.	N.C.	13	42	N.C.	N.C.	DQ8
V _{DD}	V _{DD}	V _{DD}	14	41	V _{SS}	V _{SS}	V _{SS}
LDQM	N.C.	N.C.	15	40	N.C./RFU	N.C./RFU	N.C./RFU
WE	WE	WE	16	39	DQM	DQM	UDQM
CAS	CAS	CAS	17	38	CLK	CLK	CLK
RAS	RAS	RAS	18	37	CKE	CKE	CKE
CS	CS	CS	19	36	N.C.	N.C.	N.C.
BA0	BA0	BA0	20	35	A11	A11	A11
BA1	BA1	BA1	21	34	A9	A9	A9
A10/AP	A10/AP	A10/AP	22	33	A8	A8	A8
A0	A0	A0	23	32	A7	A7	A7
A1	A1	A1	24	31	A6	A6	A6
A2	A2	A2	25	30	A5	A5	A5
A3	A3	A3	26	29	A4	A4	A4
V _{DD}	V _{DD}	V _{DD}	27	28	V _{SS}	V _{SS}	V _{SS}

54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

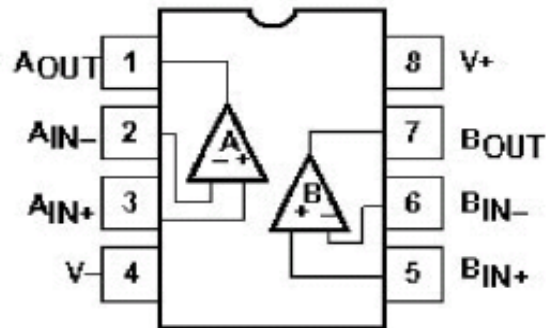
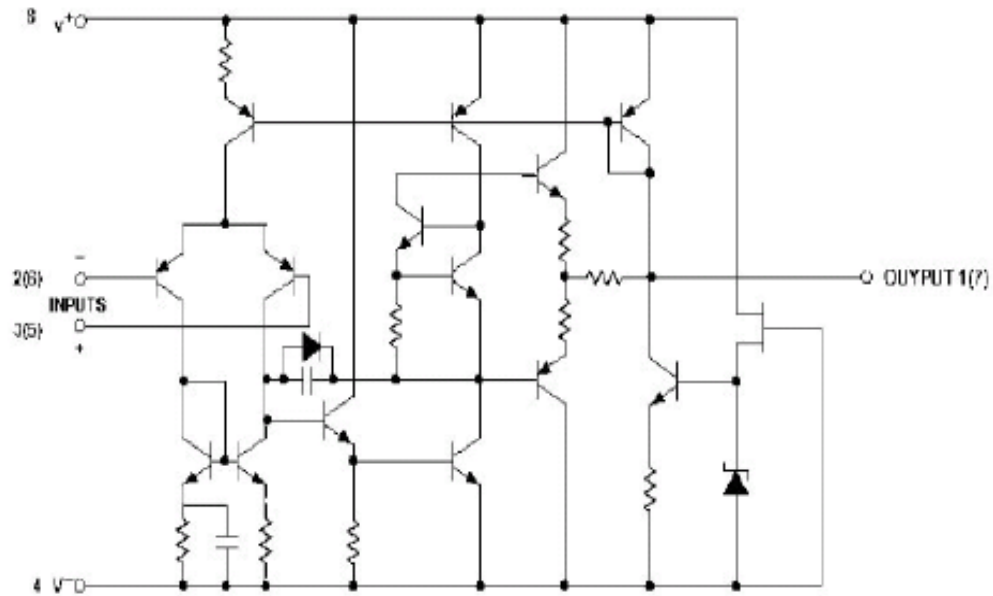
IC function description

IC K4S641632

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A ₀ ~ A ₁₁	Address	Row/column addresses are multiplexed on the same pins. Row address : RA ₀ ~ RA ₁₁ , Column address : (x4 : CA ₀ ~ CA ₃ , x8 : CA ₄ ~ CA ₇ , x16 : CA ₈ ~ CA ₁₁)
BA ₀ ~ BA ₁	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low, Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low, Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
DQ ₀ ~ DQ ₁₅	Data input/output	Data inputs/outputs are multiplexed on the same pins.
V _{DD} /V _{SS}	Power supply/ground	Power and ground for the input buffers and the core logic.
V _{DDQ} /V _{SSQ}	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C./RFU	No connection reserved for future use	This pin is recommended to be left No Connection on the device.

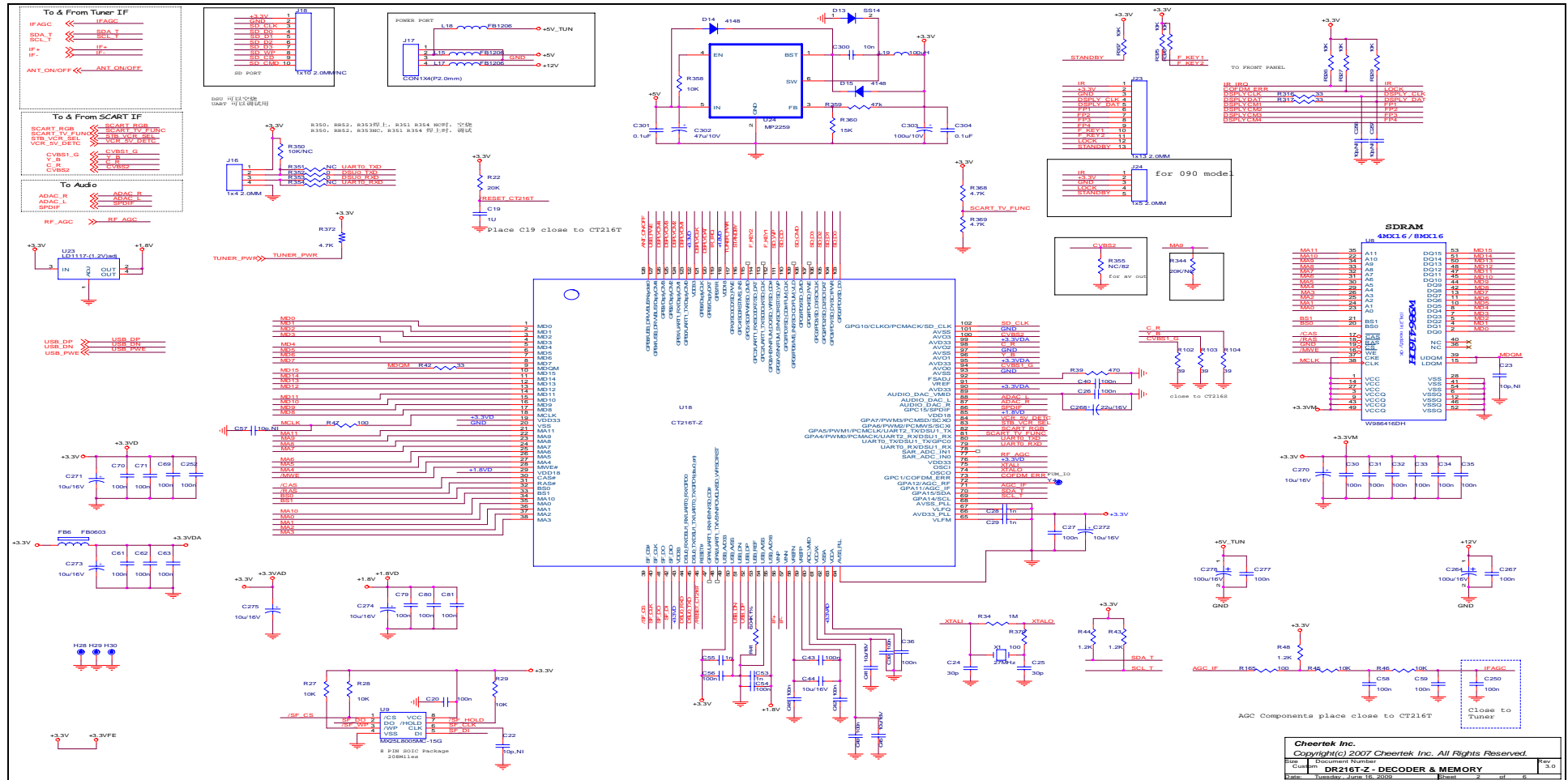
IC function description

IC C4558

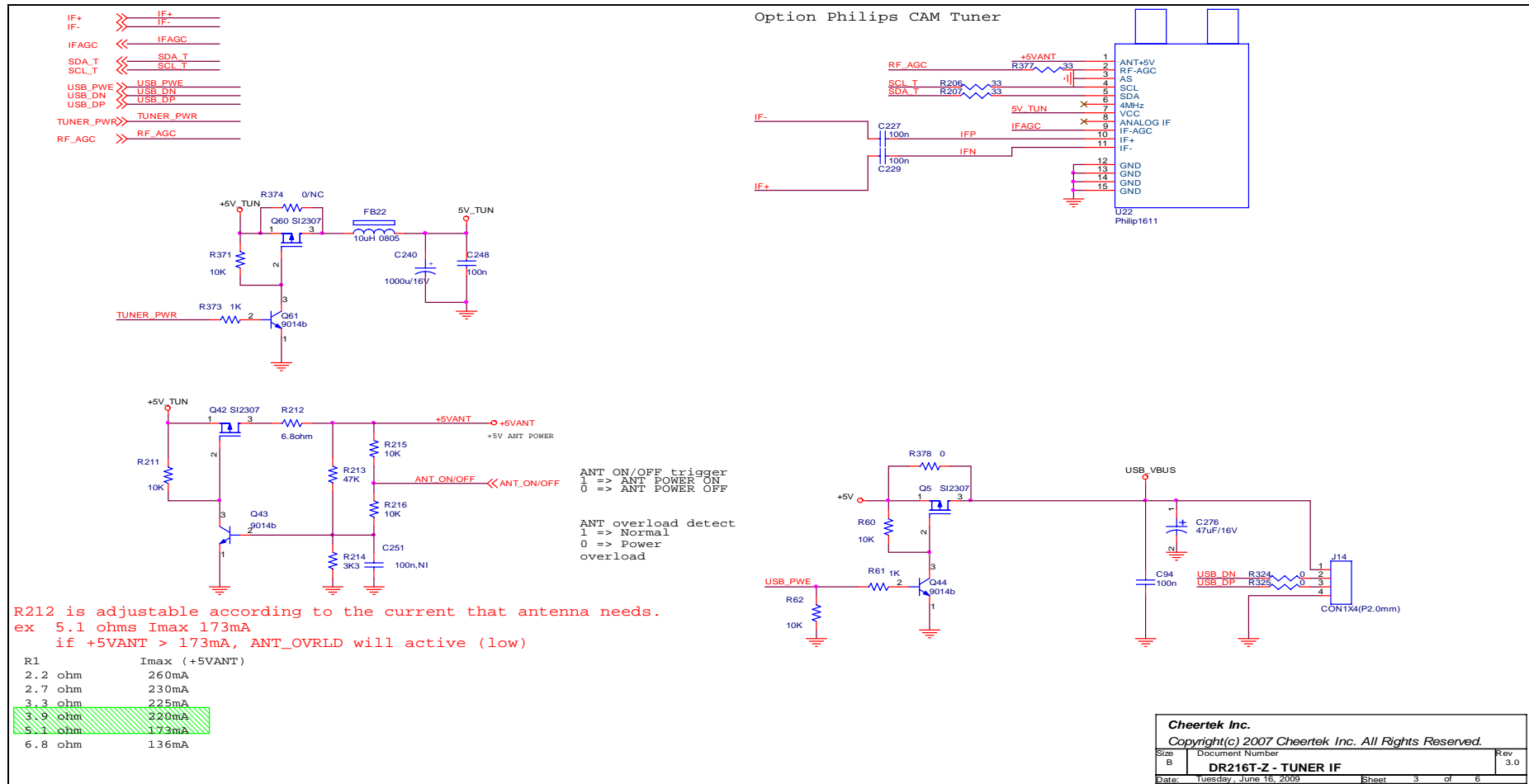


PIN	NAME	PIN	NAME
1.	AOUT	5.	BIN+
2.	AIN-	6.	BIN-
3.	AIN+	7.	BOUT
4.	V-	8.	V+

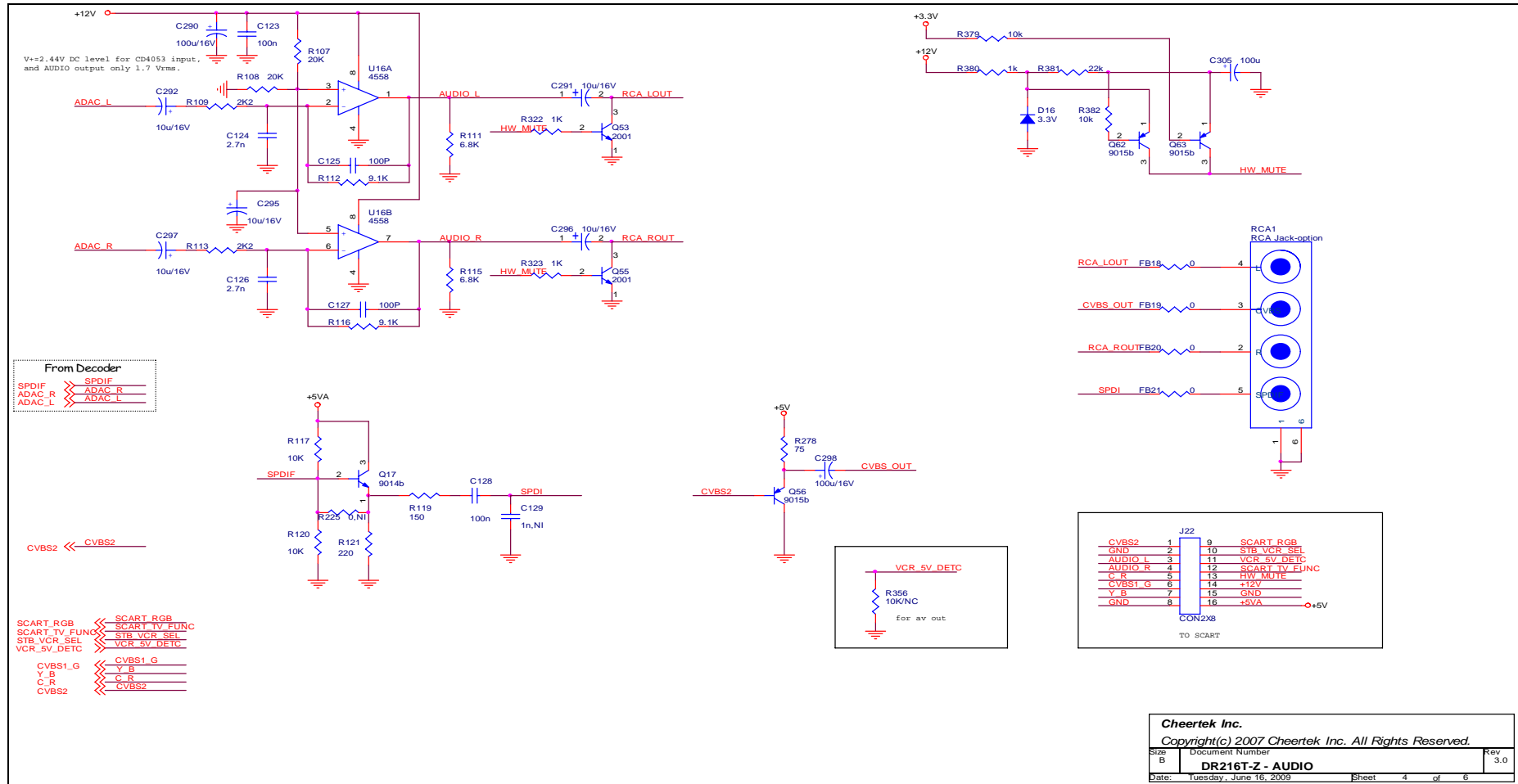
Schematics diagram



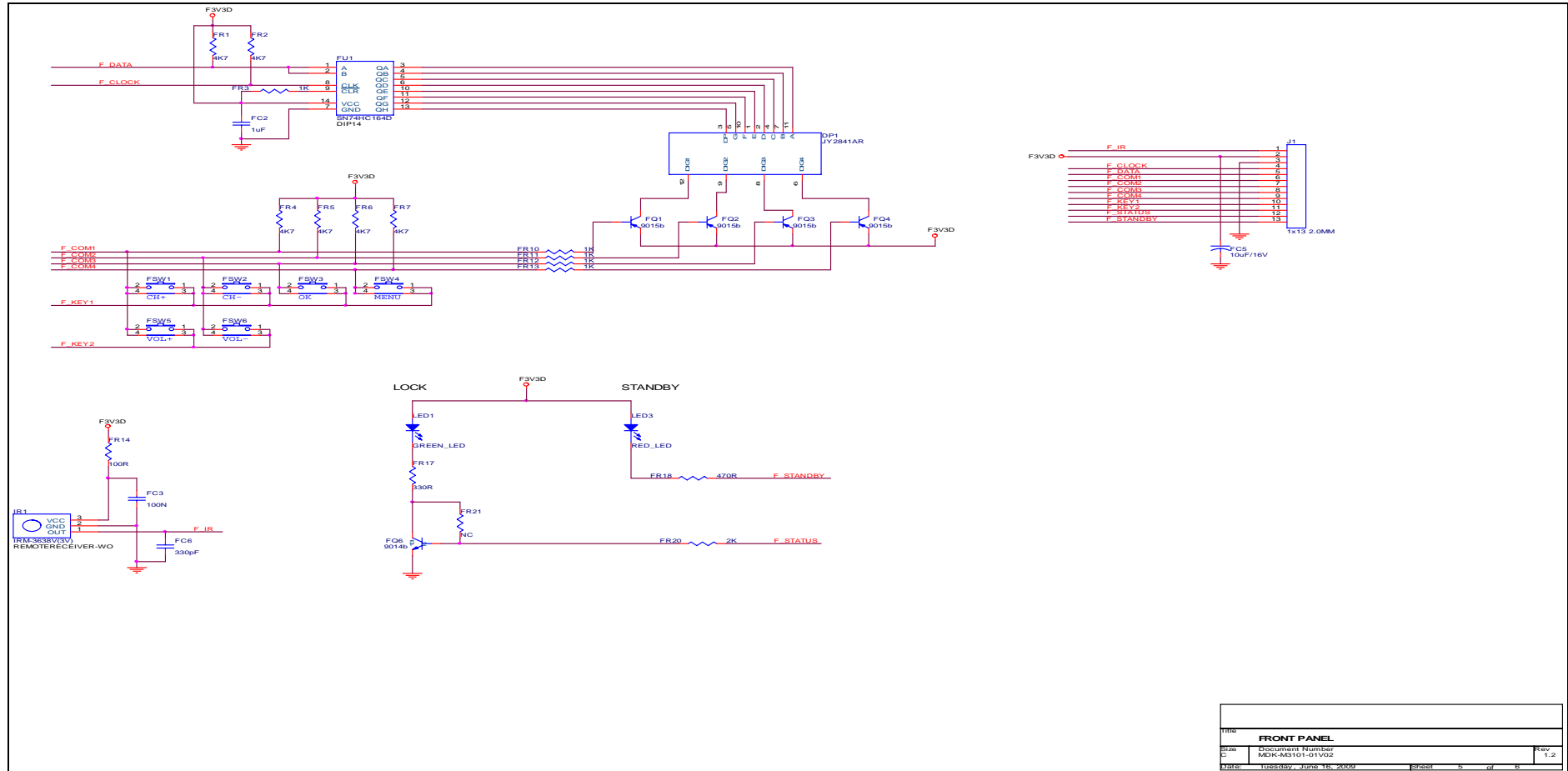
Schematics diagram



Schematics diagram



Schematics diagram



Schematics diagram

