Service Manual

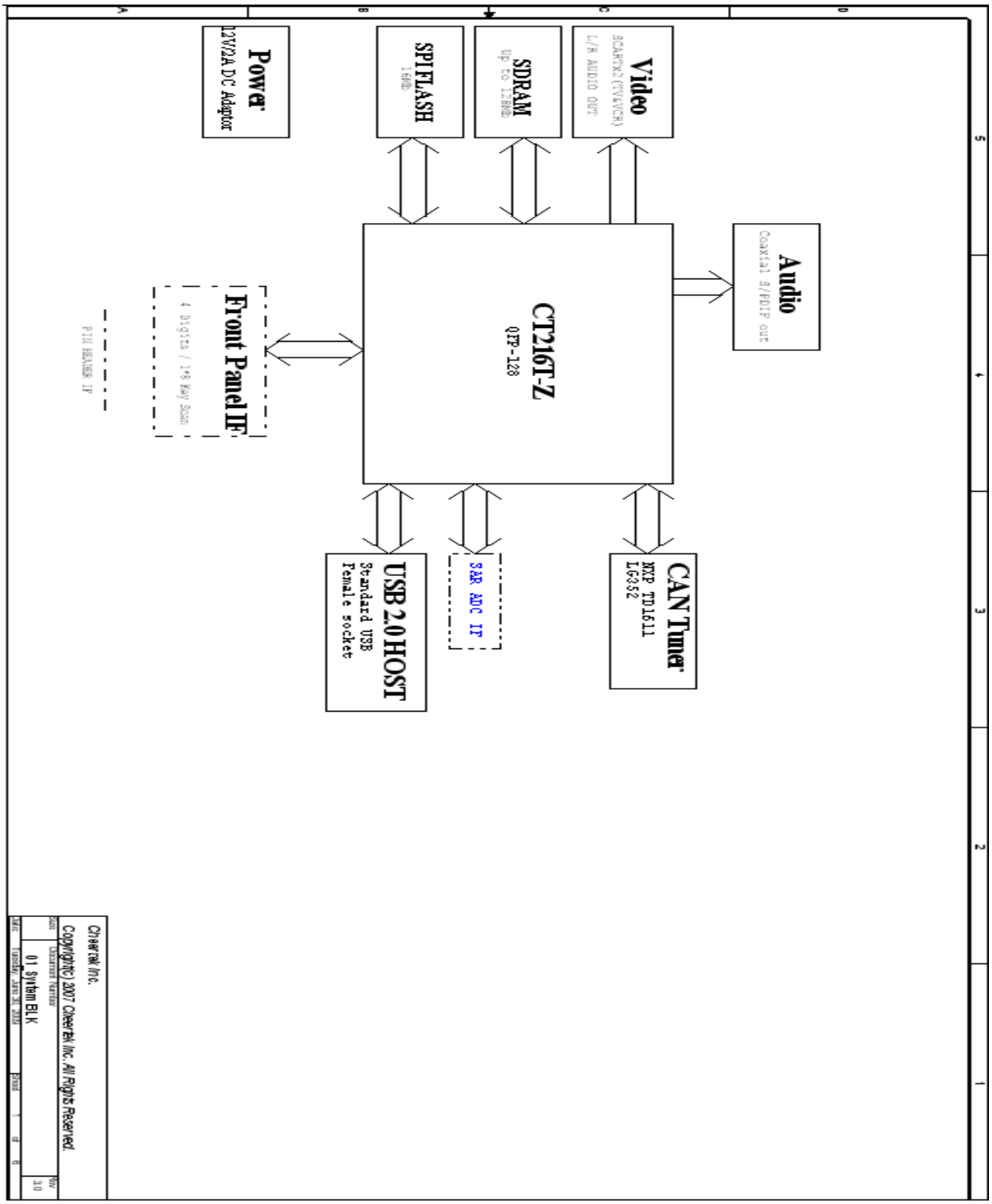
Set Top Box

Model: DST01A

Troubleshooting

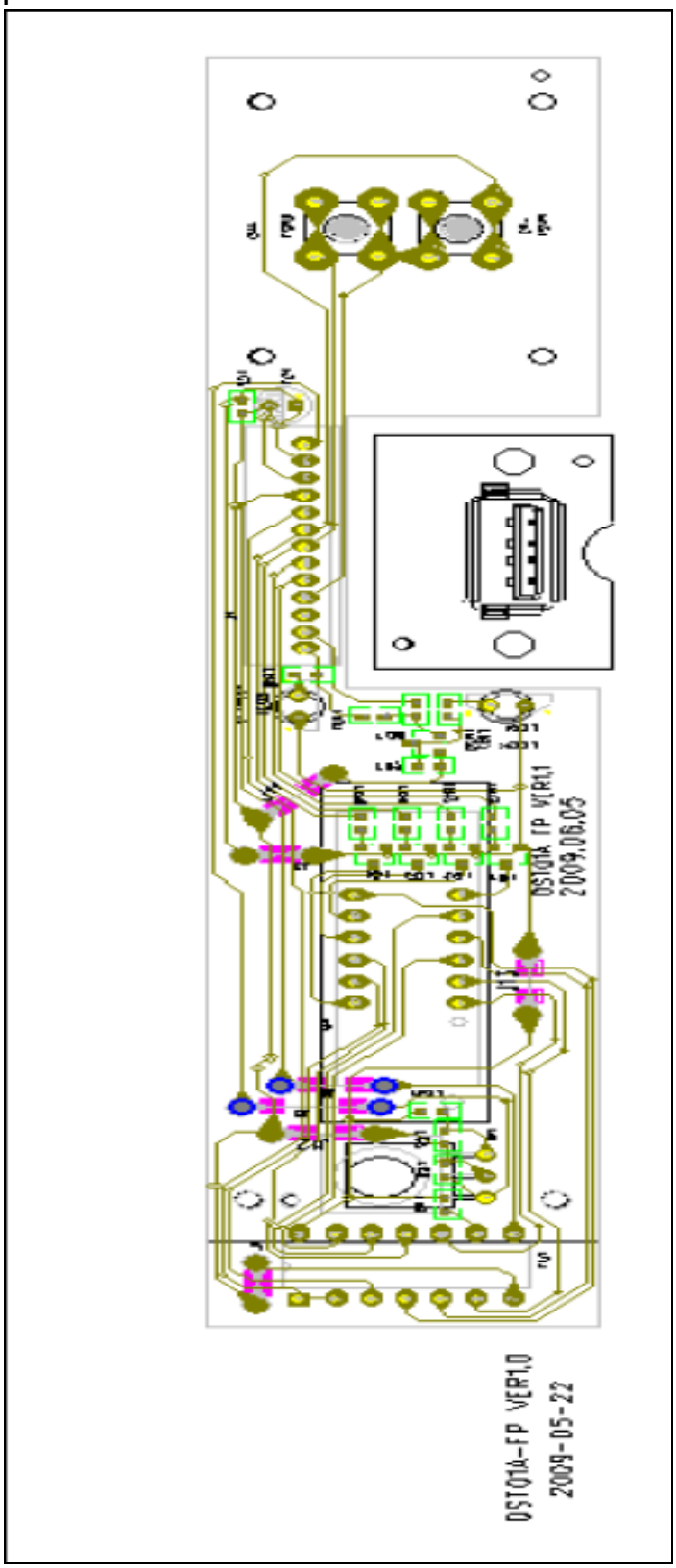
SYMPTOM	CAUSE	REMEDY
1.No power	✂ Check FUSE1, L17,L18,L15,U24	✂ Check FUSE1, L17,L18,L15,U24
2.No picture	✂ Check FB19.Q56 R278	✂ Check FB19,Q56,R278
3.No channel	✂ Check the device around FB22, U22	✂ Replace the device around FB22, U22

Block diagram



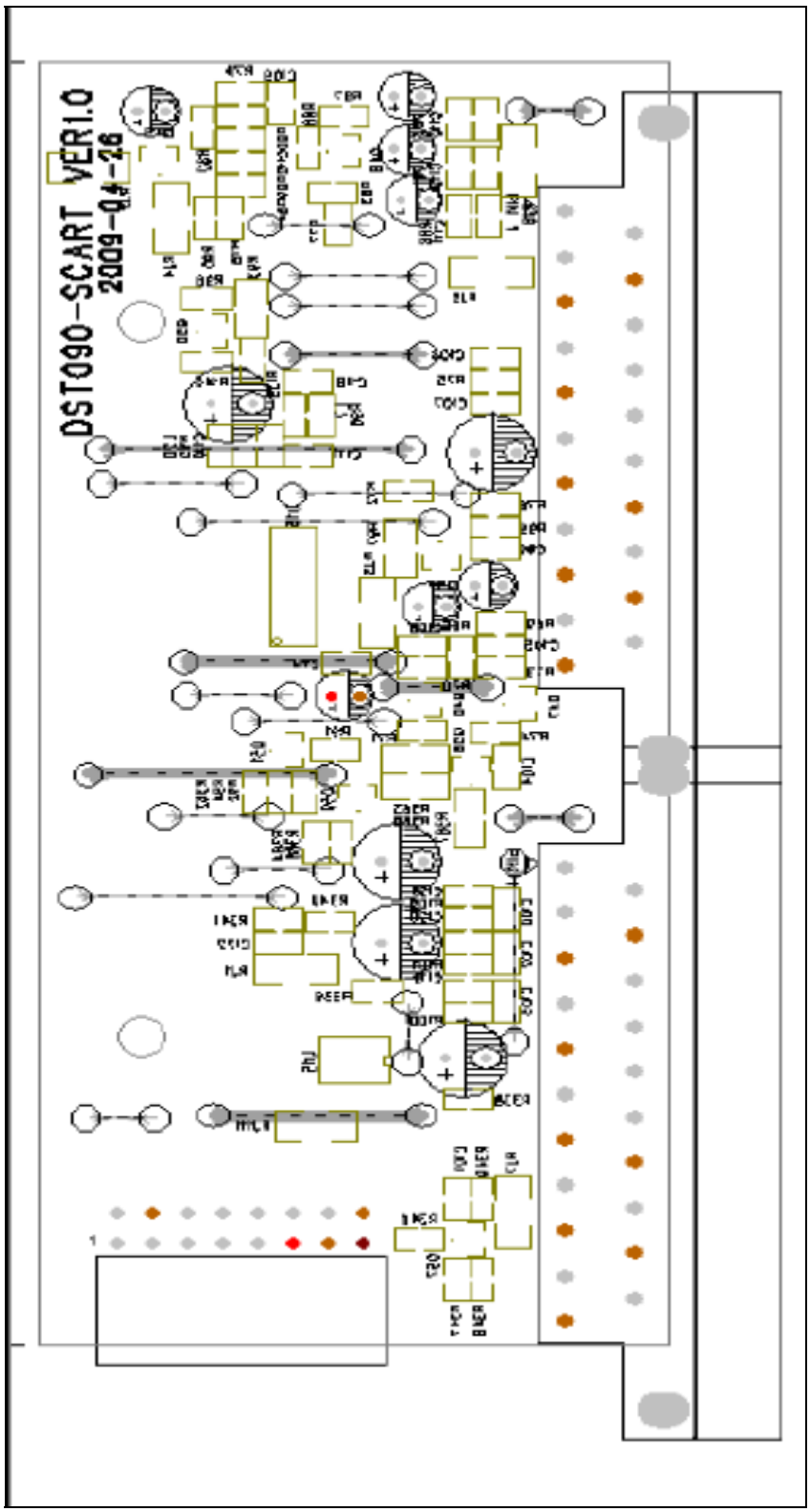
Printed Circuit Board

Front panel

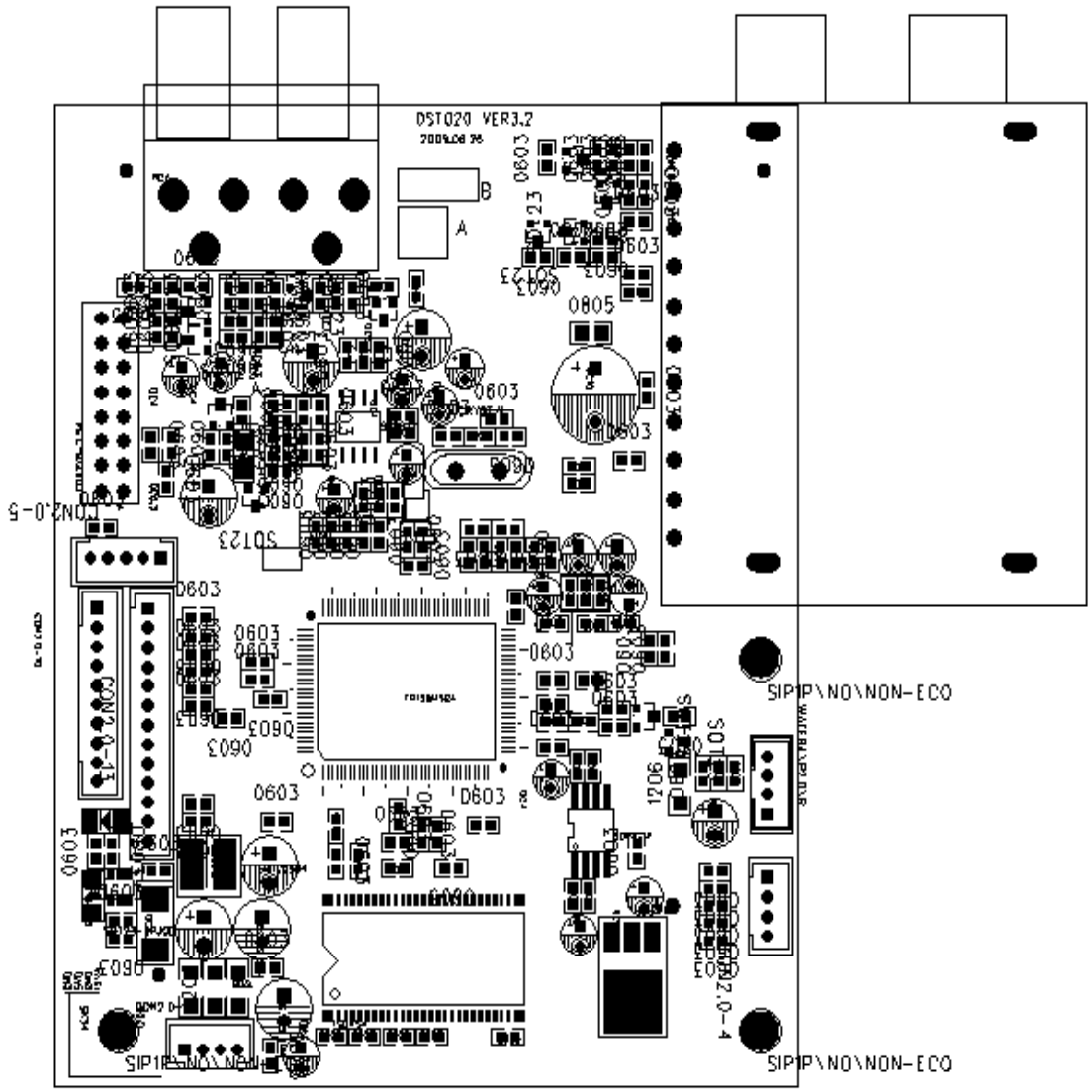


Printed Circuit Board

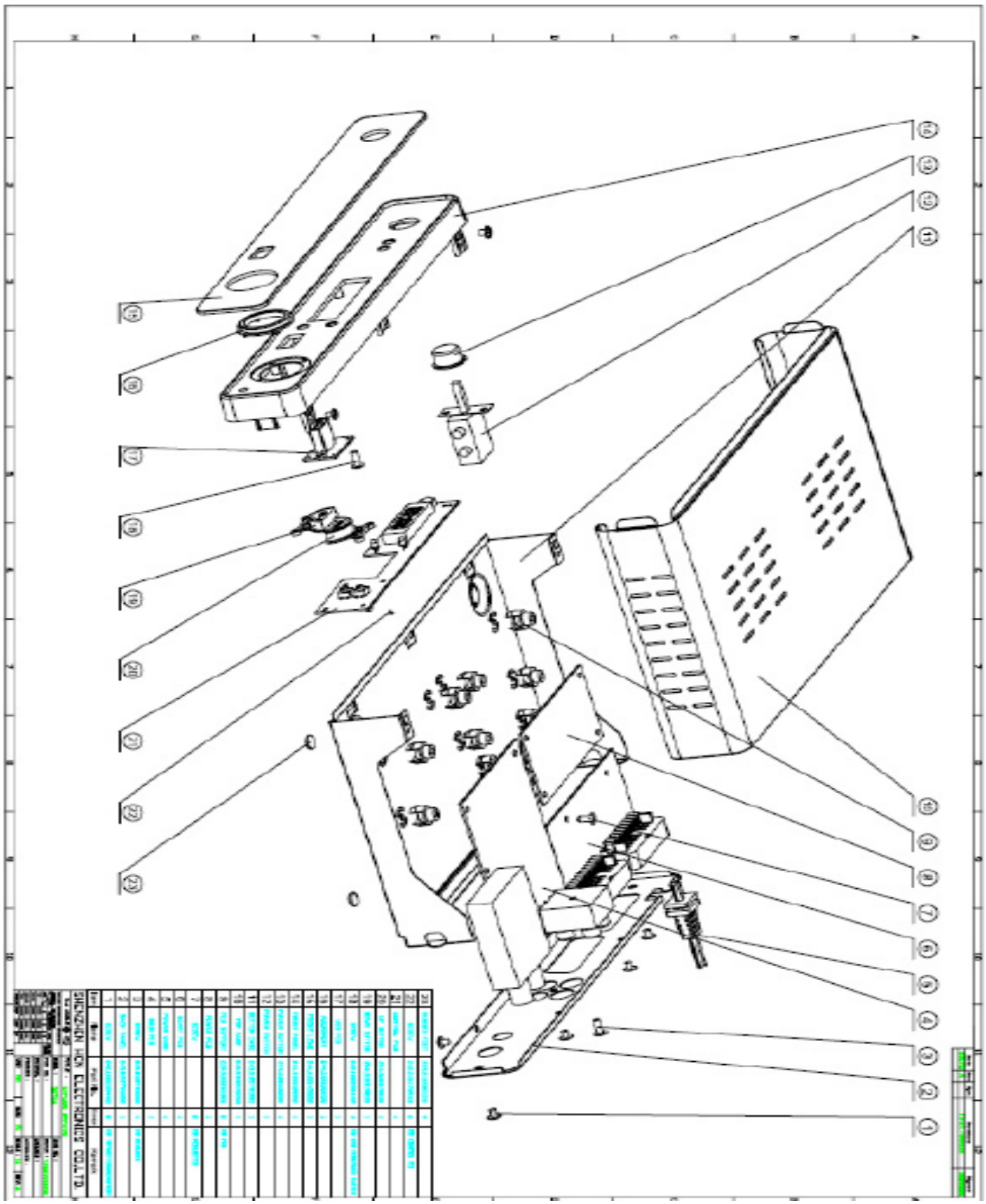
Scart board



Mainboard

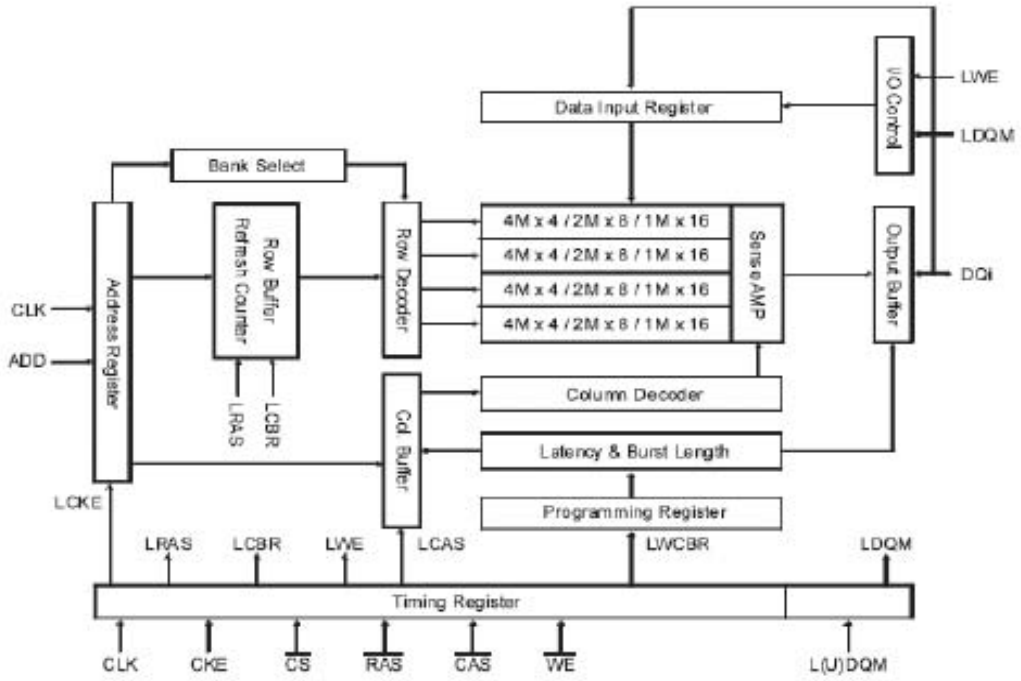


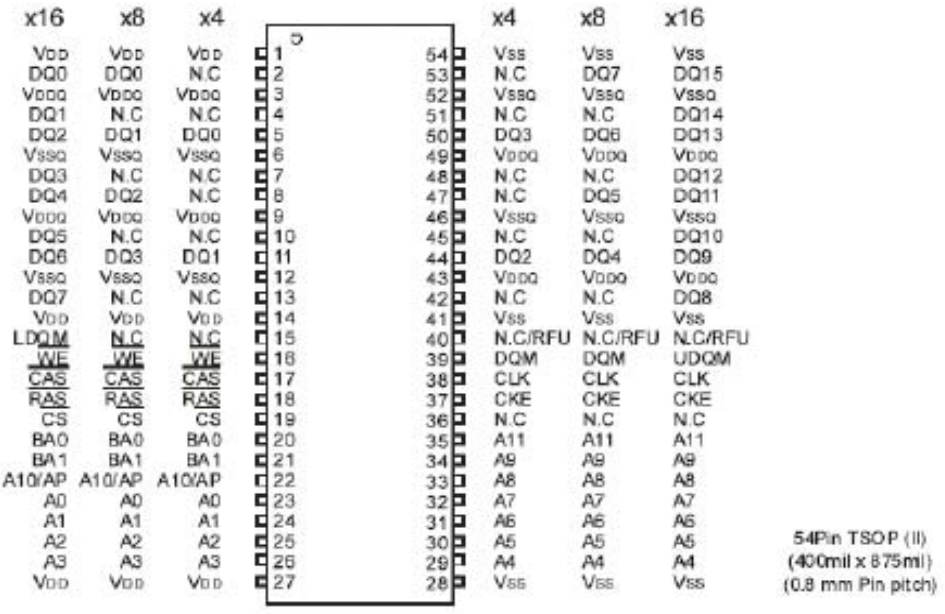
Explosive view



IC function description

IC K4S641632





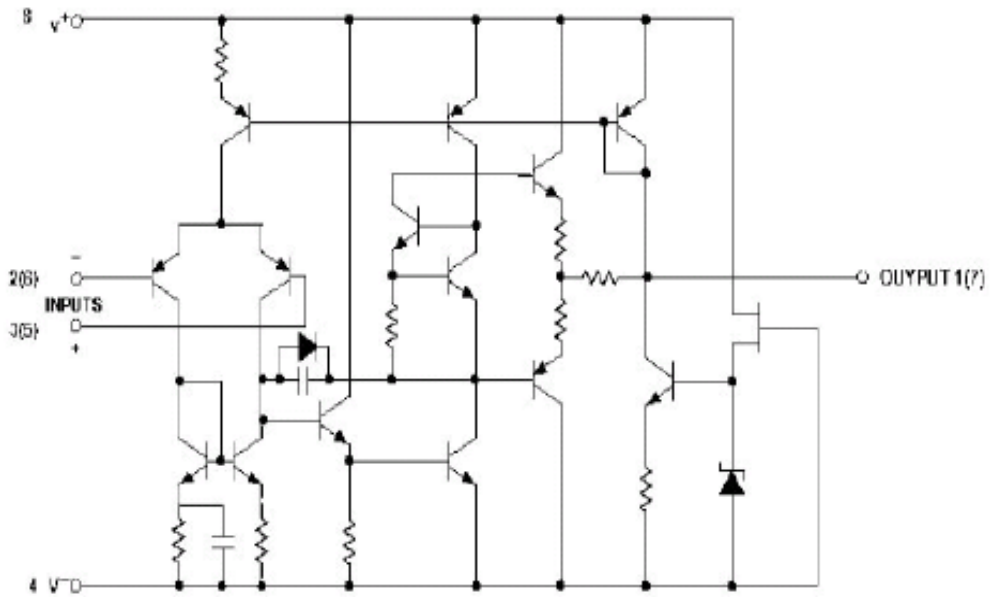
IC function description

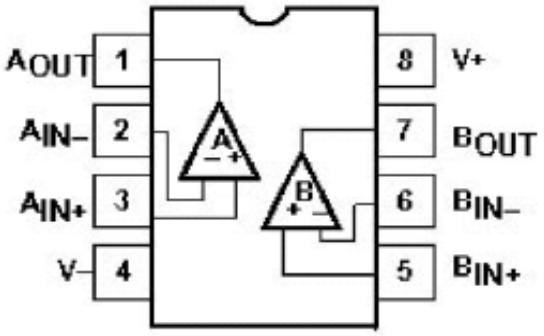
IC K4S641632

Pin	Name	Input function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{CS}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	Address	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, Column address : (x4 : CA_0 ~ CA_9, x8 : CA_0 ~ CA_9, x16 : CA_0 ~ CA_7)
BA_0 ~ BA_1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	Data input/output mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ_0 ~ x1 s	Data input/output	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/Vss	Power supply/ground	Power and ground for the input buffers and the core logic.
V_{DDQ}/Vssq	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

IC function description

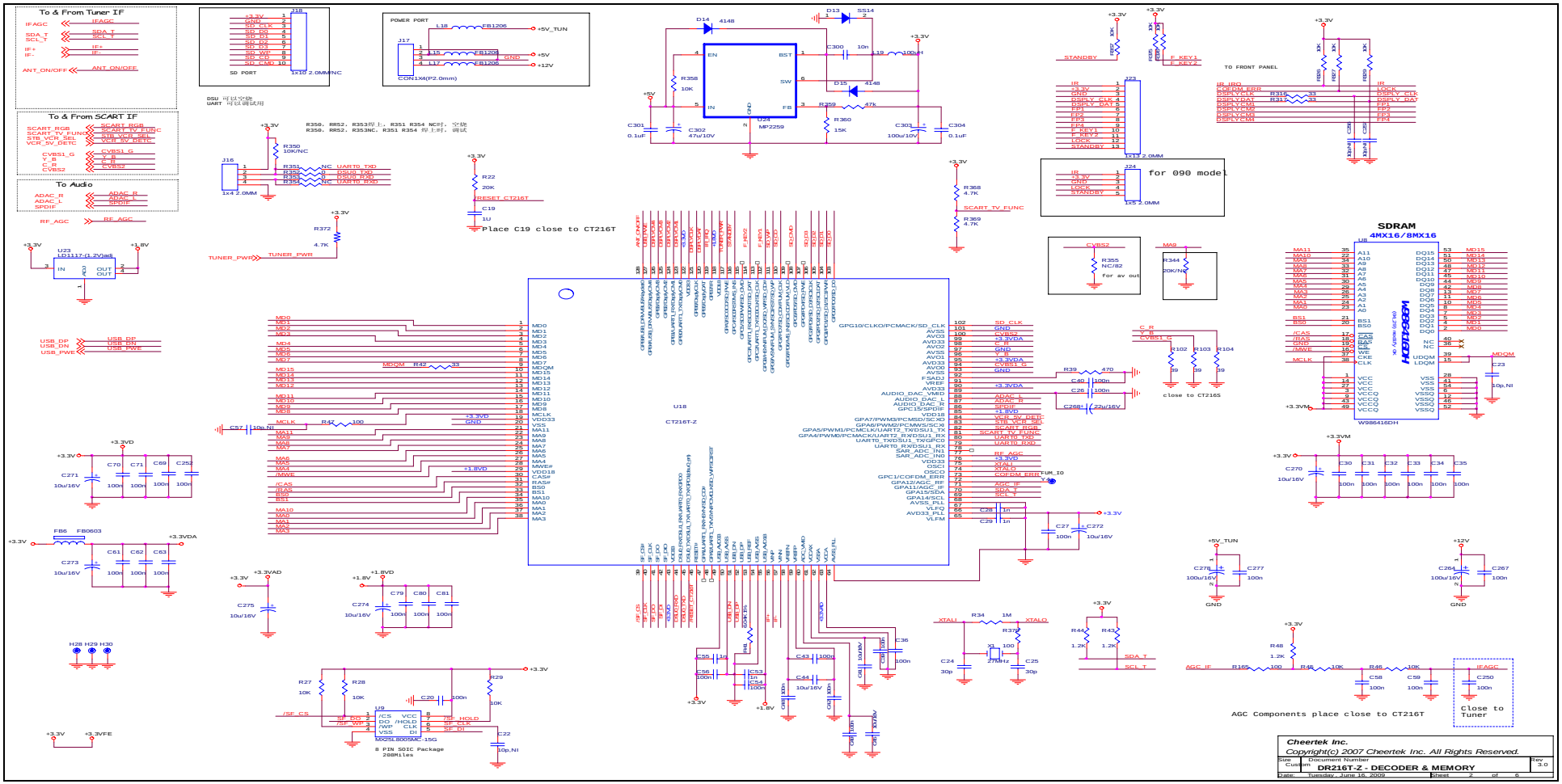
IC C4558



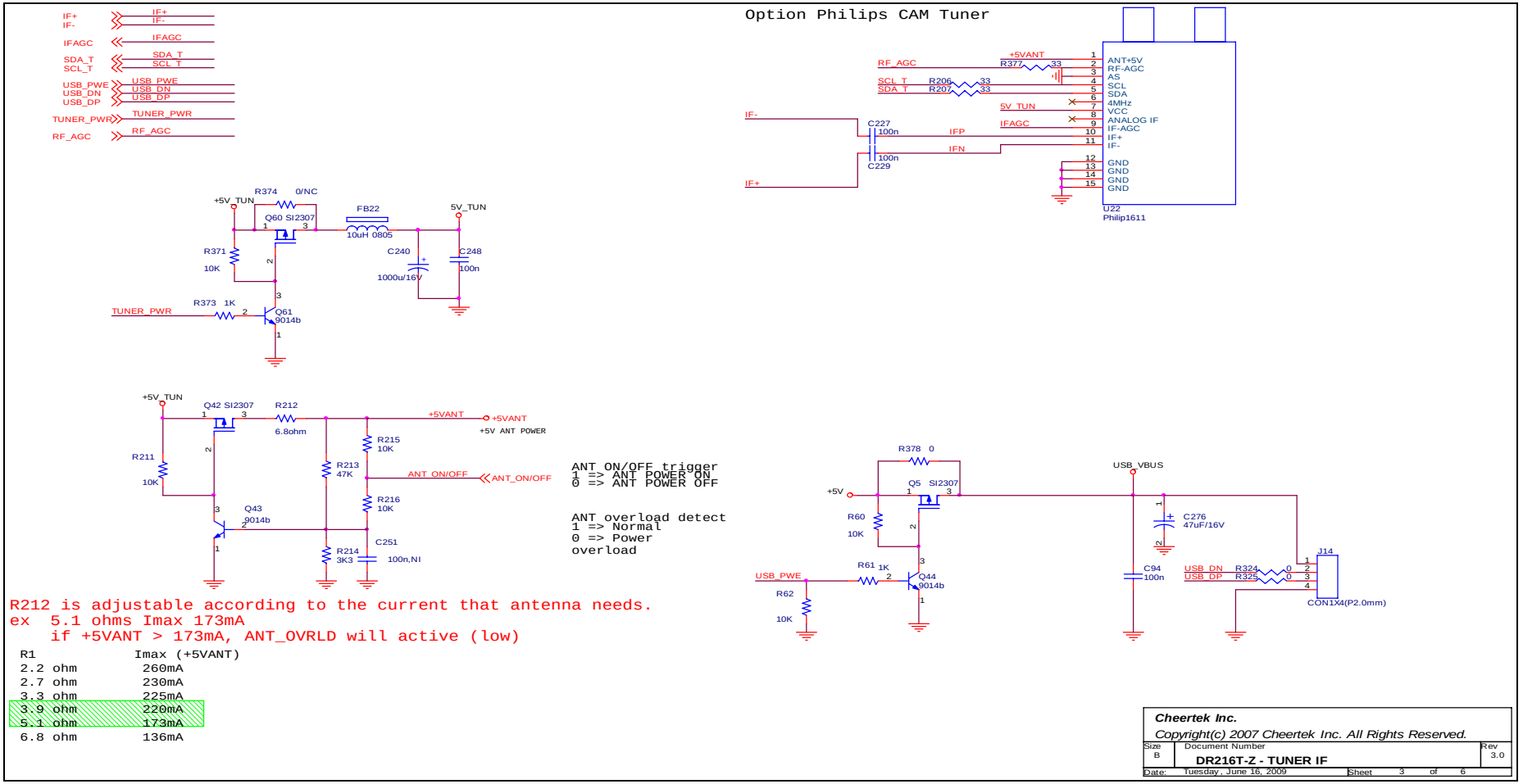


PIN	NAME	PIN	NAME
1.	AOUT	5.	BIN+
2.	AIN-	6.	BIN-
3.	AIN+	7.	BOUT
4.	V-	8.	V+

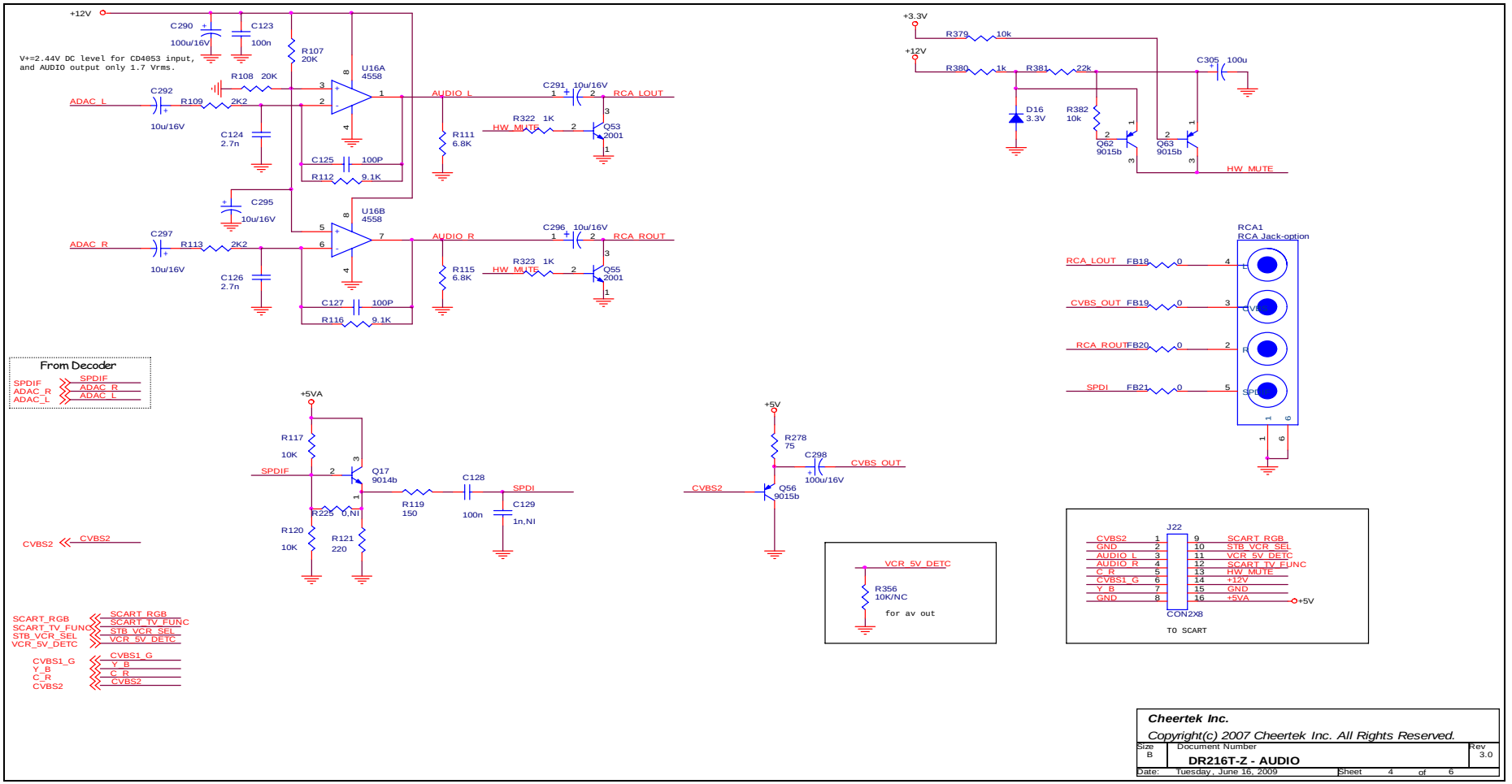
Schematics diagram



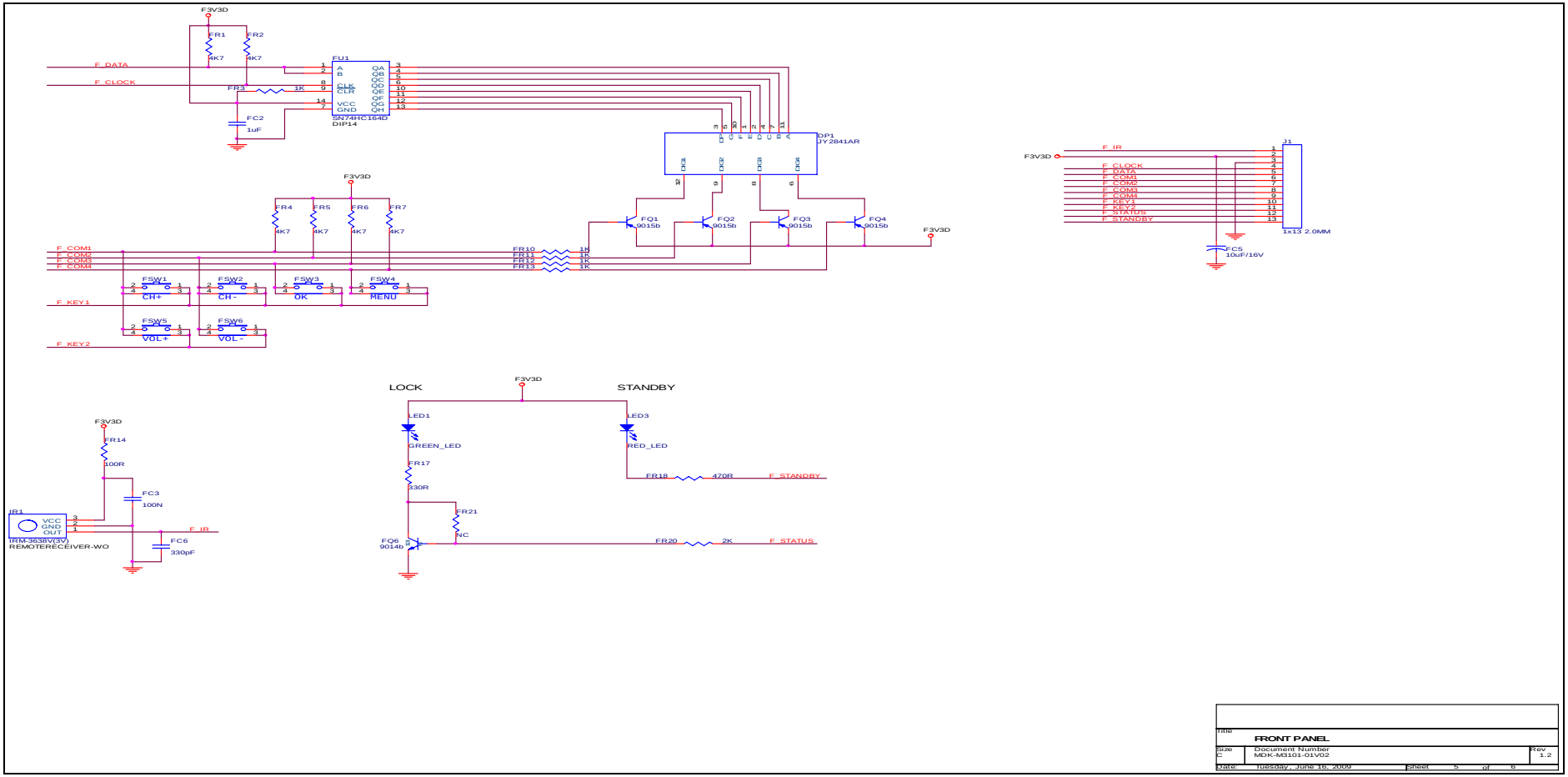
Schematics diagram



Schematics diagram



Schematics diagram



Title	FRONT PANEL	
Size: C	Document Number: MDK-M3101-01V02	Rev: 1.2
Date: Tuesday, June 16, 2009	Sheet 5 of 6	

Schematics diagram