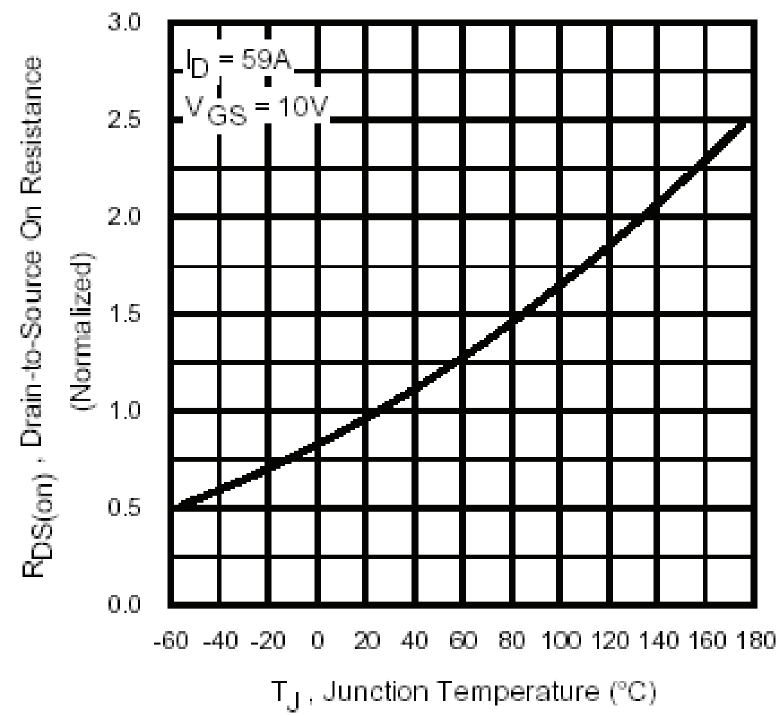
Key Parameters of MOSFETs (3)

- **Static Drain-to-Source On-Resistance, $R_{DS(ON)}$**

This is the drain-source resistance, typically specified on data sheet at 25°C with VGS = 10V.

$R_{DS(ON)}$ parameter is temperature-dependent, and is directly related to the MOSFET conduction losses. lower $R_{DS(ON)}$ results in lower conduction losses.



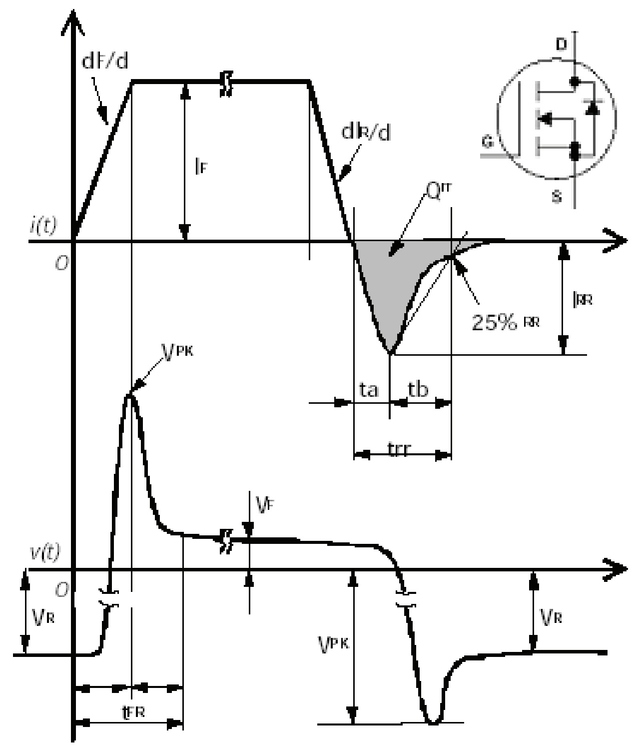
Normalized On-Resistance vs. Temperature

Key Parameters of MOSFETs (4)

- **Body Diode Reverse Recovery Characteristics, Q_{rr}, t_{rr}, I_{rr} and S factor.**

Power MOSFETs inherently have an integral reverse body-drain diode. This body diode exhibits reverse recovery characteristics. Reverse Recovery Charge Qrr, Reverse Recovery Time trr, Reverse Recovery Current Irr and Softness factor (S = tb/ta), are typically specified on data sheets at 25°C and di/dt = 100A/us.

Reverse recovery characteristics are temperature-dependent and lower trr, Irr and Qrr improves THD, EMI and Efficiency η.



Typical Voltage –Current Waveforms for a MOSFET Body Diode

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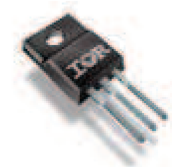
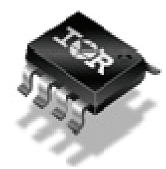
Key Parameters of MOSFETs (5)

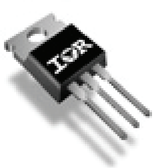
- **Package**

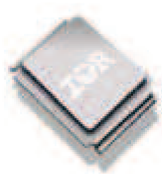
  MOSFET devices are available in several packages as SO-8,TO-220, D-Pak, I-Pak, TO-262, DirectFET™, etc.

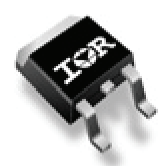
  The selection of a MOSFET package for a specific application depends on the package characteristics such as dimensions, power dissipation capability, current capability, internal inductance, internal resistance, electrical isolation and mounting process.











Choosing the MOSFET Voltage Rating for Class D applications (1)

- **MOSFET voltage rating for a Class D amplifier is determined by:**
  - **Desired P_{OUT} and load impedance (i.e. 250W on 4Ω)**
  - **Topology (Full Bridge or Half Bridge)**
  - **Modulation Factor M (80-90%)**

$$VB_{DSS\,min} = \sqrt{\frac{2 * P_{OUT} * R_{LOAD}}{M}} * 1.5$$

Typical additional factor due to stray resistance, power supply fluctuations and MOSFET Turn-Off peak voltage

Choosing the MOSFET Voltage Rating for Class D Applications (2)

- **Full-Bridge Topology Class D amplifier**

	BVDSS Minimum					Corresponding IR MosFET BVDSS				
	Load (Ohms)					Load (Ohms)				
Output Power (W)	1	2	4	6	8	1	2	4	6	8
100	25.0	35.3	49.9	61.1	70.6	30	40	55	75	75
150	30.6	43.2	61.1	74.9	86.5	40	55	75	75	100
200	35.3	49.9	70.6	86.5	99.8	40	55	75	100	100
500	55.8	78.9	111.6	136.7	157.8	75	100	150	150	200
1000	78.9	111.6	157.8	193.3	223.2	100	150	200	200	250

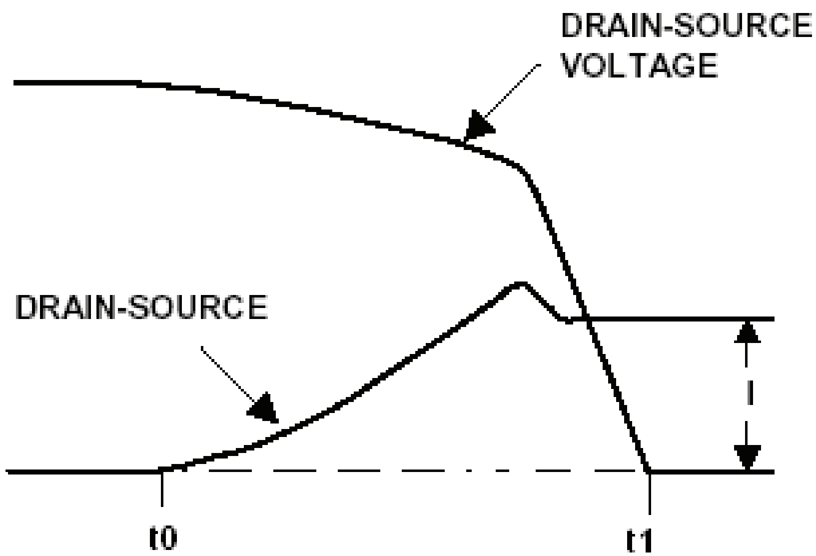
- **Half-Bridge Configuration Class D amplifier**

	VBDSS Minimum					Corresponding IR MosFET BVDSS				
	Load (Ohms)					Load (Ohms)				
Output Power (W)	1	2	4	6	8	1	2	4	6	8
100	49.9	70.6	99.8	122.3	141.2	55	75	100	150	150
150	61.1	86.5	122.3	149.7	172.9	75	100	150	150	200
200	70.6	99.8	141.2	172.9	199.7	75	100	150	200	200
500	111.6	157.8	223.2	273.4	315.7	150	200	250	300	400
1000	157.8	223.2	315.7	386.6	446.4	200	250	400	400	450

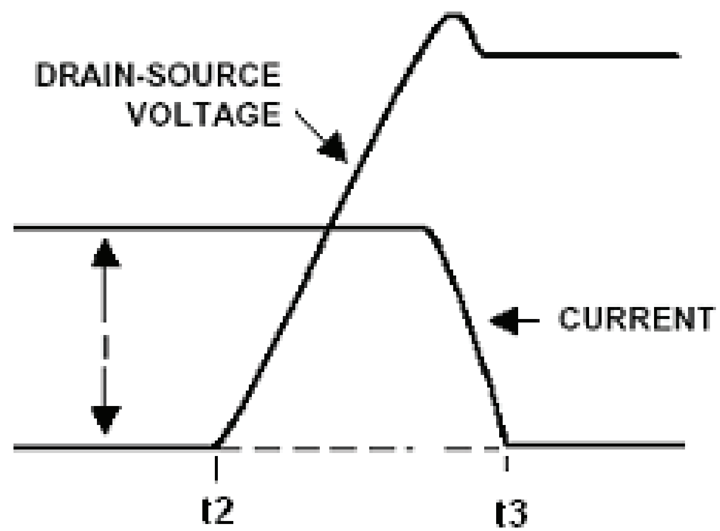
Note 1. Modulation Factor M = 85%

Calculation of Switching Loss (1)

- **Switching Losses are the result of turn-on and turn-off switching times**



MOSFET Turn-On



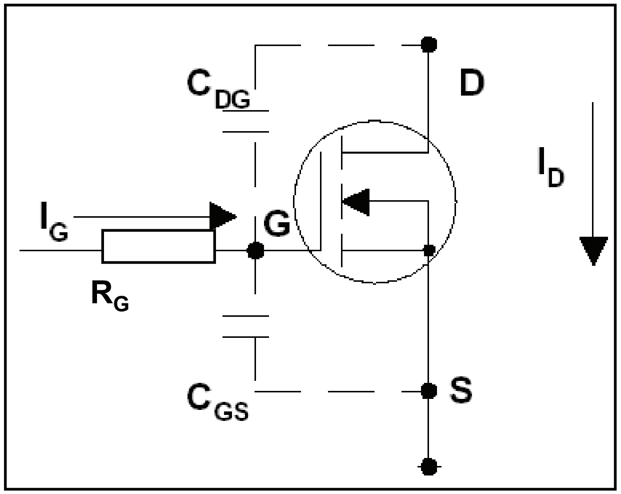
MOSFET Turn-Off

Calculation of Switching Loss (2)

- **Gate resistance Rg, and gate charge Qg, have a significant influence on turn-on and turn-off switching times**

$$\uparrow R_g \Rightarrow \downarrow I_g \Rightarrow \uparrow t_{SWITCHING} \Rightarrow \uparrow P_{SWITCHING}$$

$$\uparrow Q_g \Rightarrow \uparrow t_{SWITCHING} \Rightarrow \uparrow P_{SWITCHING}$$



Estimation of Switching Losses (1)

- **Switching losses can be obtained by calculating the switching energy dissipated in the MOSFET**

$$E_{sw} = \int_0^t V_{DS}(t) * I_D(t)\,dt$$

Where t is the length of the switching pulse.

- **Switching losses can be obtained by multiplying switching energy with switching frequency.**

$$P_{SWITCHING} = E_{SW} * F_{SW}$$

Estimation of Conduction Loss (2)

- **Conduction losses can be calculated using $R_{DS(ON)}$ @ Tj max and $I_{D\ RMS}$ current of MOSFET**

$$P_{CONDUCTION} = (I_{D\ RMS})^2 * R_{DS(ON)}$$

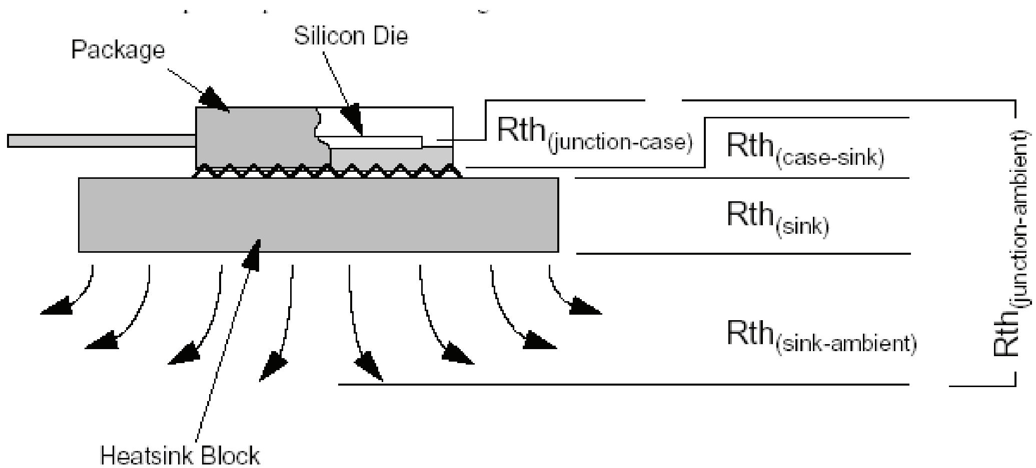
$I_{D\ RMS}$ is determined using amplifier specifications:

$$I_{D\ RMS} = \sqrt{\frac{P_{OUT}}{R_{LOAD}}}$$

$R_{DS(ON)}$ data can be obtained from the MOSFET data sheet.

Thermal Design

- **Maximum allowed power dissipation for a MOSFET mounted on a heat sink:**



$$P_{max} = \Delta Tj / R_{thja\ max}$$

$$P_{max} = (T_{amb} - Tj_{max}) / (R_{thjc\ max} + R_{thcs\ max} + R_{ths\ max} + R_{thsa\ max})$$

Where: T_{amb} = Ambient Temperature

Tj_{max} = Max. Junction Temperature

$R_{thjc\ max}$ = Max. Thermal Resistance Junction to Case

$R_{thcs\ max}$ = Max. Thermal Resistance Case to Heatsink

$R_{ths\ max}$ = Max. Thermal Resistance of Heatsink

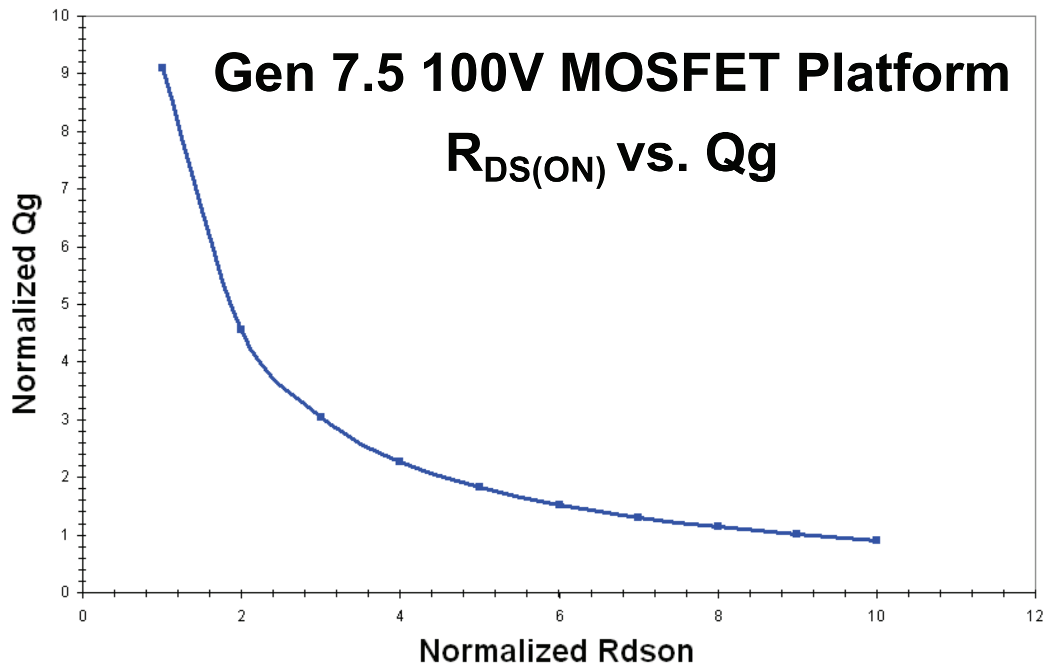
$R_{thsa\ max}$ = Max. Thermal Resistance Heatsink to Ambient

$R_{DS(ON)}$ vs Qg

- **There is tradeoff between Static Drain-to-Source On-Resistance, $R_{DS(ON)}$ and Gate charge, Qg**

Higher $R_{DS(ON)}$ ⇒ Lower Qg ⇒ Higher $P_{CONDUCTION}$ & Lower $P_{SWITCHING}$

Lower $R_{DS(ON)}$ ⇒ Higher Qg ⇒ Higher $P_{SWITCHING}$ & Lower $P_{CONDUCTION}$



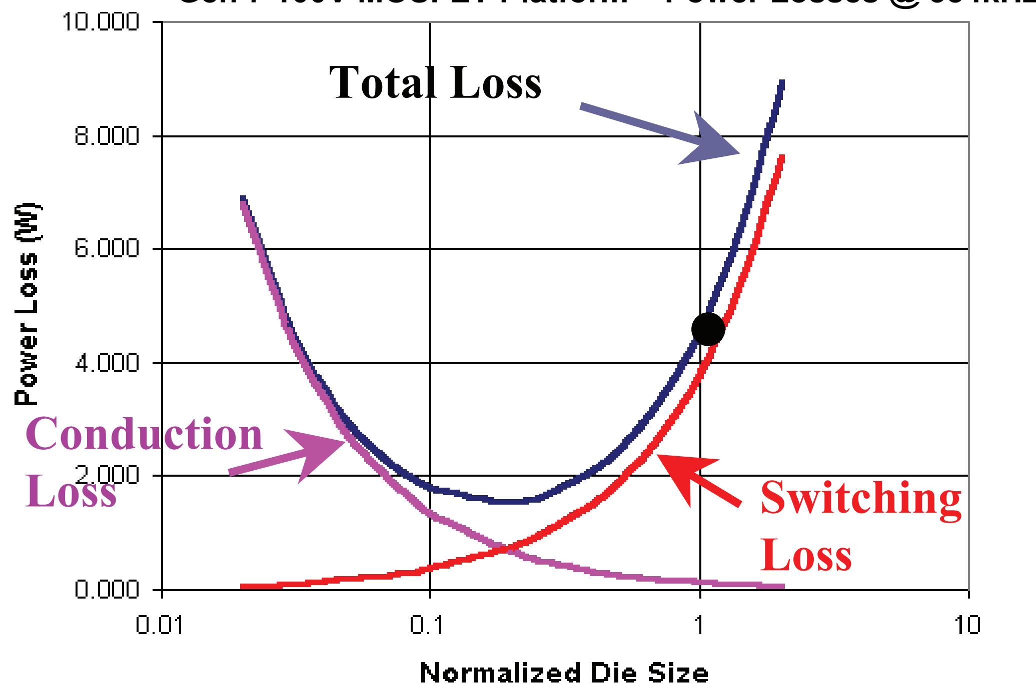
Die Size vs Power Loss (1)

- **Die size has a significant influence on MOSFET power losses**

Smaller Die ⇒ Higher $P_{CONDUCTION}$ & Lower $P_{SWITCHING}$

Bigger Die ⇒ Higher $P_{SWITCHING}$ & Lower $P_{CONDUCTION}$

Gen 7 100V MOSFET Platform – Power Losses @ 384kHz

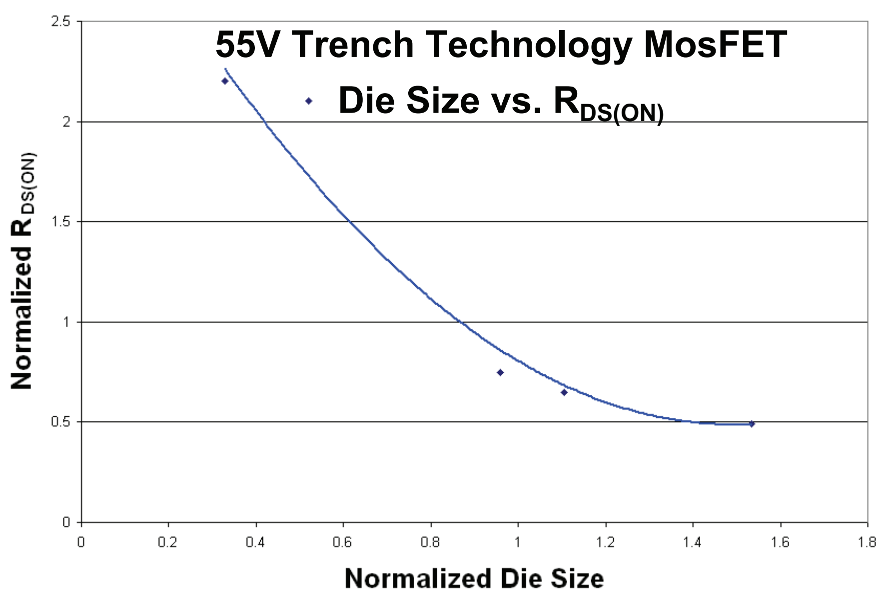


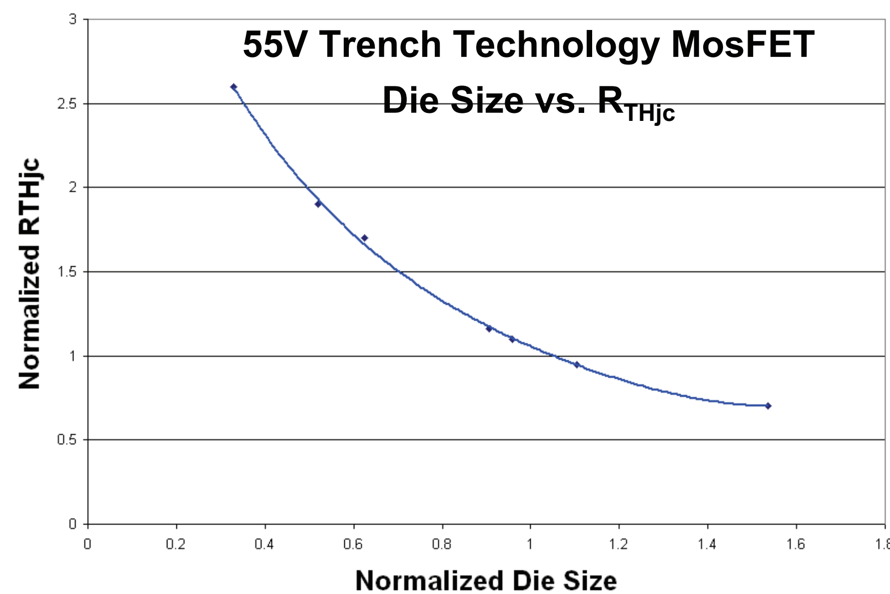
Die Size vs Power Loss (2)

- **Die size is directly related with $R_{DS(ON)}$ and R_{THjc} of the MOSFET**

Smaller Die ⇒ Higher $R_{DS(ON)}$ and Higher R_{THjc}

Bigger Die ⇒ Lower $R_{DS(ON)}$ and Lower R_{THjc}





Choosing the Right MOSFET for Class D Applications (1)

- **The criteria to select the right MOSFET for a Class D amplifier application are:**
  - VB_{DSS} should be selected according to amplifier operating voltage, and it should be large enough to avoid avalanche condition during operation
  - Efficiency η is related to static drain-to-source on-resistance, $R_{DS(ON)}$. smaller $R_{DS(ON)}$ improves efficiency η. $R_{DS(ON)}$ is recommended to be smaller than 200mΩ for mid and high-end power, full-bandwidth amplifiers
  - Low gate charge, Qg, improves THD and efficiency η. Qg is recommended to be smaller than 20nC for mid and high-end power, full-bandwidth amplifiers

Choosing the Right MOSFET for Class D Application (2)

- Amplifier performance such as THD, EMI and efficiency η are also related to MOSFET reverse recovery characteristics. Lower trr, Irr and Qrr improves THD, EMI and efficiency η
- Rthjc should be small enough to dissipate MOSFET power losses and keep Tj < limit
- Better reliability and lower cost are achieved with higher MOSFET Tj max
- Finally, selection of device package determines the dimensions, electrical isolation and mounting process. These factors should be considered in package selection. Because cost, size and amplifier performance depend on it.

Development of Class D Dedicated Devices

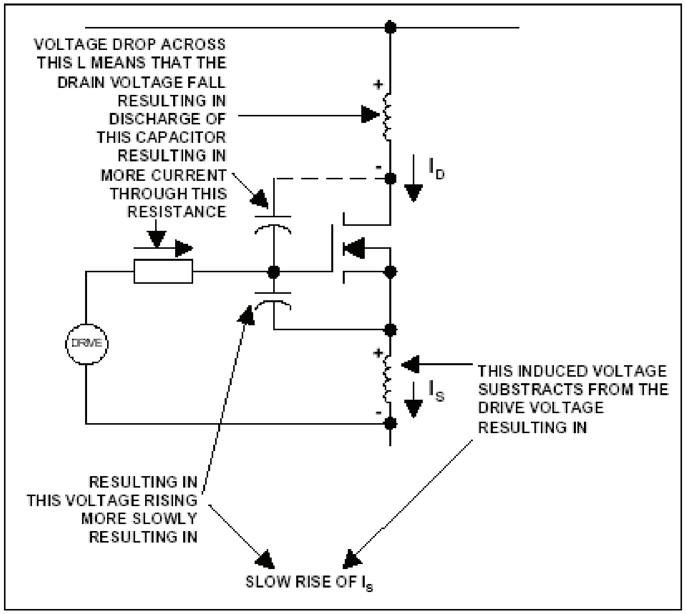
- **Performance of the Class D amplifying stage strongly depends on the characteristics of MOSFETs and ICs.**
- **Designers of driver IC and MOSFET silicon need to keep the special requirements of the Class D application in mind.**

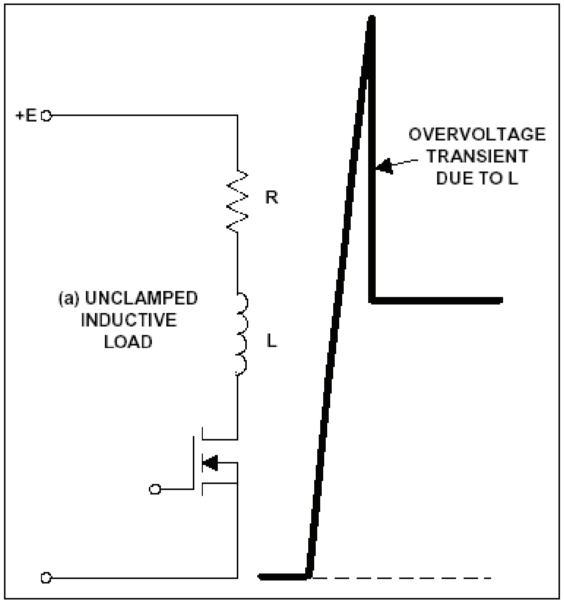
Influences of Stray Inductance

- **PCB layout and the MOSFET internal package inductances contribute to the stray inductance (L_S) in the circuit.**

- **Stray inductances affect the MOSFET performance and EMI of the system.**

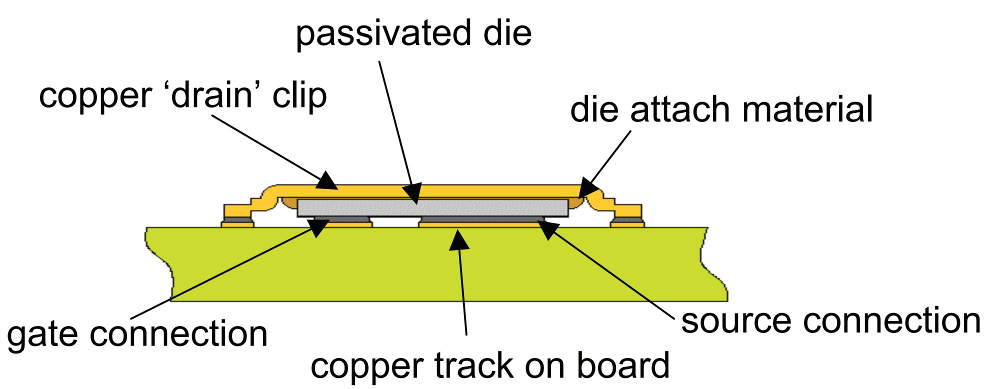
Influences of Stray Inductance

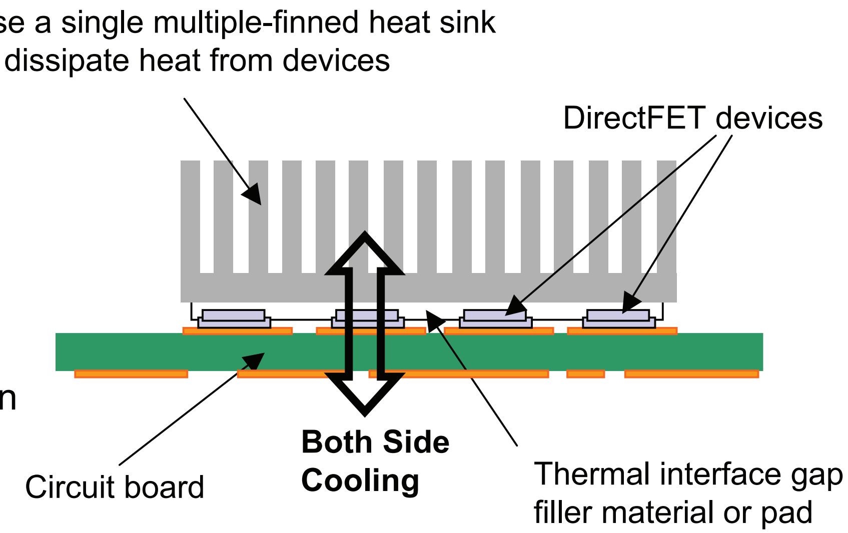


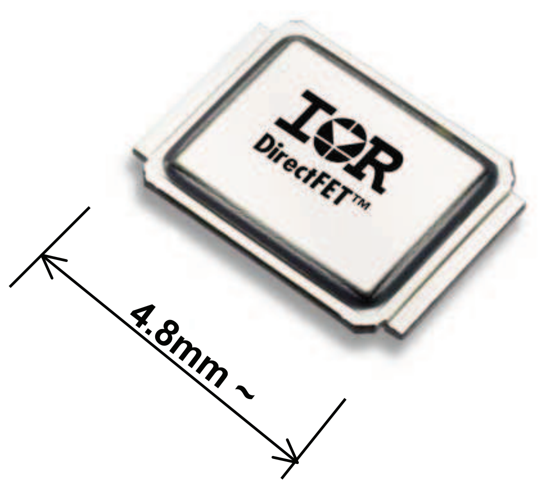


- Drain and source stray inductances reduces the gate voltage during turn-on resulting in longer switching time.
- Also during turn-off, drain and source stray inductances generate a large voltage drop due to dI_D/dt, producing drain to source over-voltage transients.

DirectFET™ Packaging



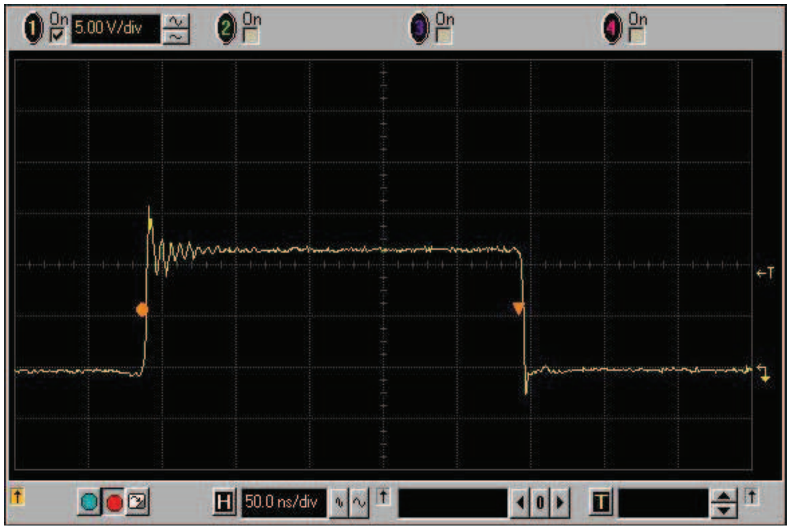




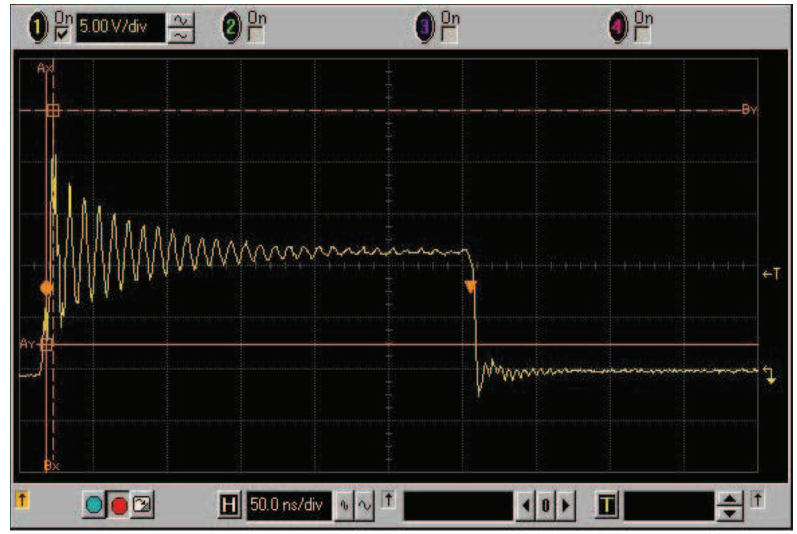
- Remove wirebonds from package and replace with large area solder contacts
- Reduced package inductance and resistance
- Copper can enables dual sided cooling

DirectFET™ Packaging

DirectFET waveform



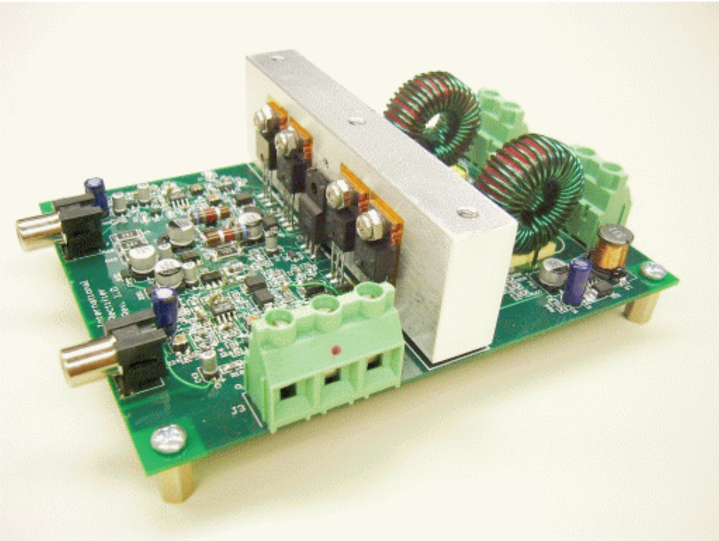
SO-8 waveform



- 30A VRM output current
- 500 kHz per phase
- Silicon of the near identical active area, voltage and generation used in both packages
- Inductance related ringing greater in case of SO-8

Class D Amp Reference Design

- **Specs**



Topology: Half Bridge

IR Devices: IR2011S, IRFB23N15D

Switching frequency: 400kHz (Adjustable)

Rated Output Power: 200W+200W / 4 ohm

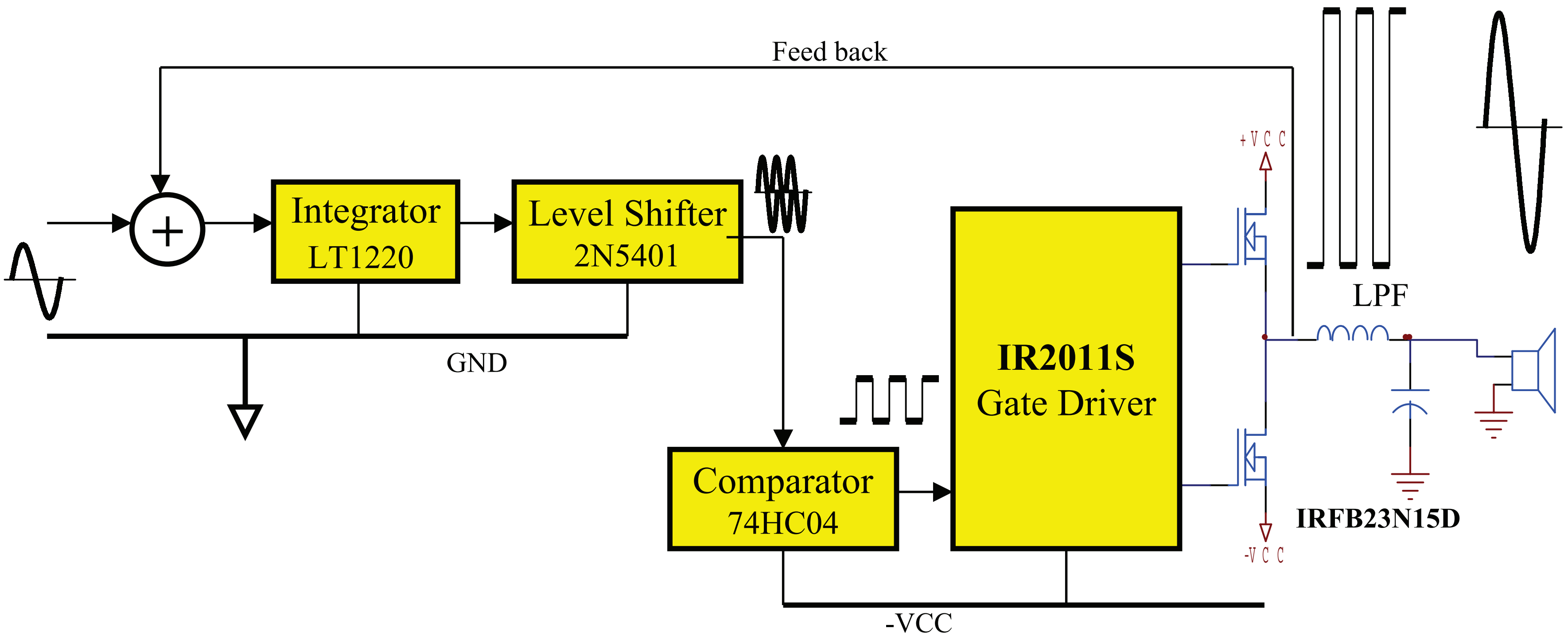
THD: 0.03% @1kHz, Half Power

Frequency Response: 5Hz to 40kHz (-3dB)

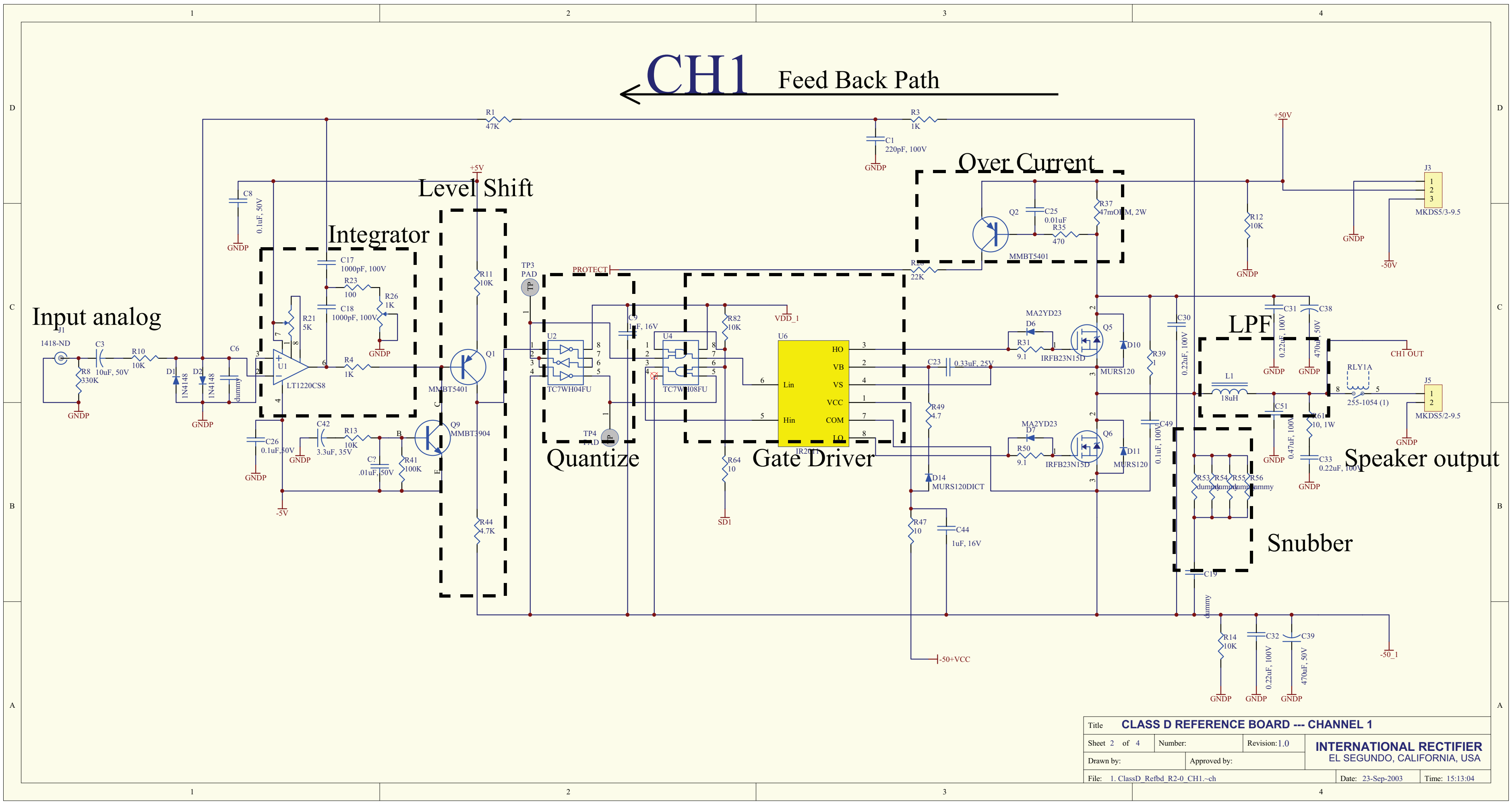
Power Supply: ~ ±50V

Size: 4.0” x 5.5”

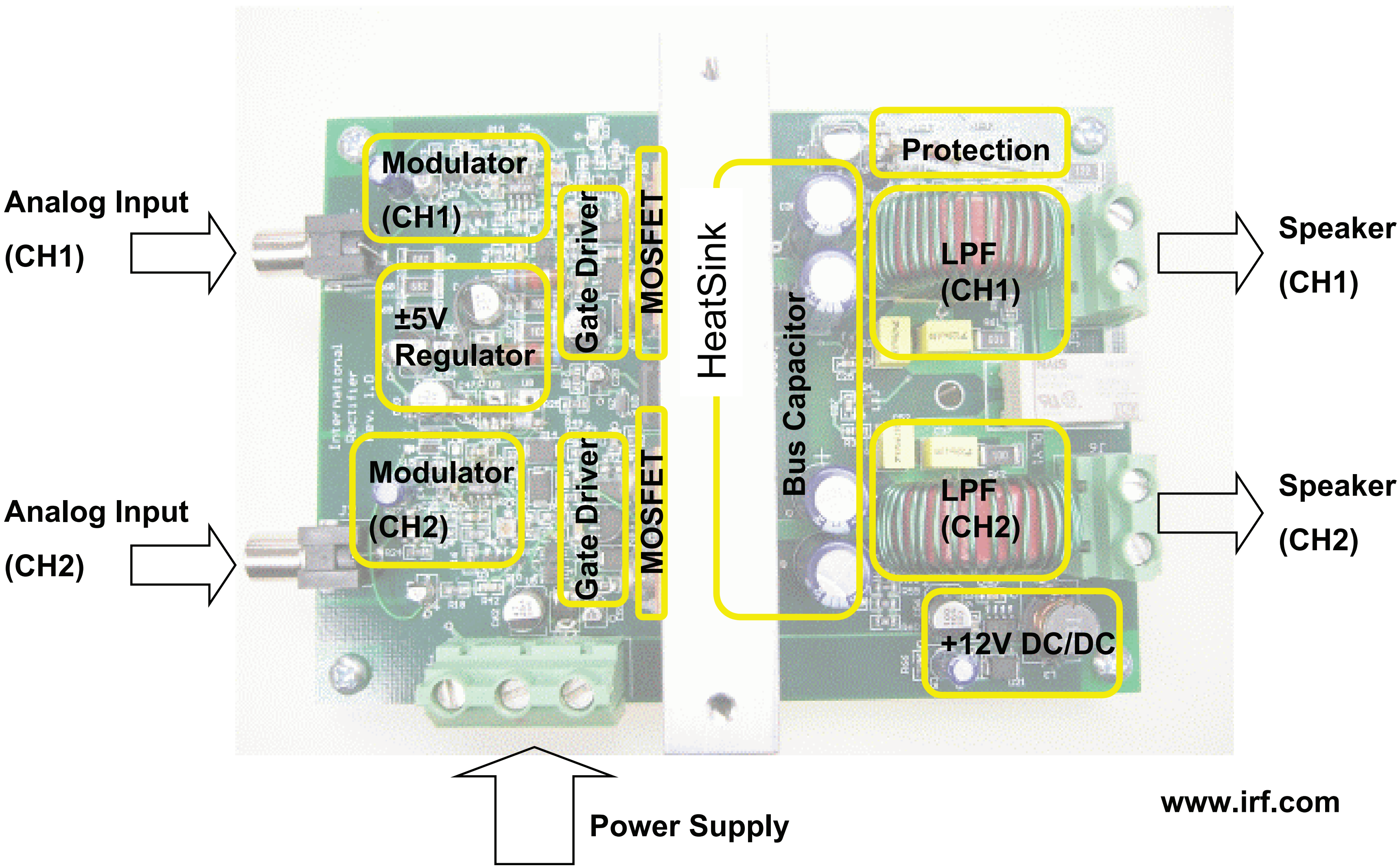
Class D Amp Reference Board: Block Diagram



Circuit Diagram

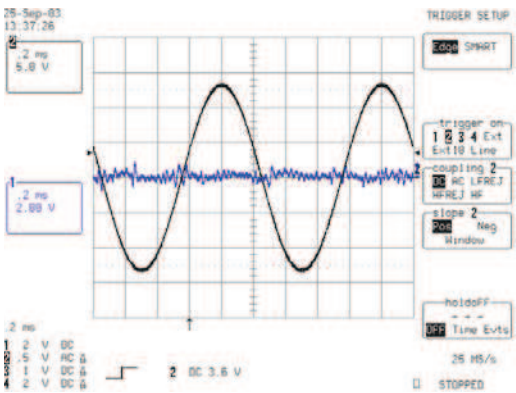


Class D Amp Reference Board: Layout

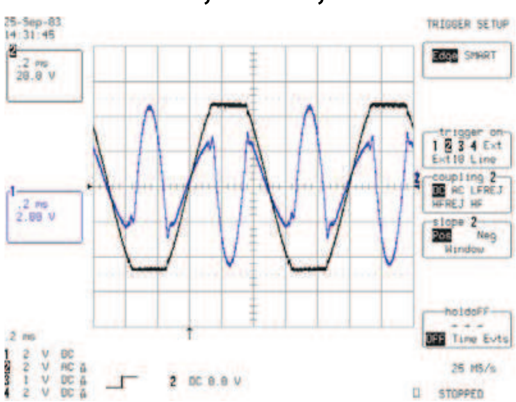


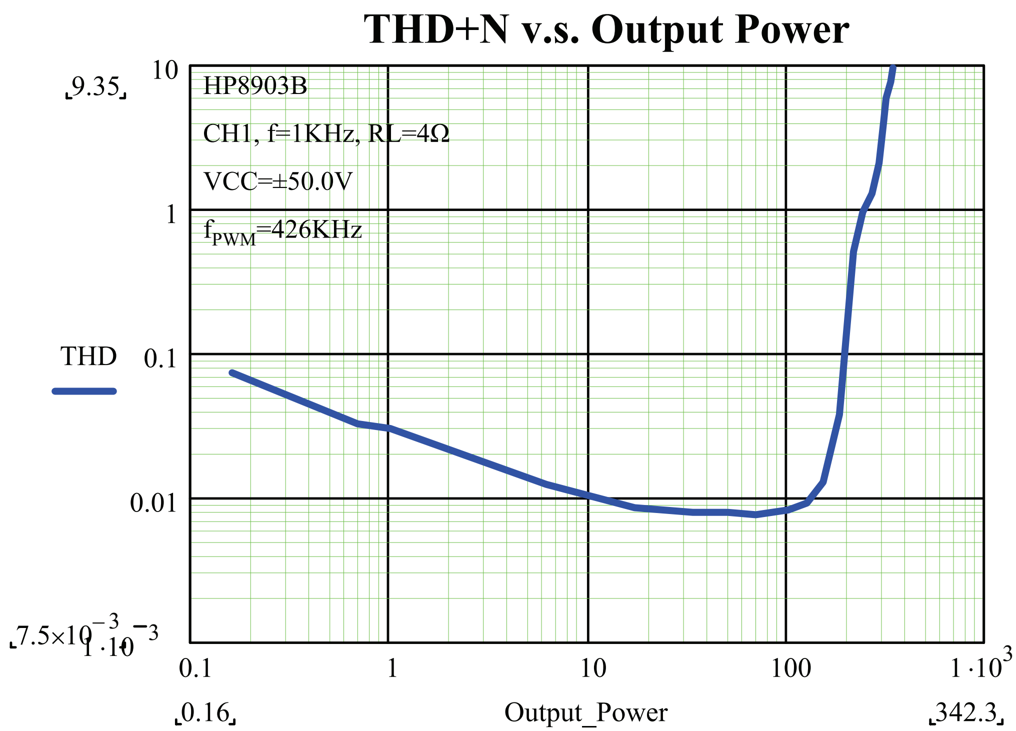
Performance

50W / 4Ω, 1KHz, THD+N=0.0078%



342W / 4Ω, 1KHz, THD+N=10%





- **Peak Output Power (f=1KHz)**
  - **120W / 8Ω / ch, THD=1%**
  - **180W / 8Ω / ch, THD=10%**
  - **245W / 4Ω / ch, THD=1%**
  - **344W / 4Ω / ch, THD=10%**

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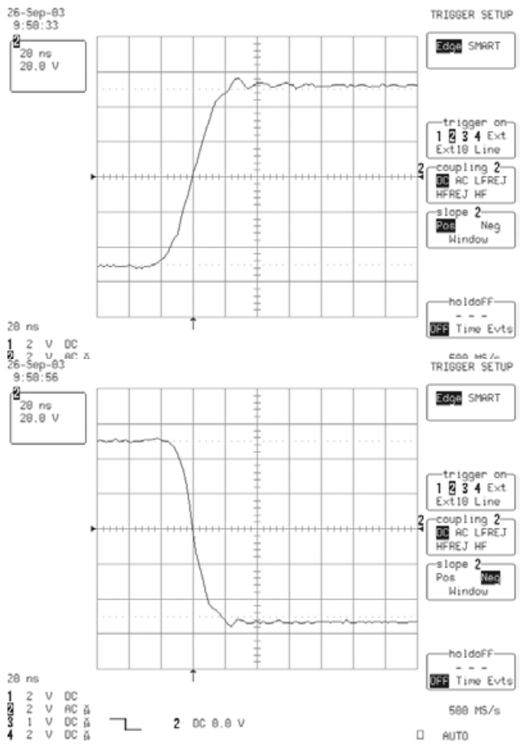
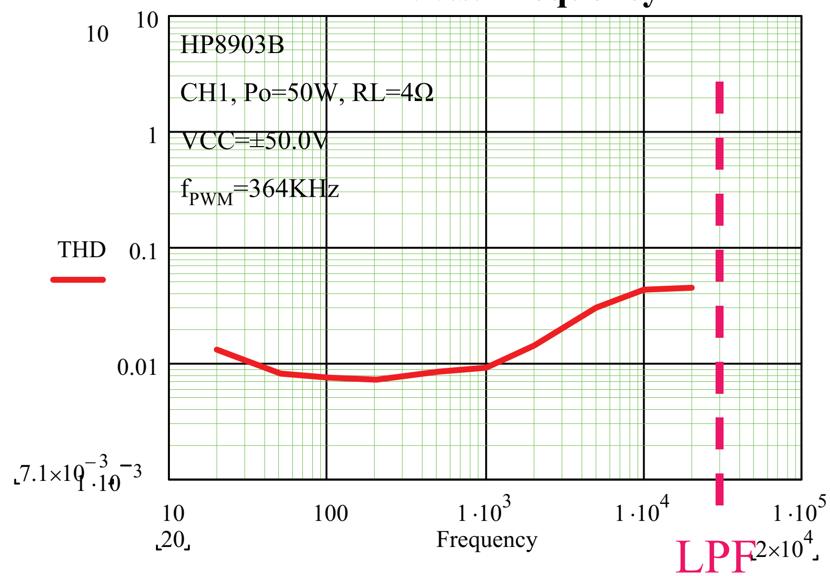
Performance (Cont'd)

Switching waveform



THD+N v.s. Frequency



Residual Noise: 62.5µVrms, A-Weighted, 30KHz-LPF

Conclusion

- Highly efficient Class D amplifiers now provide similar performance to conventional Class AB amplifiers -

  If key components are carefully selected and the layout takes into account the subtle, yet significant impact due to parasitic components.

Constant innovation in semiconductor technologies helps the growing Class D amplifiers usage due to improvements in higher efficiency, increased power density and better audio performance.