International Rectifier CLASS D AUDIO

Class D Audio Amplifier Design

- **Class D Amplifier Introduction**
  Theory of Class D operation, topology comparison
- **Gate Driver**
  How to drive the gate, key parameters in gate drive stage
- **MOSFET**
  How to choose, tradeoff relationships, loss calculation
- **Package**
  Importance of layout and package, new packaging technology
- **Design Example**
  200W+200W stereo Class D amplifier

www.irf.com

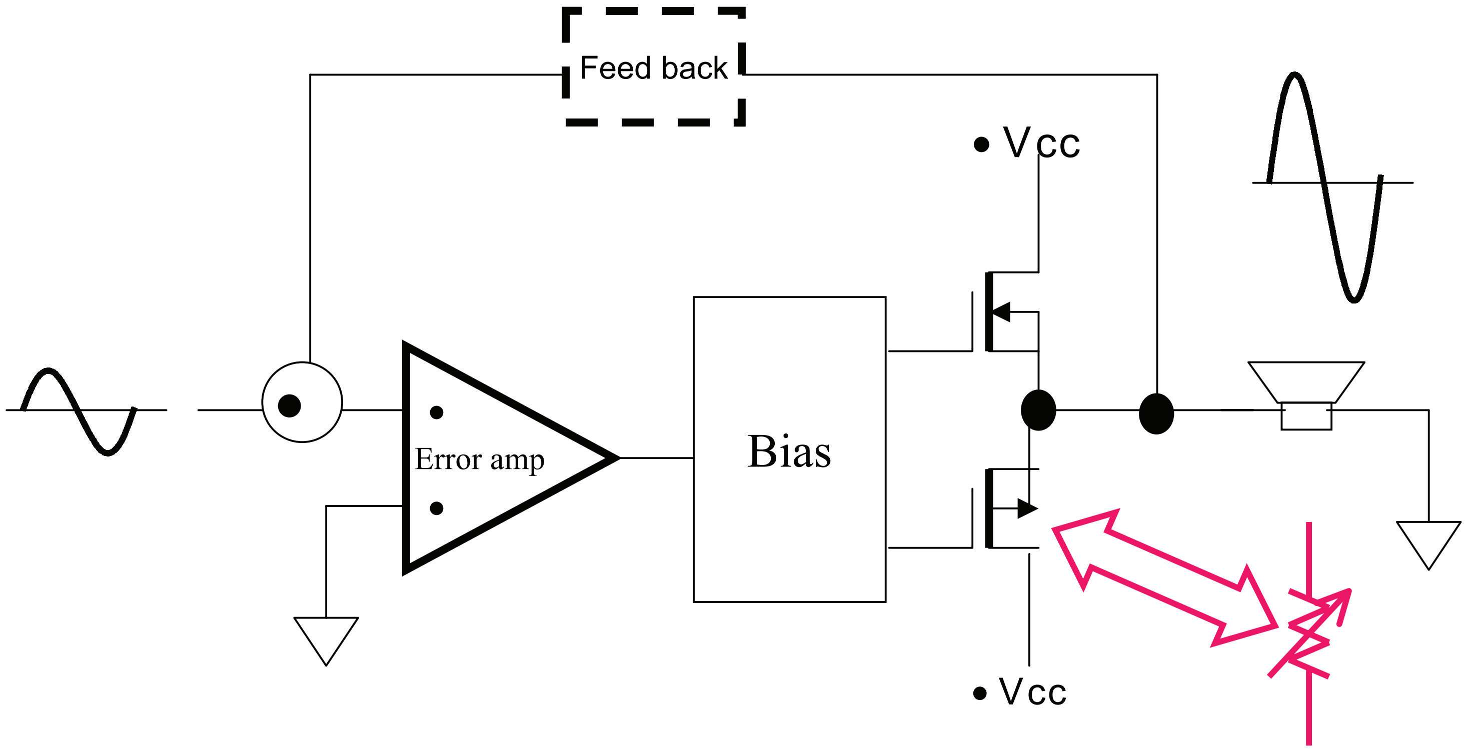
Prepared Oct.8 2003 by Jun Honda and Jorge Cerezo

Trend in Class D Amplifiers

- **Make it smaller!**
  - **- higher efficiency**
  - **- smaller package**
  - **- Half Bridge**

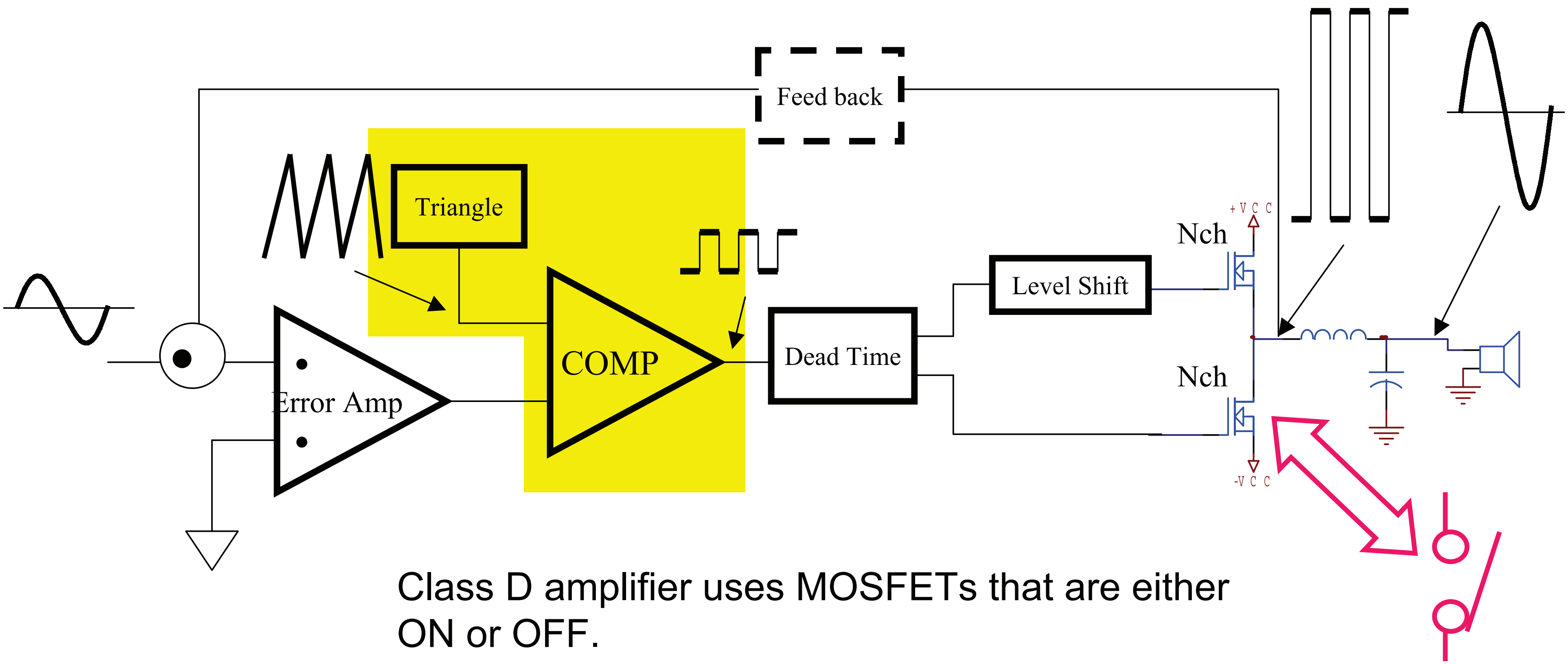
- **Make it sound better!**
  - **- THD improvement**
  - **- fully digitally processed modulator**

Traditional Linear Amplifier



Class AB amplifier uses linear regulating transistors to modulate output voltage. η = 30% at temp rise test condition.

How a Class D Amplifier Works

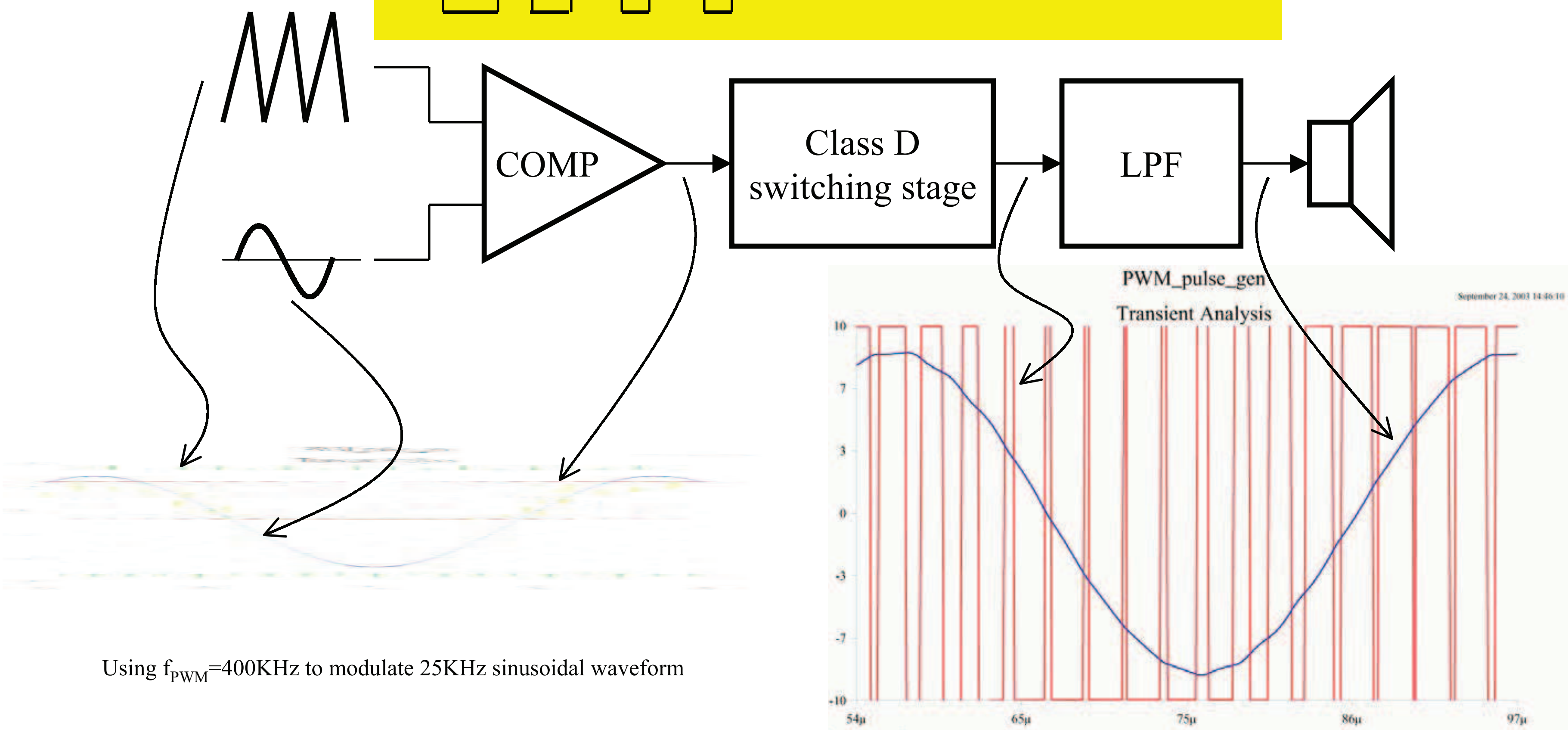


Class D amplifier uses MOSFETs that are either ON or OFF.

PWM technique is used to express analog audio signals with ON or OFF states in output devices.

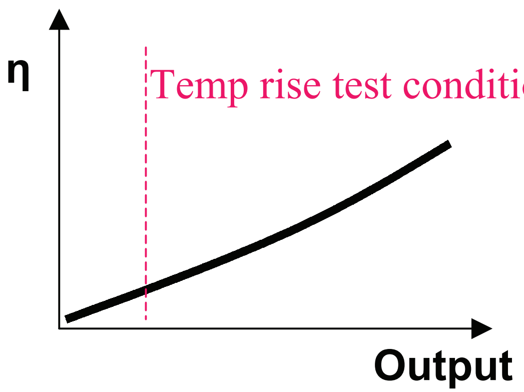
Basic PWM Operation

The output signal of comparator goes high when the sine wave is higher than the sawtooth.

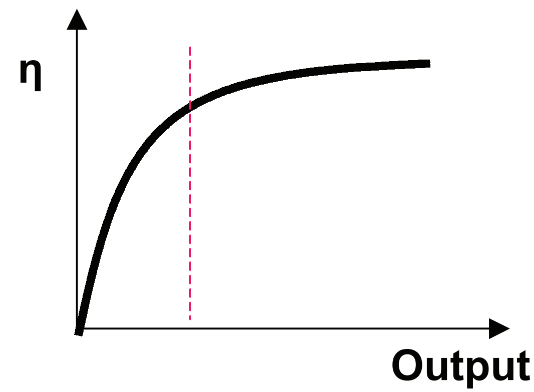


Using f_{PWM}=400KHz to modulate 25KHz sinusoidal waveform

Topology Comparison: Class AB vs Class D



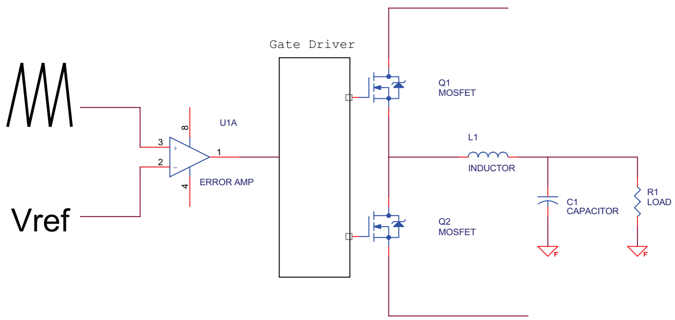
← Efficiency →



Class AB		Class D
Constant over Vbus	Gain	Proportional to Vbus
Good	PSRR	0 dB
Always from supply to load	Direction of energy flow	Both way Creates Vbus pumping phenomena

Analogy to Buck DC-DC Converter

Buck Converter



Load Current Direction

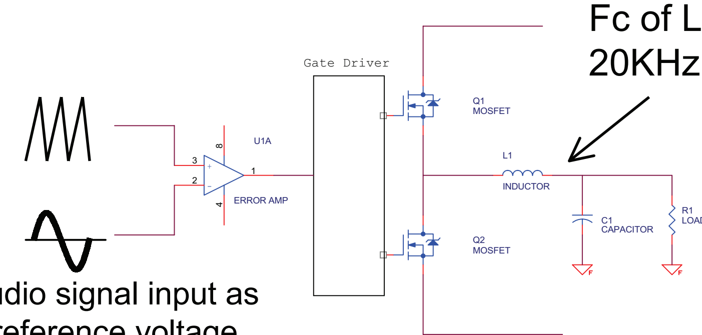
Duty ratio is fixed

➔Independent optimization for HS/LS

➔Low $R_{DS(ON)}$ for longer duty, low Qg for shorter duty

Class D Amplifier

Fc of LPF is above 20KHz



Audio signal input as a reference voltage

Both current directions

➔ Influence of dead time is different

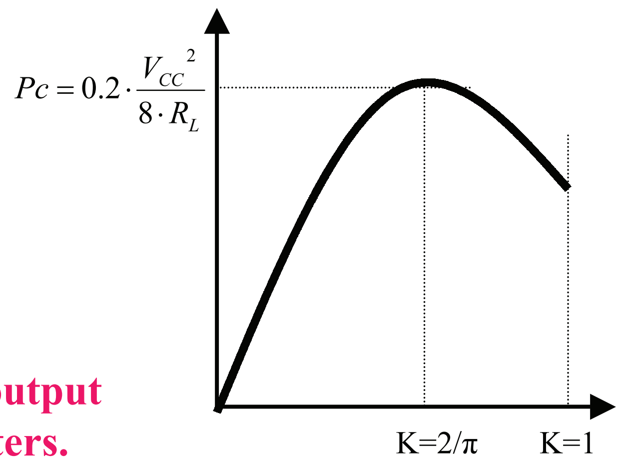
➔ Dead time needs to be very tight

Duty varies but average is 50%

➔Same optimization for both MOSFETs

➔Same $R_{DS(ON)}$ required for both sides

Loss in Power Device

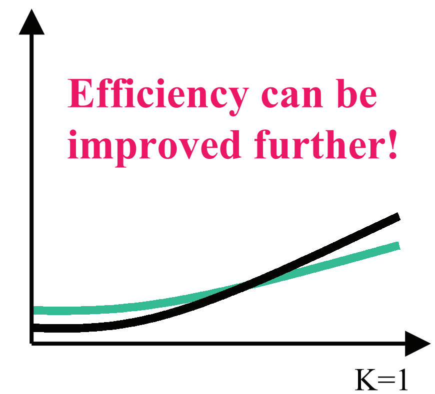


Loss in class AB

$$P_C = \frac{1}{2\cdot\pi} \cdot \int_0^{\pi} \frac{Vcc}{2}(1 - K\sin\omega\cdot t)\frac{Vcc}{2\cdot R_L} K\sin\omega\cdot t \bullet d\omega\cdot t$$

$$= \frac{Vcc^2}{8\pi\cdot R_L}\cdot\left(\frac{2K}{\pi} - \frac{K^2}{2}\right)$$

Regardless of output device parameters.



Loss in Class D

$$P_{TOTAL} = Psw + Pcond + Pgd$$

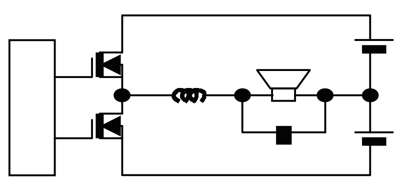
$$Pcond = \frac{R_{DS(ON)}}{R_L}\cdot Po \qquad Pgd = 2\cdot Qg\cdot Vgs\cdot f_{PWM}$$

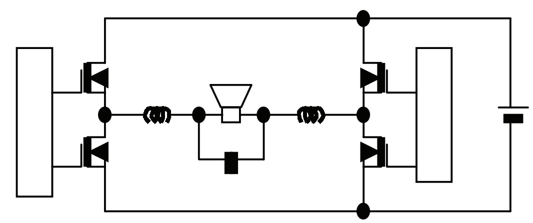
$$Psw = C_{OSS}\cdot V_{BUS}^{\ 2}\cdot f_{PWM} + I_D\cdot V_{DS}\cdot t_f\cdot f_{PWM}$$

K is a ratio of Vbus and output voltage.

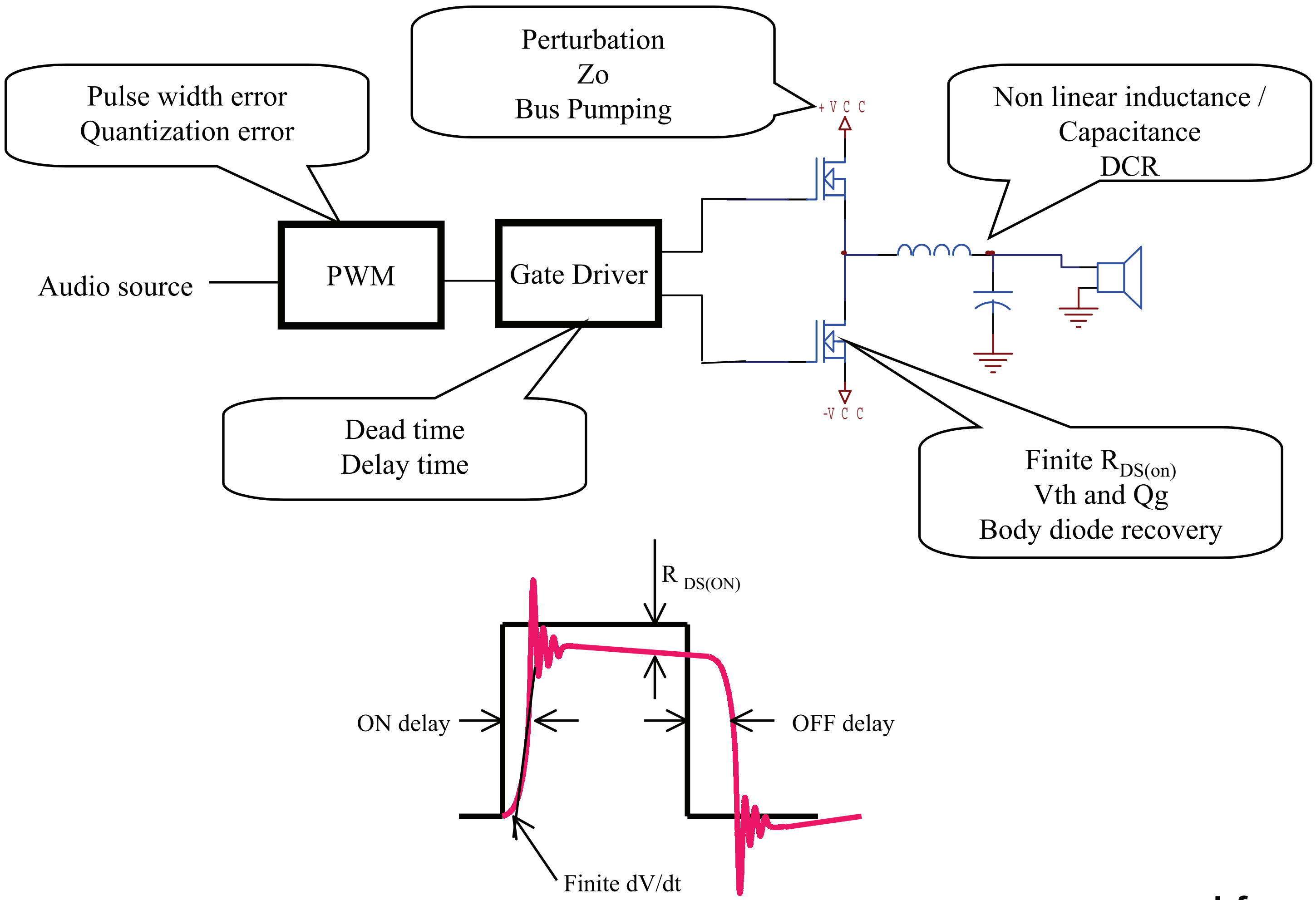
Half Bridge vs Full Bridge

Supply voltage	0.5 x 2ch	1
Current ratings	1	2
MOSFET	2 MOSFETs/CH	4 MOSFETs/CH
Gate Driver	1 Gate Driver/CH	2 Gate Drivers/CH
Linearity		Superior (No even order HD)
DC Offset	Adjustment is needed	Can be cancelled out
PWM pattern	2 level	3 level PWM can be implemented
Notes	Pumping effect Need a help of feed back	Suitable for open loop design

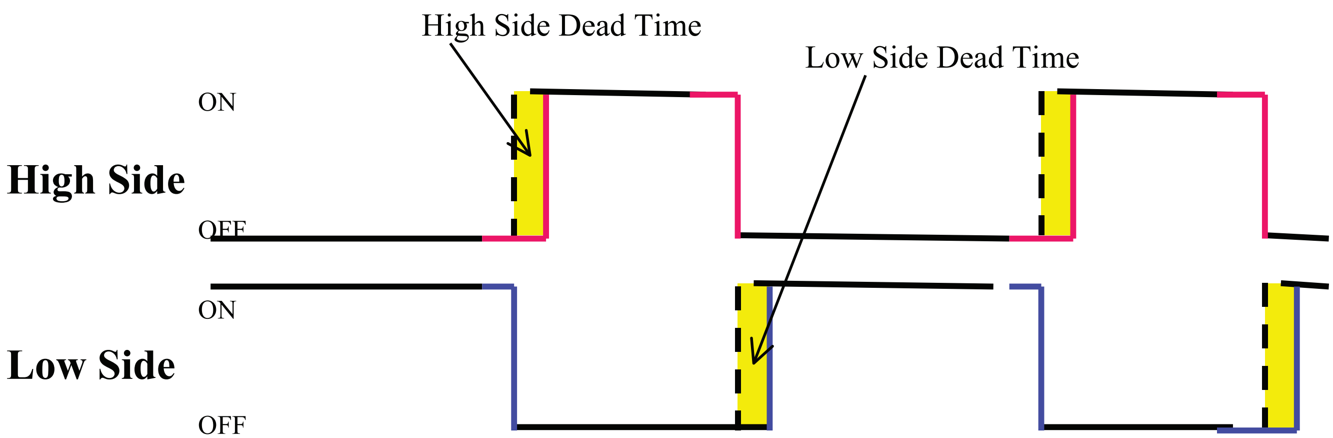


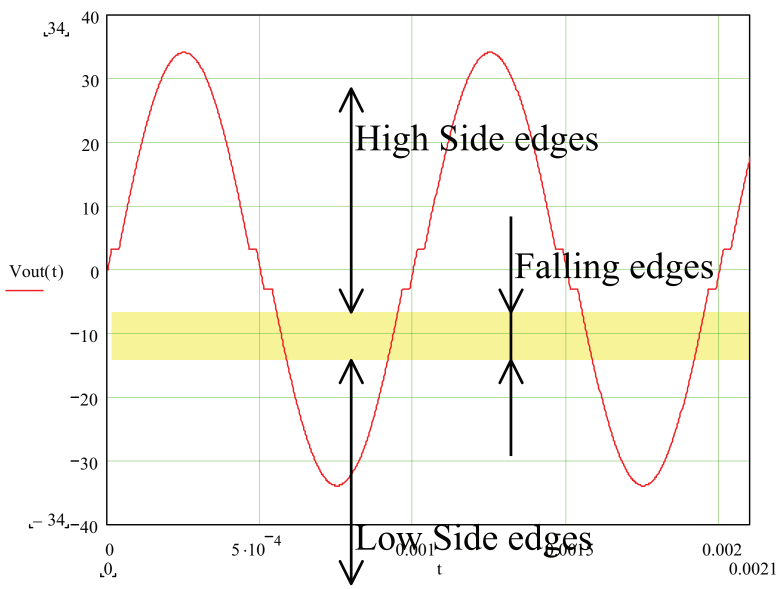


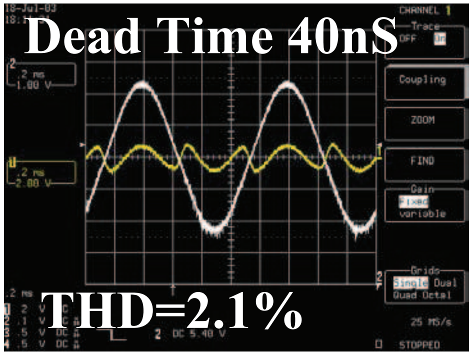
Major Cause of Imperfection

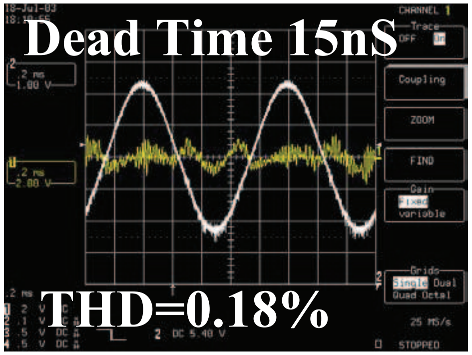


THD and Dead Time





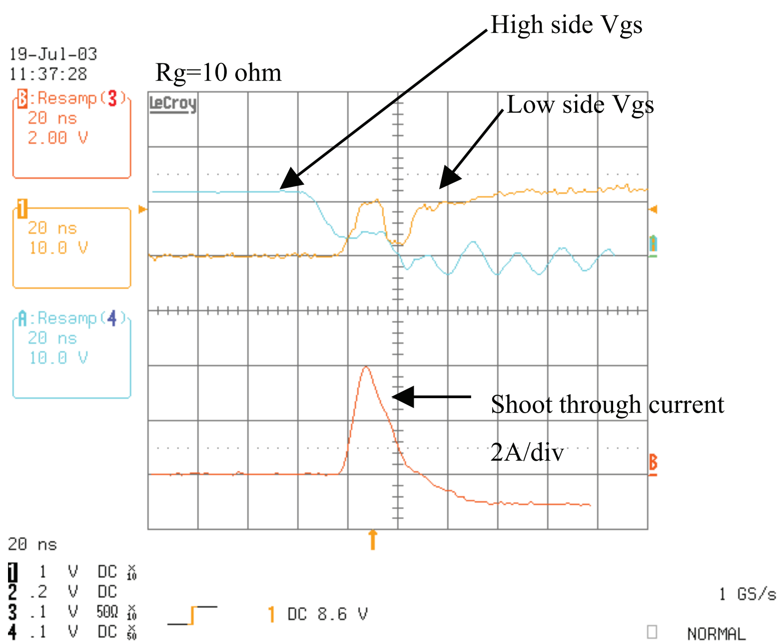


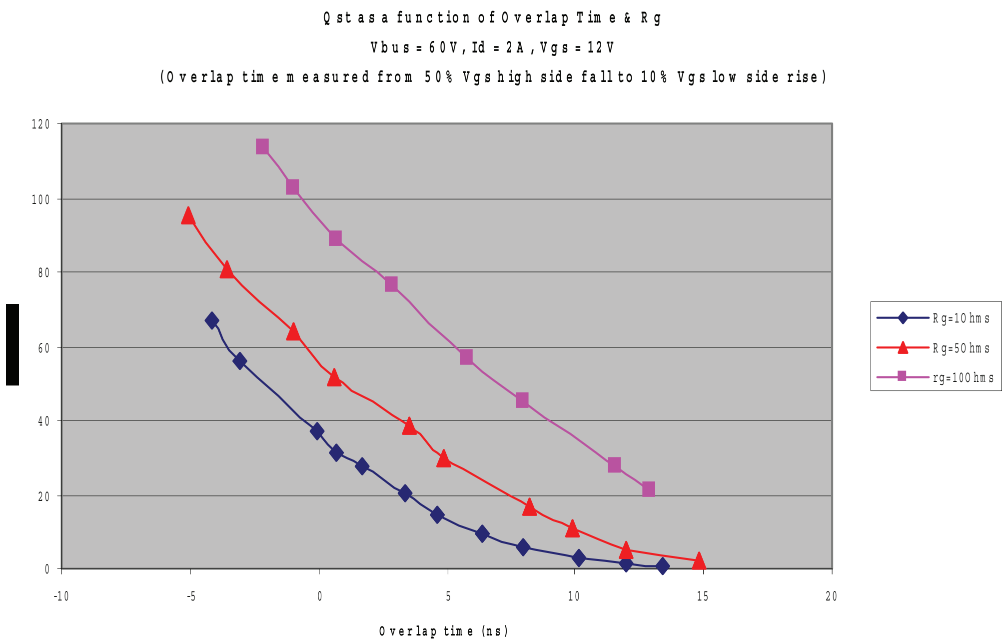


Note: THD (Total Harmonic Distortion) is a means to measure linearity with sinusoidal signal.

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \cdots}}{V_{fundamental}}$$

Shoot Through and Dead Time

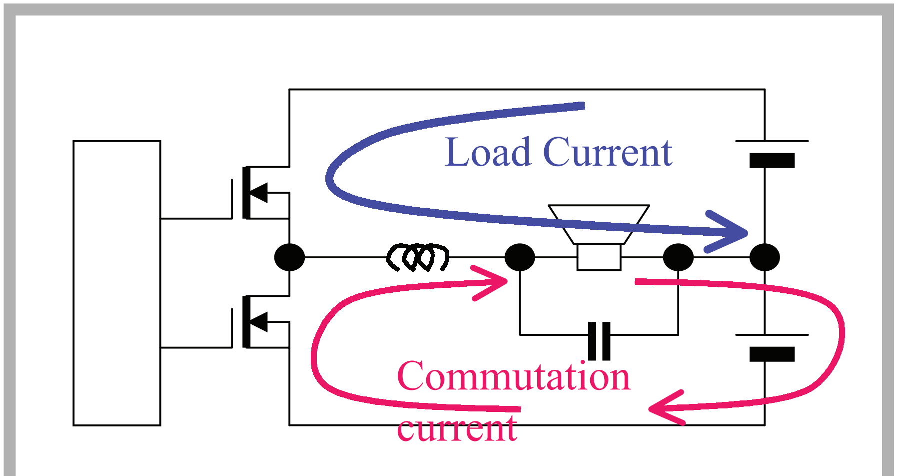




-Shoot through charge increases rapidly as dead time gets shorter.

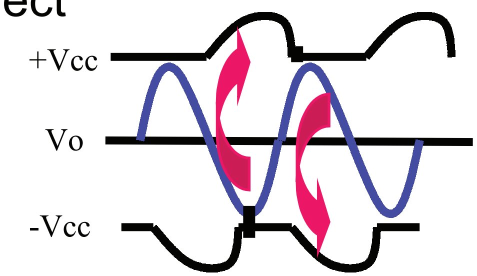
-Need to consider manufacturing tolerances and temperature characteristics.

Power Supply Pumping



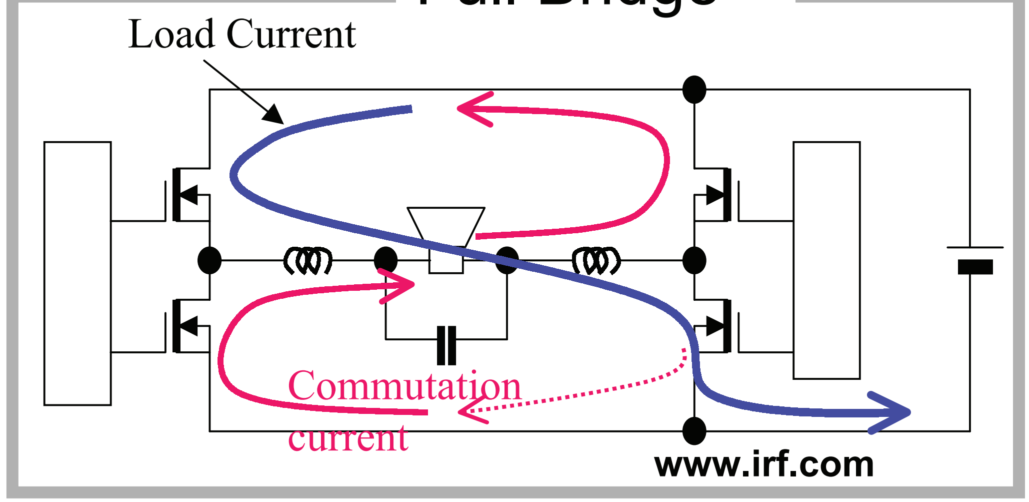
Half Bridge

Supply voltage Pumping effect



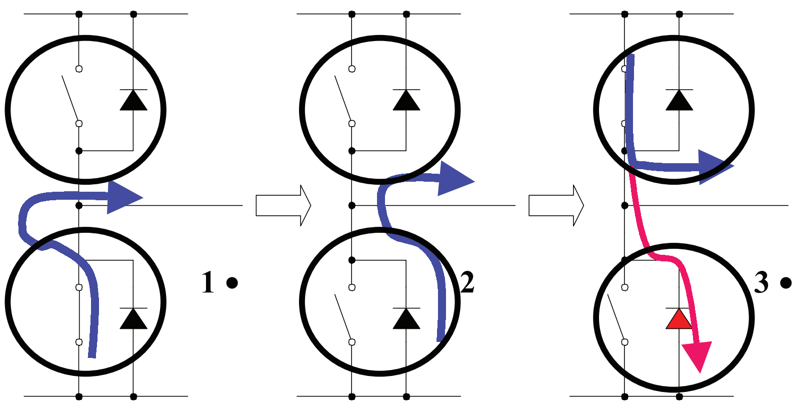
$$\Delta V_{BUS}\ \max = \frac{V_{BUS}}{8 \cdot \pi \cdot f_{PWM} \cdot R_{LOAD} \cdot C_{BUS}}$$

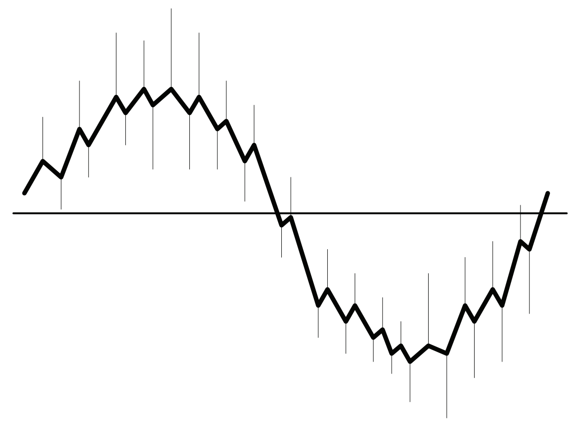
Full Bridge



- -Significant at low frequency output
- -Significant at low load impedance
- -Significant at small bus capacitors
- -Largest at duty = 25%, and 75%

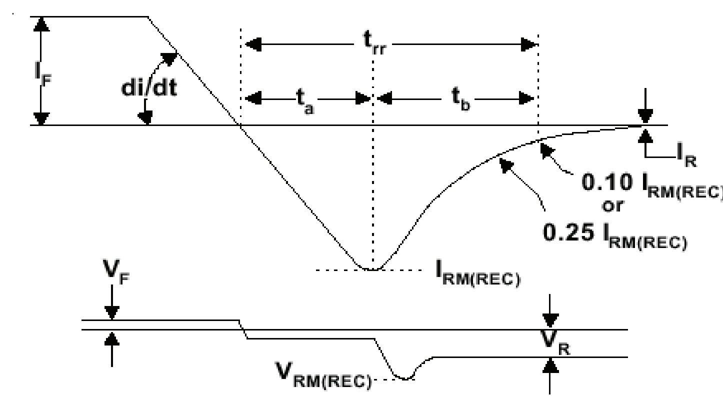
EMI consideration: Qrr in Body Diode





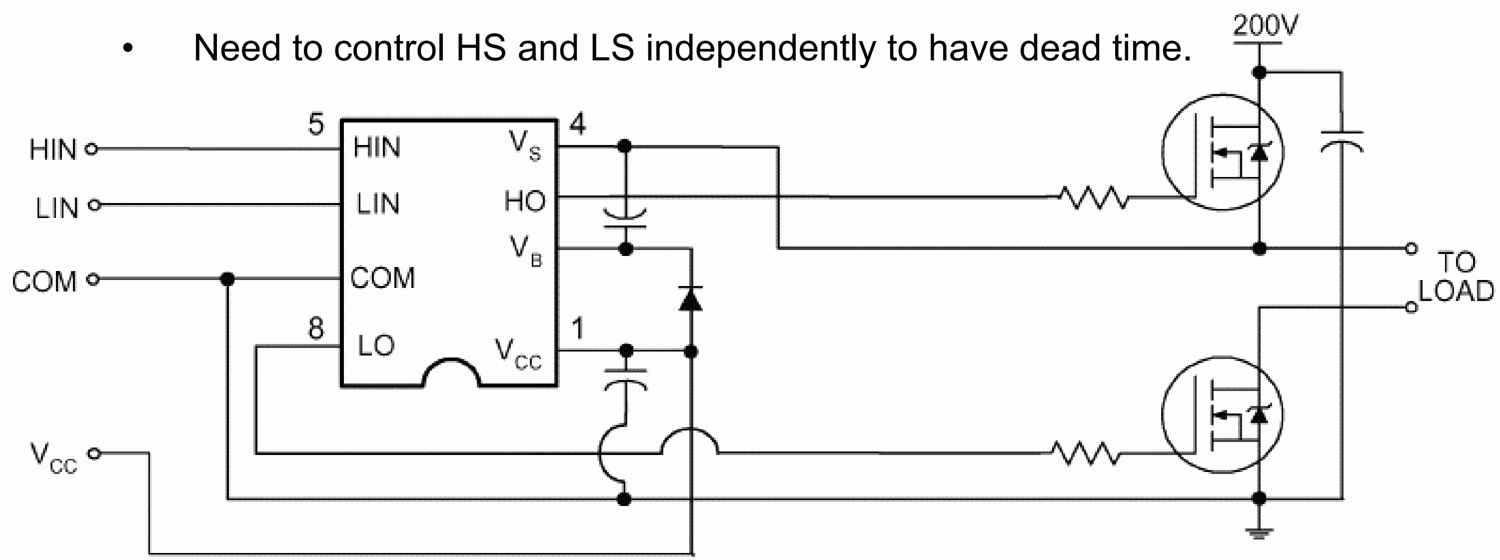
1. Low side drains inductor current
2. During dead time body diode of low side conducts and keep inductor current flow
3. At the moment high side is turned ON after dead time, the body diode is still conducting to wipe away minority carrier charge stored in the duration of forward conduction.

➔This current generates large high frequency current waveform and causes EMI noises.

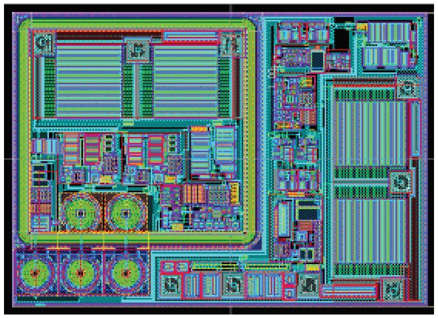


Gate Driver: Why is it Needed?

- Gate of MOSFET is a capacitor to be charged and discharged. Typical effective capacitance is 2nF.
- High side needs to have a gate voltage referenced to it's Source.
- Gate voltage must be 10-15V higher than the drain voltage.
- Need to control HS and LS independently to have dead time.

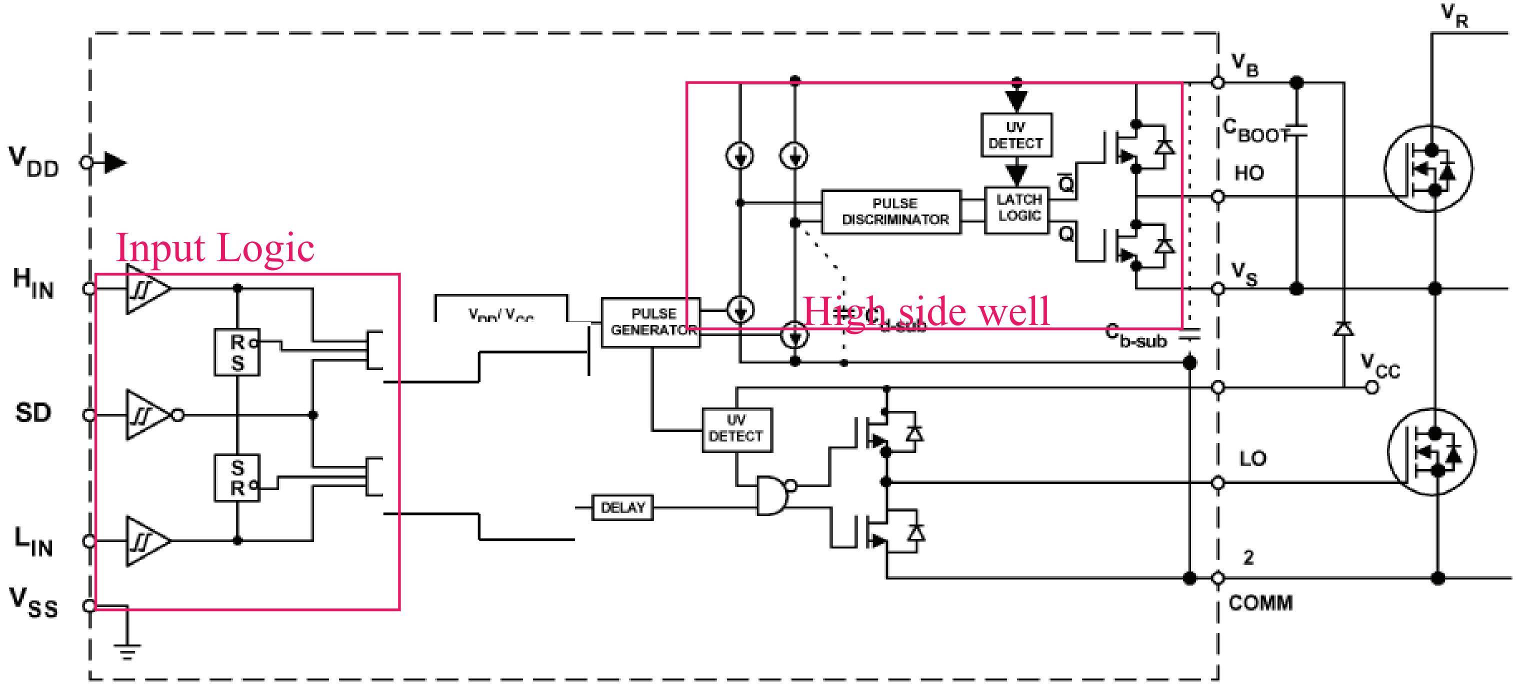


Functional Block Diagram Inside Gate Driver

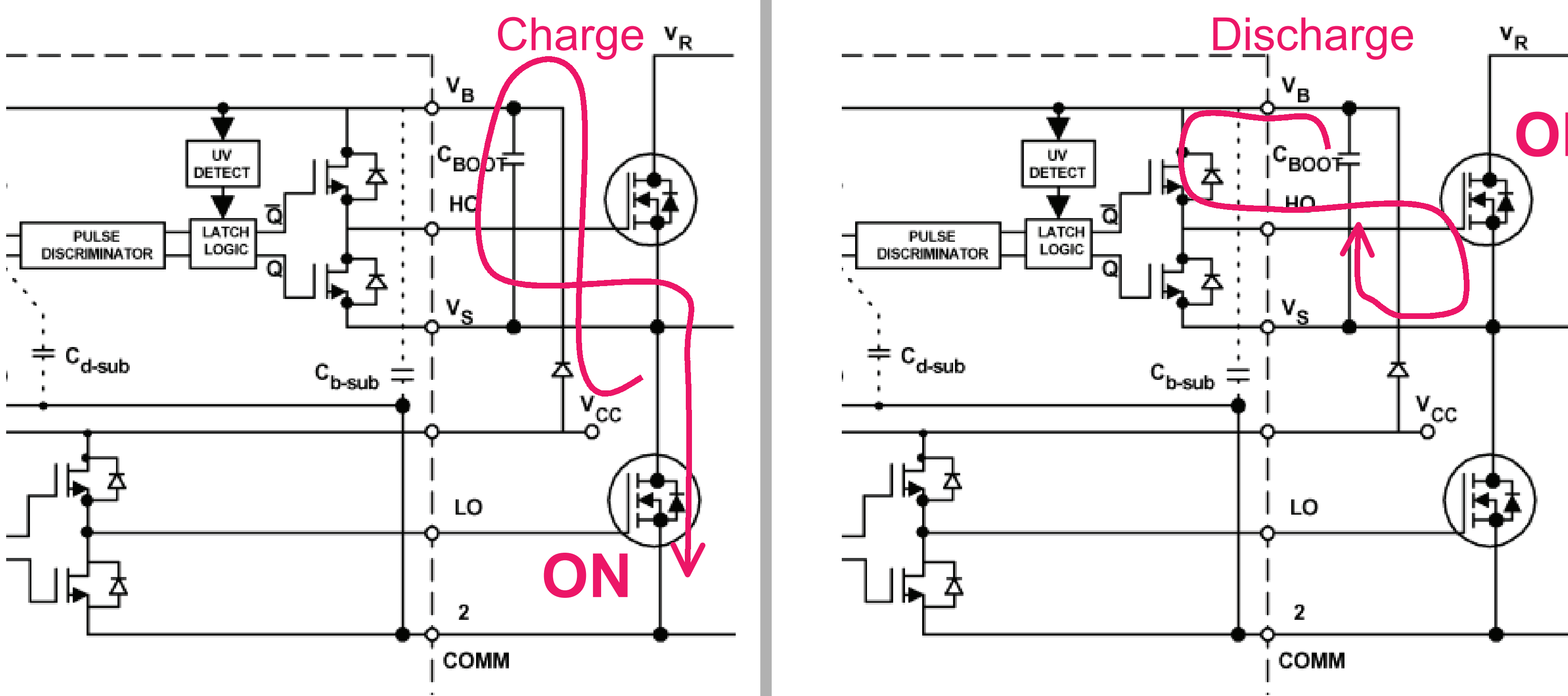


International Rectifier's family of MOS gate drivers integrate most of the functions required to drive one high side and one low side power MOSFET in a compact package.

With the addition of few components, they provide very fast switching speeds and low power dissipation.



Boot Strap High Side Power Supply



When Vs is pulled down to ground through the low side FET, the bootstrap capacitor (C_{BOOT}) charges through the bootstrap diode (Dbs) from the Vcc supply, thus providing a supply to Vbs.

Boot Strap High Side Power Supply (Cont'd)

- **Boot Strap Capacitor Selection**

$$C \geq \frac{2\left[2Q_g + \frac{I_{qbs(max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{cc} - V_f - V_{LS} - V_{Min}} \qquad \text{EQ(2)}$$

Where:

V_f = Forward voltage drop across the bootstrap diode

V_{LS} = Voltage drop acros FET (or load for a high side driver)

V_{Min} = Minimum voltage between V_B and V_S

To minimize the risk of overcharging and further reduce ripple on the Vbs voltage the Cbs value obtained from the above equation should be should be multiplied by a factor of 15 (rule of thumb).

- **Boot Strap Diode Selection**

The bootstrap diode (Dbs) needs to be able to block the full power rail voltage, which is seen when the high side device is switched on. It must be a fast recovery device to minimize the amount of charge fed back from the bootstrap capacitor into the Vcc supply.

VRRM = Power rail voltage, max trr = 100ns, IF > Qbs x f

For more details on boot strap refer to DT98-2

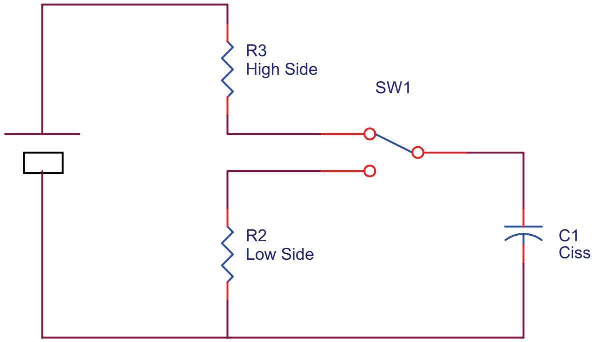
Power Dissipation in Gate Driver

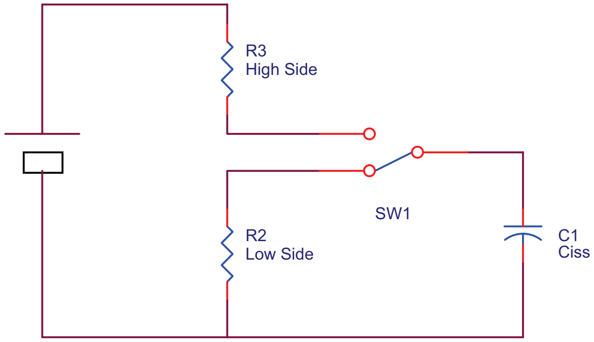
- Whenever a capacitor is charged or discharged through a resistor, half of energy that goes into the capacitance is dissipated in the resistor. Thus, the losses in the gate drive resistance, internal and external to the MGD, for one complete cycle is the following:

$$P_G = V \cdot f_{SW} \cdot Q_G$$

For two IRF540 HEXFET® MOSFETs operated at 400kHz with Vgs = 12V, we have:

PG = 2 • 12 • 37 • 10^{-9} • 400 • 10^{3} = 0.36W





For more details on gate driver ICs, refer to AN978

Power Dissipation in Gate Driver (Cont'd)

- The use of gate resistors reduces the amount of gate drive power that is dissipated inside the MGD by the ratio of the respective resistances.

- These losses are not temperature dependent.

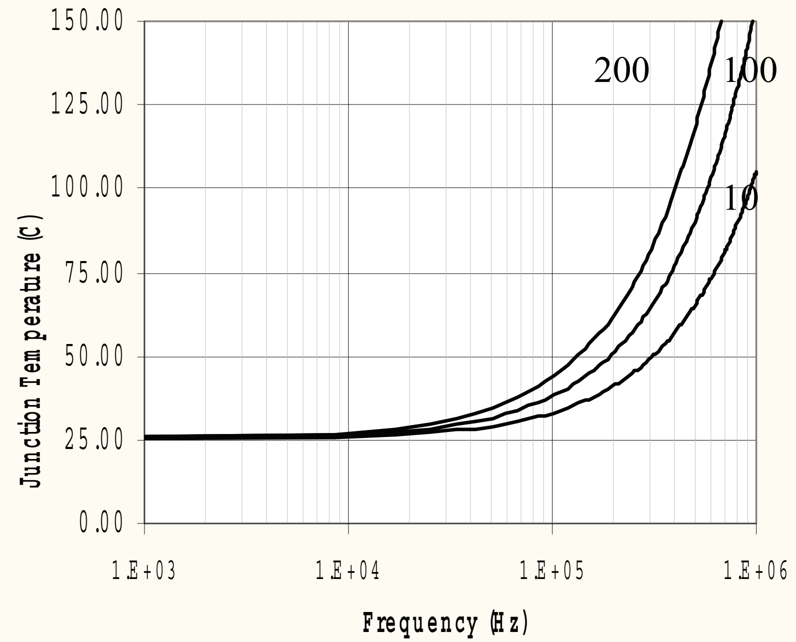
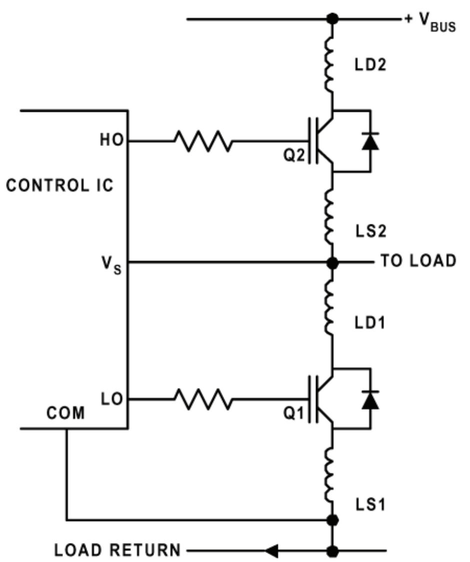
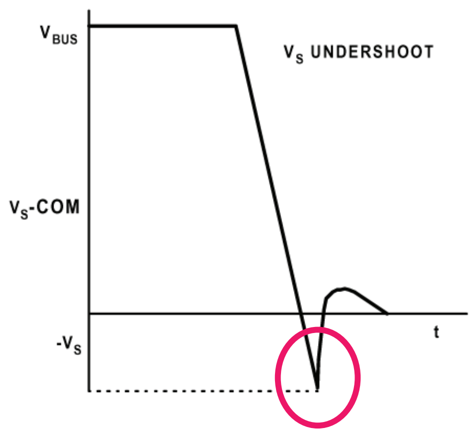


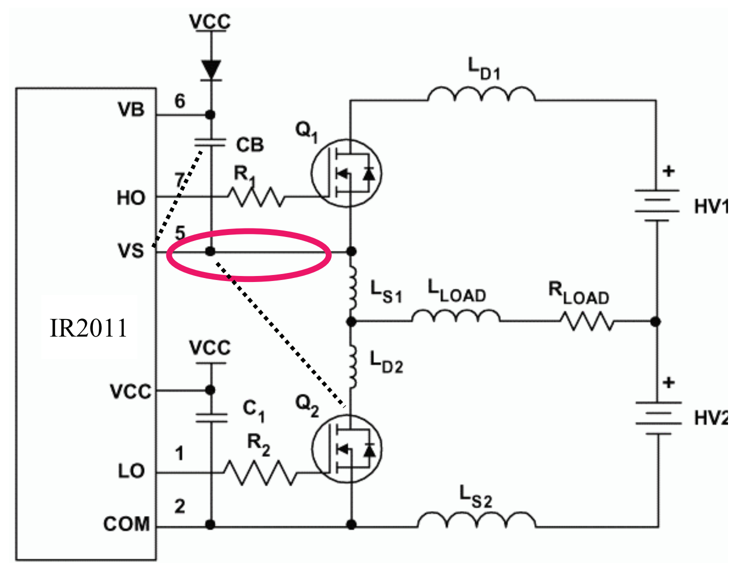
Figure 32: IR2010S Tj vs Frequency
R_{GATE} = 10 Ohm, Vcc = 15V with IRFPE50

Layout Considerations

- Stray inductance LD1+LS1 contribute to undershoot of the Vs node beyond the ground







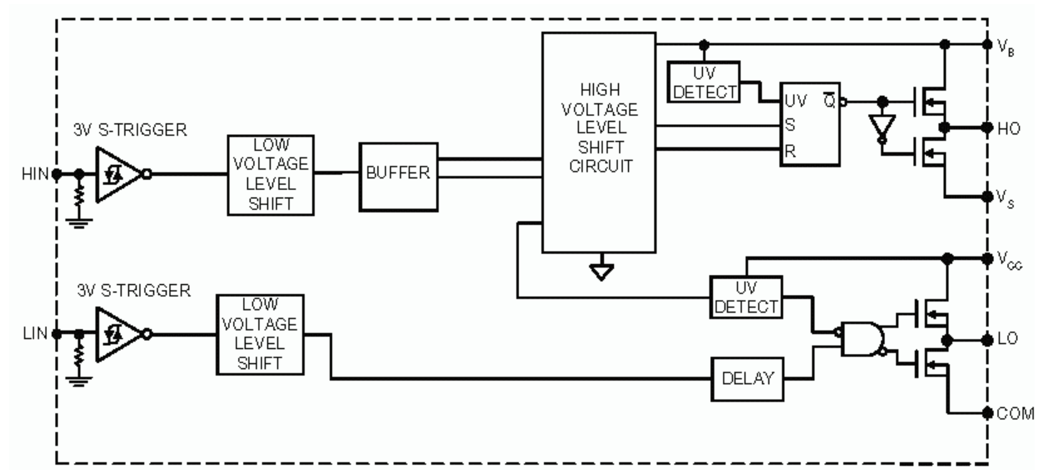
As with any CMOS device, driving any of parasitic diodes into forward conduction or reverse breakdown may cause parasitic SCR latch up.

Gate Driver for Class D Applications

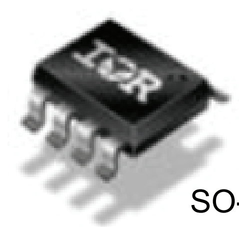
IR2011(S)

Key Specs

V_{OFFSET}	200V max.
I_O+/-	1.0A /1.0A typ.
V_{OUT}	10 - 20V
$t_{on/off}$	80 & 60 ns typ.
Delay Matching	20 ns max.



- Fully operational up to +200V
- Low power dissipation at high switching frequency
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Tolerant to negative transient voltage, dV/dt immune
- SO-8/DIP-8 Package

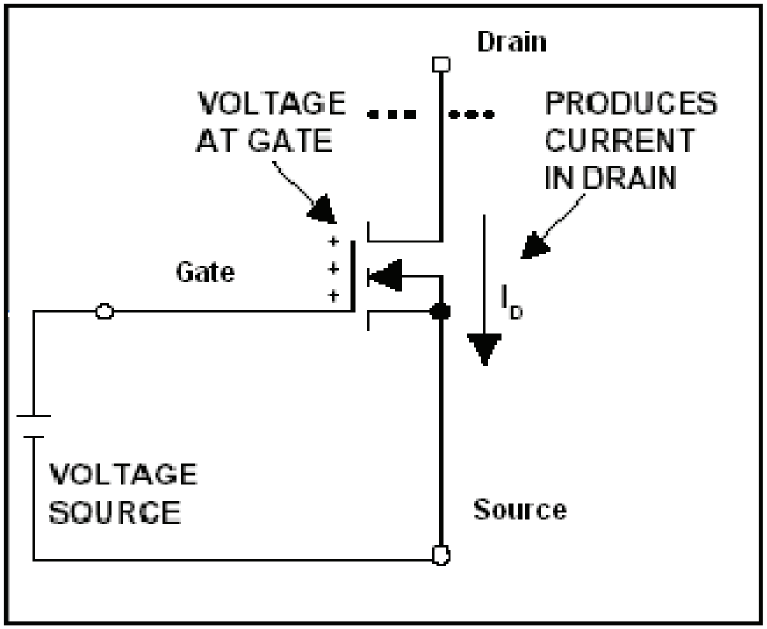


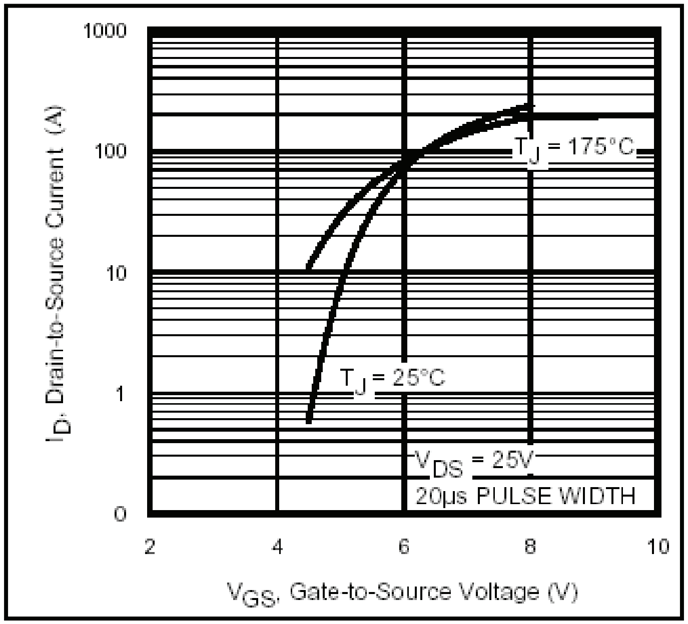
SO-8

How MOSFETs Work

- **A MOSFET is a voltage-controlled power switch.**

  A voltage must be applied between Gate and Source terminals to produce a flow of current in the Drain.

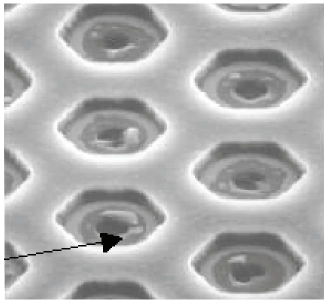




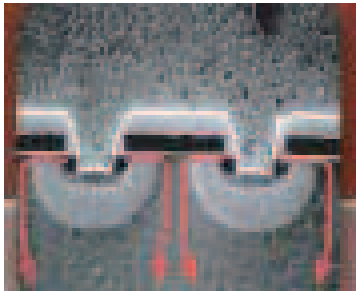
MOSFET Technologies (1)

- **IR is striving to continuously improve the power MOSFET to enhance the performance, quality and reliability.**

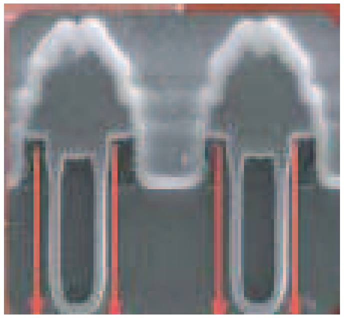
- **Hexagonal Cell Technology**



- **Planar Stripe Technology**

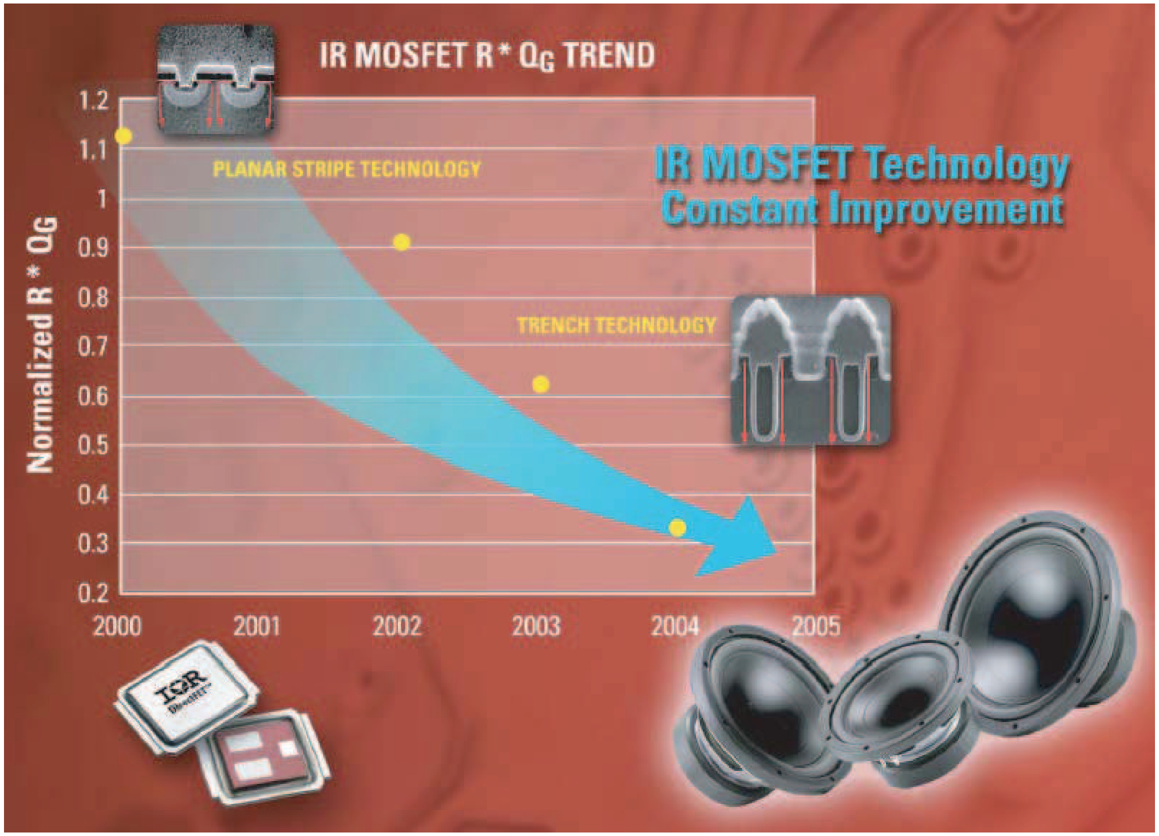


- **Trench Technology**



MOSFET Technologies (2)

- **Power MOSFET FOMs (R*Qg) have significantly improved between the released IR MOSFET technologies**



Key Parameters of MOSFETs (1)

- **Voltage Rating, BV_{DSS}**

This is the drain-source breakdown voltage (with VGS = 0). BV_{DSS} should be greater than or equal to the rated voltage of the device, at the specified leakage current, normally measured at Id=250uA.

This parameter is temperature-dependent and frequently $\Delta BV_{DSS}/\Delta Tj$ (V/°C) is specified on datasheets.

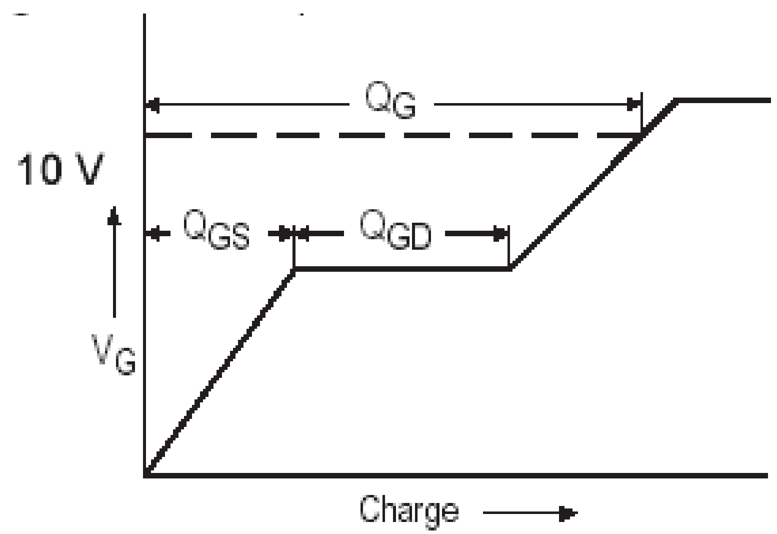
BV_{DSS} MOSFET voltages are available from tens to thousand volts.

Key Parameters of MOSFETs (2)

- **Gate Charge, Qg**

This parameter is directly related to the MOSFET speed and is temperature-independent. Lower Qg results in faster switching speeds and consequently lower switching losses.

The total gate charge has two main components: the gate-source charge, Qgs and, the gate-drain charge, Qgd (often called the Miller charge).



Basic Gate Charge Waveform