RS Data Library

# Bucket brigade delay lines

**Stock numbers 631-288 to 301**

The RS bucket brigade delay line system comprises two delay lines and a matching clock driver.

## Introduction to the bucket-brigade delay line

To characterise an analogue signal of f hertz completely, at least 2f samples per second are needed. If these are stored in the stages of a kind of shift register then the attractive features of the shift register – especially as a delay line – can be used for analogue signal handling.

Sampled values of the analogue signal are stored in the form of charges on a series of capacitors. Between successive capacitors is a switch that transfers the charge from one capacitor to the next on command of a clock pulse. By analogy with the old fire-fighting method, in which buckets of water were passed along the line from man to man, a delay line of this sort is known as a bucket-brigade.

Since each capacitor cannot take up a new charge until it has passed on its previous one, only half the capacitors carry information and the ones in between are empty. Starting from the condition shown in Figure 1(a), the transfer proceeds in two stages:

in the first, bucket 1 empties into bucket 2, and bucket 3 into bucket 4;

and in the second, bucket 2 empties into bucket 3, and bucket 4 into bucket 5.

Two antiphase clock signals are required; one to govern the emptying of even-numbered, and the other of odd-numbered buckets.

There is a practical drawback to the scheme illustrated in Figure 1. The buckets in which the samples are stored must empty completely during each transfer. In practice, the buckets are capacitors and the samples are charges on them. Owing to leakage current, complete discharge is difficult to ensure. So instead, the scheme illustrated in Figure 2 is adopted.

Figure 2(a) represents the initial condition; buckets 2 and 4 are full, and samples are stored in buckets 1 and 3. During the first transfer, bucket 2 fills bucket 1, and bucket 4 fills bucket 3. What remains in bucket 2 is then equal to the original contents of bucket 1, and what remains in bucket 4 is equal to the original contents of bucket 3. During the next transfer, bucket 3 fills bucket 2, and bucket 5 fills bucket 4. Thus, as the buckets empty from right to left, the sampled quantities move, as before, from left to right; that is, from input to output. This is the scheme used in a practical bucket-brigade delay line.

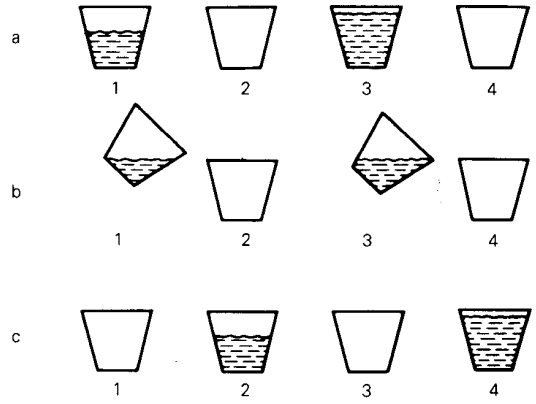



Figure 1 **Sample transfer in a bucket-brigade, simplified scheme. Samples in buckets 1 and 3 (a) are poured into empty buckets 2 and 4 (b); thus, the samples move step by step from left to right (c)**

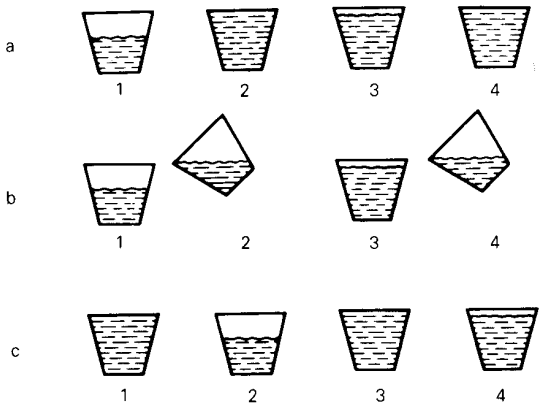



Figure 2 **Sample transfer in a bucket-brigade, practical scheme. Buckets 1 and 3 contain samples (a); when full buckets 2 and 4 are poured into them (b), the sample quantities move, as before, from left to right (c)**

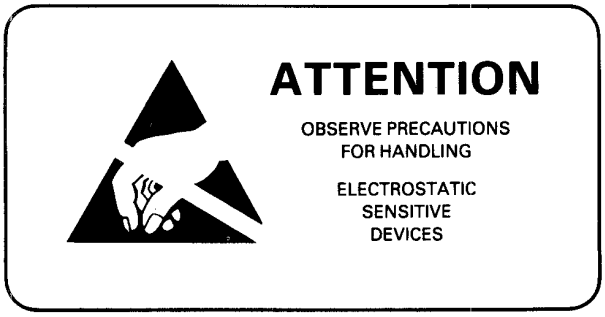
## MN3004 (631-288)

The MN3004 is a 512 stage, low noise, bucket brigade delay line providing a signal to noise ratio of 85dB. The device features low insertion loss and no gate back bias is required.

Analogue signals, in the audio band, can be delayed by 2.56ms to 25.6ms by adjusting the clock frequency. The device is ideally suited for processing audio signals to generate an artificial delay in public address systems. May also be used to obtain musical effects such as reverberation, vibrato and chorus effects.

### Absolute maximum ratings

| | |
|---|---|
| Supply voltage | −18V to +0.3V |
| Output voltage | −18V to +0.3V |
| Operating temperature | −20°C to +60°C |
| Storage temperature | −55°C to +125°C |




### Features

- Variable delay of audio signal: 2.56ms ~ 25.6ms
- Clock component cancellation capability
- Low insertion loss: $L_i$ = 1/5dB typ.
- Wide dynamic range: S/N ≃ 85dB typ.
- Wide frequency response: $f_i \leq 0.3 \times f_{cp}$
- Clock frequency range: 10~ 100kHz
- Low noise: $V_{no}$ = 0.21mVrms max.
- Low distortion: THD = 0.4% typ.

### Applications

- Reverberation and echo effects of audio equipments such as stereo.
- Tremolo, vibrato and chorus effects in electronic musical instruments.
- Variable or fixed delay of analogue signals.
- Telephone time compression and delay line for voice communications systems.

Pin connections

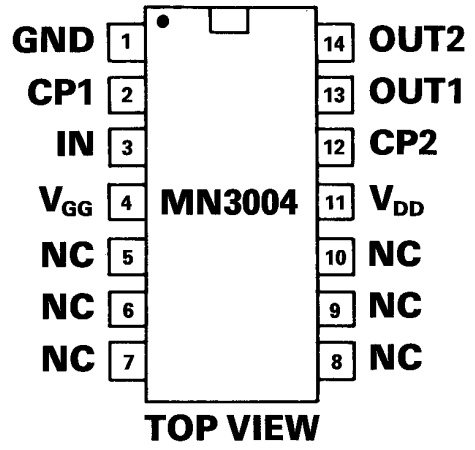
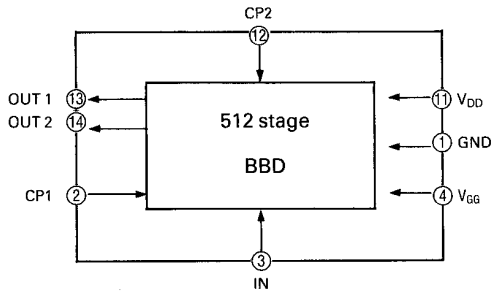



Figure 3 **Block diagram**



## Operating conditions (Ta = 25°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain supply voltage | $V_{DD}$ | | −14 | −15 | −16 | V |
| Gate supply voltage | $V_{GG}$ | | | $V_{DD}+1$ | | V |
| Clock voltage 'H' level | $V_{CPH}$ | | 0 | | −1 | V |
| Clock voltage 'L' level | $V_{CPL}$ | | | $V_{DD}$ | | V |
| Clock input capacitance | $C_{CP}$ | | | | 350 | pF |
| Clock frequency | $f_{CP}$ | | 10 | | 100 | kHz |
| Clock pulse width * | $t_{cpw}$ | | | | 0.5T** | |
| Clock rise time * | $t_{cpr}$ | | | | 500 | ns |
| Clock fall time * | $t_{cpf}$ | | | | 500 | ns |
| Clock cross point | $V_X$ | | 0 | | −3 | V |
| Input dc bias | $V_{Bias}$ | | −5 | | −10 | V |

## Electrical characteristics (Ta = 25°C, $V_{DD} = V_{CPL} = -5V$, $V_{CPH} = 0V$, $V_{GG} = -14V$, $R_L = k\Omega$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Signal delay time | $t_D$ | | 2.56 | | 25.6 | ms |
| Input signal frequency | $f_i$ | $f_{CP}$ = 40kHz, $V_i$ = 1.8Vrms, 3dB down (0 dB at $f_i$ = 1kHz) | 12 | | | kHz |
| Input signal swing | $V_i$ | $f_{CP}$ = 40kHz, $f_i$ = 1kHz, THD ≤2.5% | 1.8 | | | Vrms |
| Insertion loss | $L_i$ | $f_{CP}$ = 40kHz, $f_i$ = 1kHz, $V_i$ = 1.8Vrms | −4 | 1.5 | 4 | dB |
| Total harmonic distortion | THD | $f_{CP}$ = 40kHz, $f_i$ = 1kHz, $V_i$ = Vrms | | 0.4 | 2.5 | % |
| Noise voltage | Vno | $f_{CP}$ = 100kHz weighted by 'A' curve | | | 0.21 | mVrms |
| Signal to noise ratio | S/N | | | 85 | | dB |

* See Figure 4 ** $2T = 1/f_{cp}$ (clock period)

Figure 4 **Timing diagram**

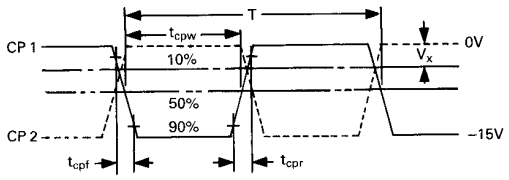
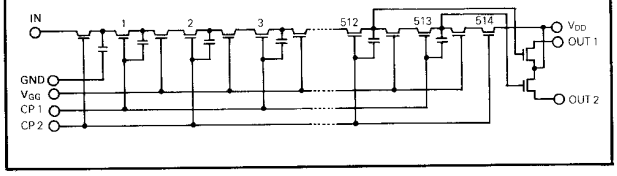



Figure 5 **Internal schematic**




## Typical electrical characteristics

Figure 6 **dc transfer characteristics**

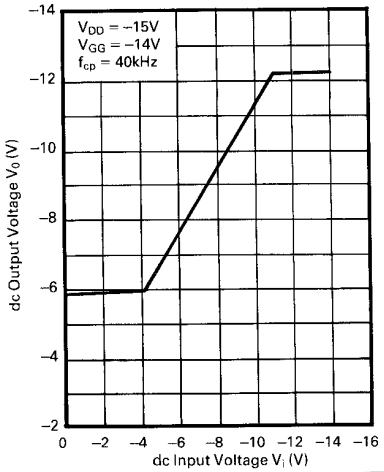



Figure 7 **ac transfer characteristics**

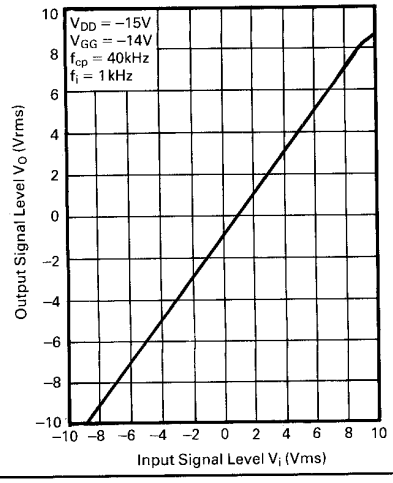


Figure 8 **Total harmonic distortion vs. input signal**

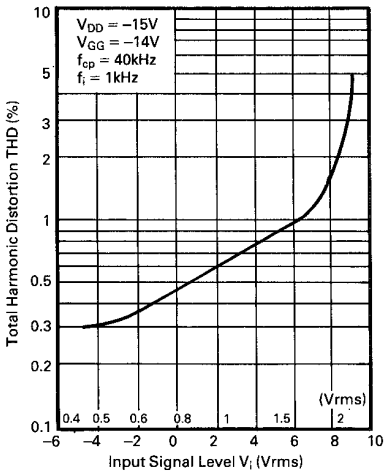



Figure 9 **Total harmonic distortion vs. clock frequency**

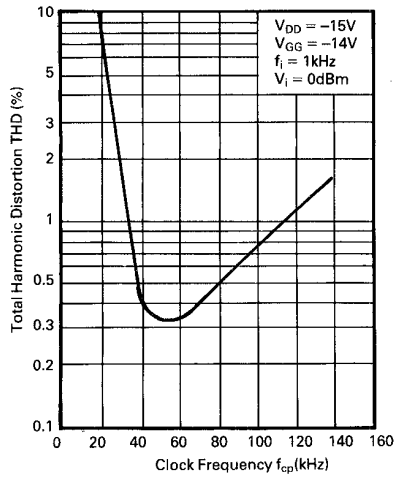



Figure 10 **Insertion gain vs. clock frequency**

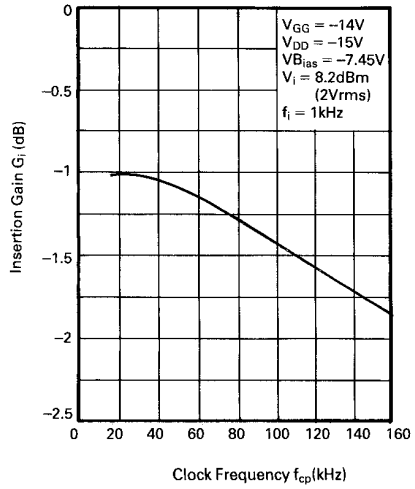



Figure 11 **Frequency response**

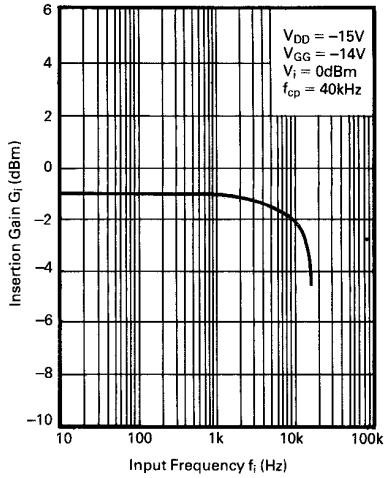



Figure 12 **Noise voltage vs. supply voltage**

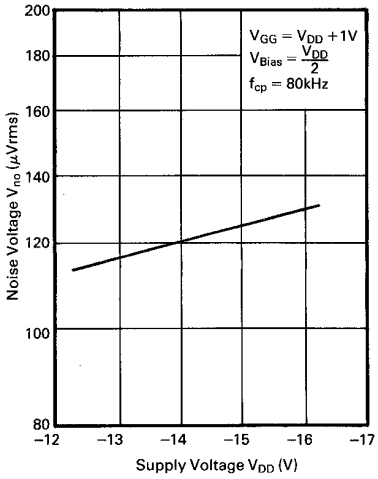
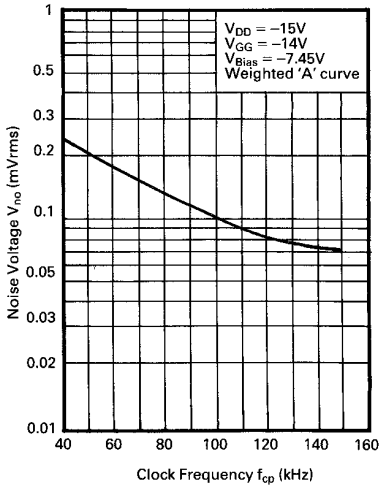



Figure 13 **Noise voltage vs. clock frequency**



## Supply voltage characteristics

Figure 14 **Bias requirements**

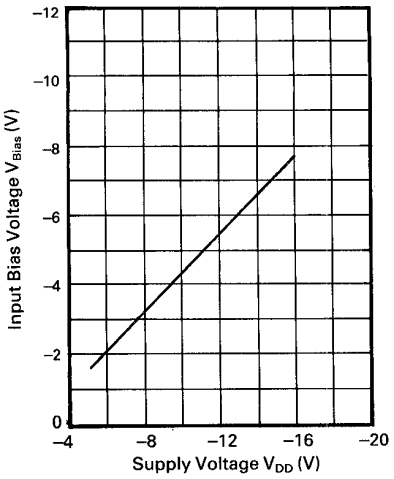



Figure 15 **Total harmonic distortion**

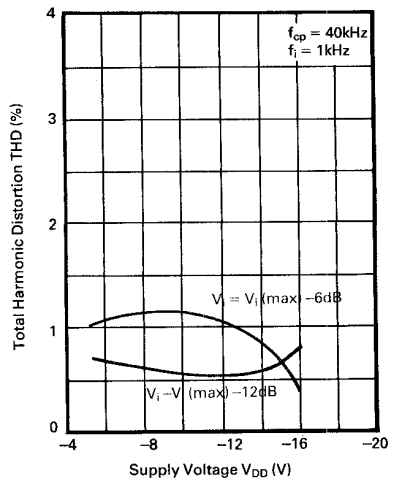



Figure 16 **Maximum input signal vs. supply voltage**

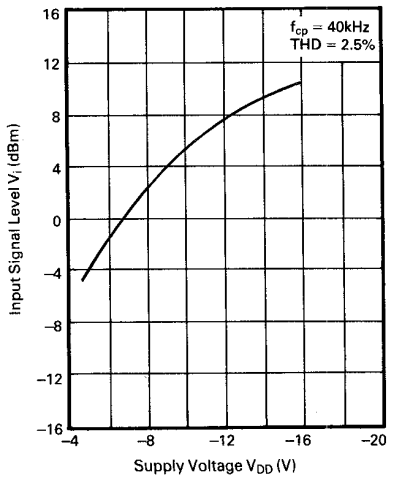



Figure 17 **Insertion gain v. supply voltage**

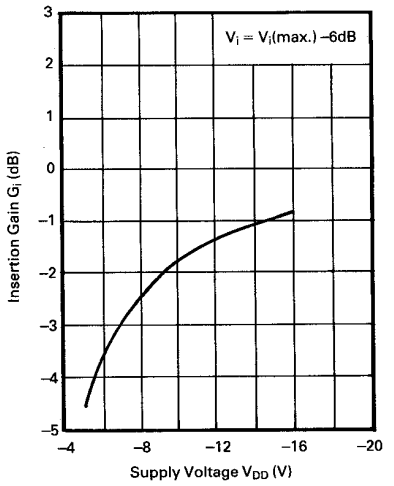
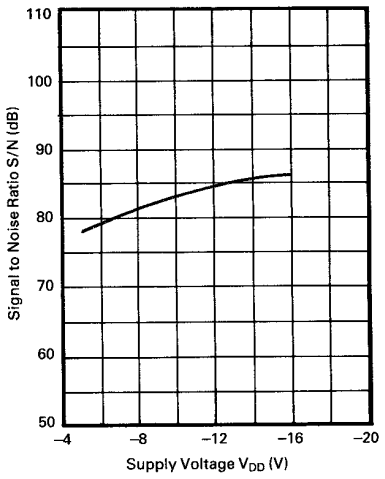
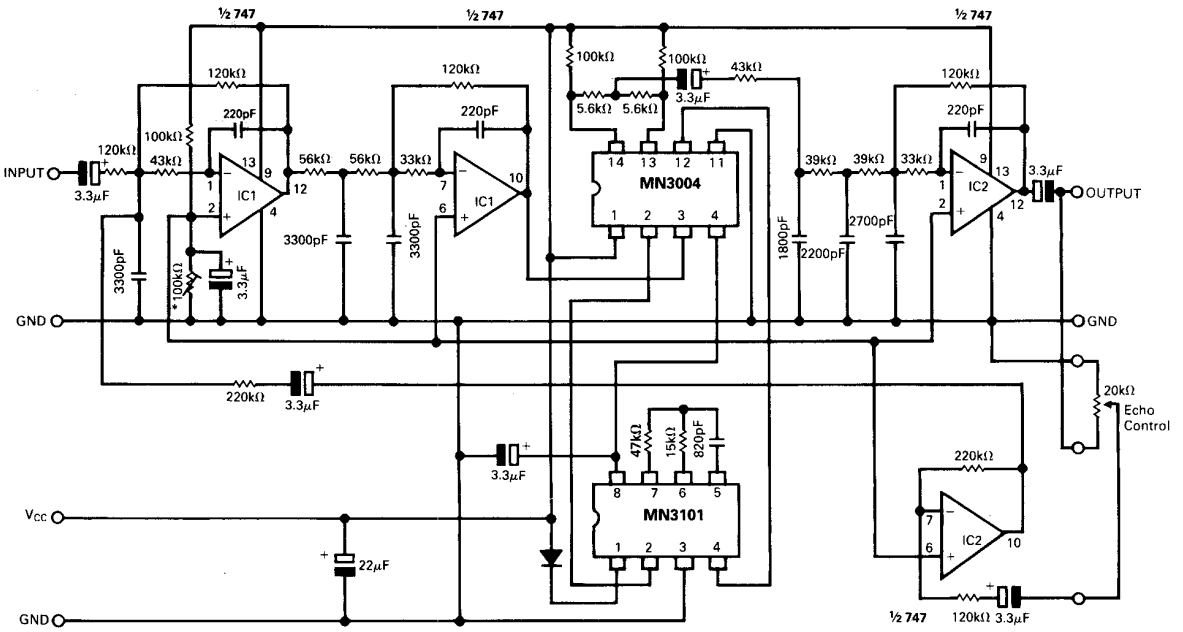



Figure 18 **Signal to noise ratio**



## Typical application

Figure 19 **Echo effect generation circuit (signal delay over 10ms)**




## MN 3011 (631-294)

The MN3011 is a 3328 stage bucket brigade delay line with 6 tap outputs. A signal of different delay is available from each output and when mixed can be used to generate natural reverberation effects. The delay time may be varied by changing the clock frequency.

### Absolute maximum ratings

| | |
|---|---|
| Supply voltage | −18V to +0.3V |
| Input voltage | −18V to +0.3V |
| Output voltage | −18V to +0.3V |
| Operating temperature | −20°C to +70°C |
| Storage temperature | −55°C to +125°C |

### Features

- 3328-stage audio signal delay device with 6 output taps
- Each output tap is independent enabling a natural reverberation effect by mixing the output signals
- Clock component cancellation capability
- Dynamic range: S/N ⩾ 76dB typ.
- No insertion loss: $L_i$ = 0dB typ.
- Low distortion: THD = 0.4% typ.
- P channel silicon gate process.

### Applications

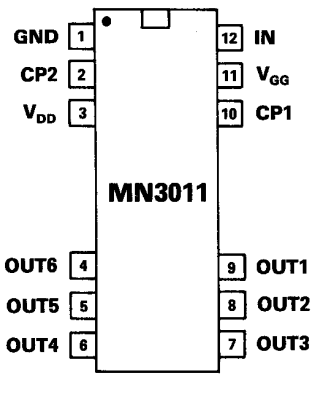
- Reverberation effect in audio equipment
- Chorus effect in electronic musical instruments.

**ATTENTION**

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

**Pin connections**




TOP VIEW

Figure 20 **Block diagram**

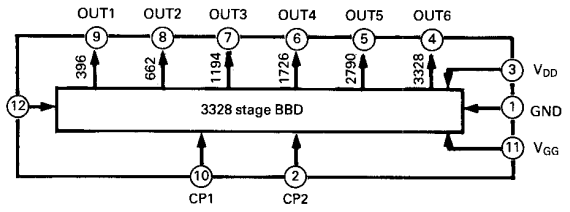
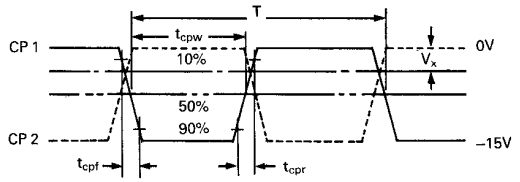



Figure 21 **Timing diagram**




## Maximum delay time by tap output

| Terminal of the tap output | OUT 1 | OUT 2 | OUT 3 | OUT 4 | OUT 5 | OUT 6 | Remarks |
|---|---|---|---|---|---|---|---|
| Stages of BBD (Stage) | 386 | 662 | 1194 | 1726 | 2790 | 3328 | |
| Maximum delay time (mS) | 19.8 | 33.1 | 59.7 | 86.3 | 139.5 | 166.4 | Clock 10kHz |

## Operating conditions (Ta = 25°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain supply voltage | $V_{DD}$ | | −14 | −15 | −16 | V |
| Gate supply voltage | $V_{GG}$ | | | $V_{DD}+1$ | | V |
| Clock voltage 'H' level | $V_{CPH}$ | | 0 | | −1.3 | V |
| Clock voltage 'L' level | $V_{CPL}$ | | | $V_{DD}$ | | V |
| Clock input capacitance | $C_{CP}$ | | | | 2300 | pF |
| Clock frequency | $f_{CP}$ | | 10 | | 100 | kHz |
| Clock pulse width * | $t_{cpw}$ | | | | 0.5T** | |
| Clock rise time * | $t_{cpr}$ | | | | 500 | ns |
| Clock fall time * | $t_{cpf}$ | | | | 500 | ns |
| Clock cross point | $V_X$ | | 0 | | −3 | V |
| Input dc bias | $V_{Bias}$ | | −5 | | −10 | V |

* See Figure 21 ** $2T = 1/f_{cp}$ (clock period)

## Electrical characteristics (Ta = 25°C, $V_{DD} = V_{CPL} = -15V$, $V_{CPH} = 0V$, $V_{GG} = -14V$, $R_L = 56k\Omega$)

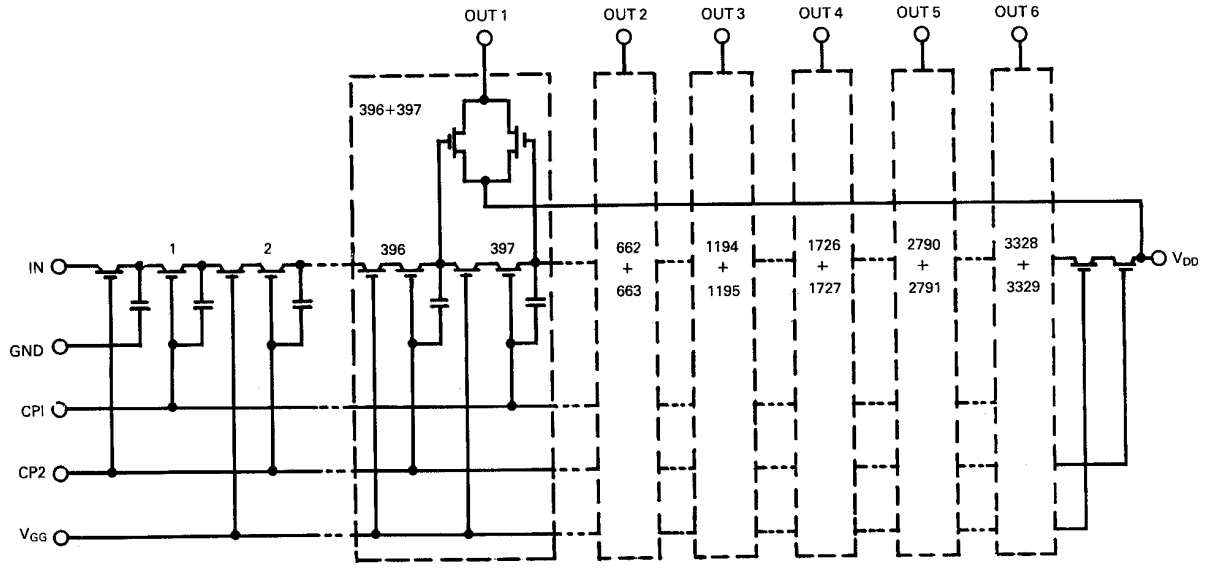
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Signal delay time | | | | | | |
| OUT 1 terminal | $t_{D1}$ | $f_{CP}$ = 10kHz ~ 100kHz | 1.98 | | 19.8 | ms |
| OUT 2 terminal | $t_{D2}$ | | 3.31 | | 33.1 | ms |
| OUT 3 terminal | $t_{D3}$ | | 5.97 | | 59.7 | ms |
| OUT 4 terminal | $t_{D4}$ | | 8.63 | | 86.3 | ms |
| OUT 5 terminal | $t_{D5}$ | | 13.95 | | 139.5 | ms |
| OUT 6 terminal | $t_{D6}$ | | 16.64 | | 166.4 | ms |
| Input signal frequency | $f_i$ | $f_{CP}$ = 40kHz, −3dB | 10 | | | kHz |
| Input signal voltage | $V_i$ | THD = 2.5% | 1.0 | | | Vrms |
| Insertion loss | $L_i$ | $f_{CP}$ = 40kHz, $f_i$ = 1kHz | −4 | 0 | 4 | dB |
| Total harmonic distortion | THD | $f_{CP}$ = 40kHz, $f_i$ = 1kHz, $V_i$ = 0.78Vrms | | 0.4 | 2.5 | % |
| Noise voltage OUT 1, OUT 2, OUT 3 OUT 4, OUT 5, OUT 6 | $V_{no}$ | $f_{cp}$ = 100kHz Weighted by 'A' curve | | | 0.4 | mVrms |
| Signal to noise ratio OUT 1, OUT 2, OUT 3 OUT 4, OUT 5, OUT 6 | S/N | $F_{cp}$ = 100kHz, weighted by 'A' curve Vno vs. max. output signal | | 76 | | dB |

## Terminal description

| Terminal No. | Symbol | Description |
|---|---|---|
| 1 | GND | |
| 2 | CP2 | Clock pulse 2 |
| 3 | $V_{DD}$ | Supply voltage |
| 4 | OUT 6 | Output of stage 3328 |
| 5 | OUT 5 | Output of stage 2790 |
| 6 | OUT 4 | Output of stage 1726 |
| 7 | OUT 3 | Output of stage 1194 |
| 8 | OUT 2 | Output of stage 662 |
| 9 | OUT 1 | Output of stage 396 |
| 10 | CP1 | Clock pulse 1 |
| 11 | $V_{GG}$ | Bias terminal |
| 12 | IN | Signal input terminal |

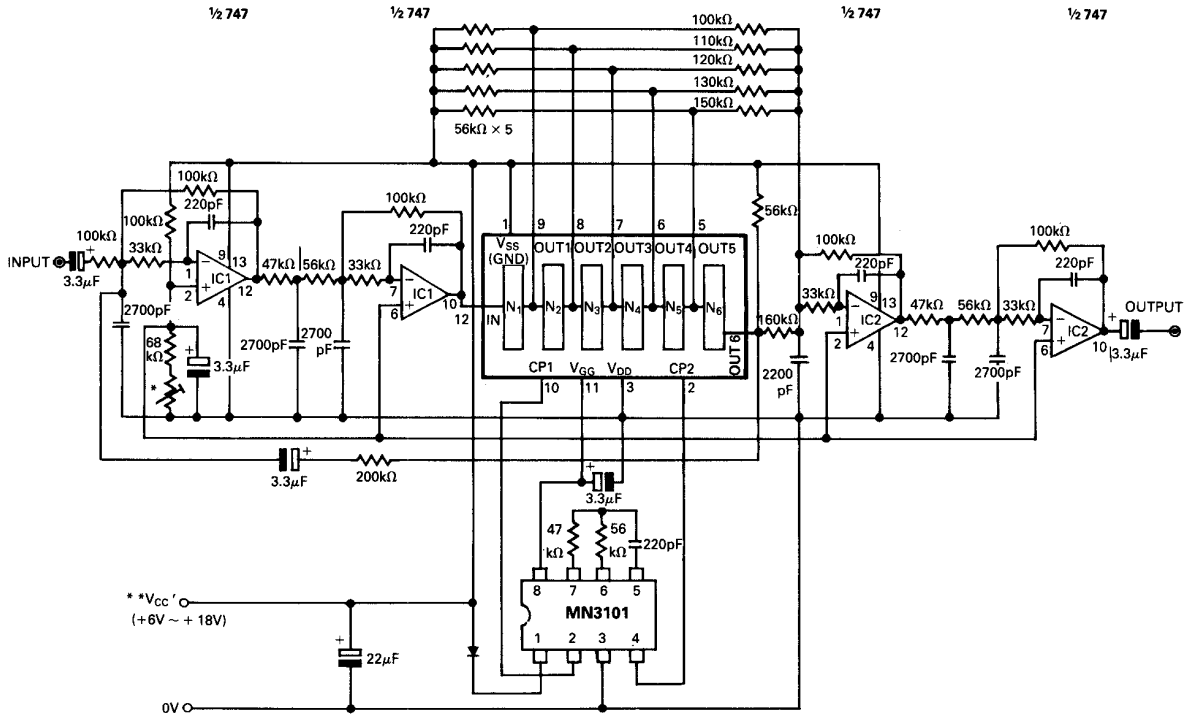
**Note.** Each delayed output is produced by combining signals from the relevant stage with the successive stage and cancelling out the clock components.

Figure 22 **Internal schematic**



## Typical application

Figure 23 **Reverberation effect generation circuit**




* Adjust to minimise distortion (VR 100kΩ typ.)
** $V_{CC}$ should not exceed +18V.

## Application circuit electrical characteristics ($V_{CC}$ = +15V, Ta = 25°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply current | $I_{CC}$ | | | 11(8) | 15(10) | mA |
| Power dissipation | $P_{tot}$ | | | 165(70) | | mW |
| Signal delay time | $t_D$ | OUT 6: $f_{CP}$ = 15 ~ 20kHz | 83 | 98 | 111 | ms |
| Cut-off frequency | $f_{CO}$ | | | 3 | | kHz |
| Input signal swing | $V_i$ | THD = 2.5% | | | 1.1(0.5) | Vrms |
| Insertion loss | $L_i$ | OUT 3: $f_i$ = 1kHz, $V_i$ = 300mV | 0 | 2 | 4 | dB |
| Total harmonic distortion | THD | $f_i$ = 1kHz, $V_i$ = $V_i$(max) -6dB | | 0.4(0.5) | | % |
| Noise voltage | $V_{no}$ | OUT 3: $V_i$ = 0V | | 0.4(0.4) | | mVrms |
| Signal to noise ratio | S/N | $V_S$ = $V_i$ (max) | | 70(60) | | dB |

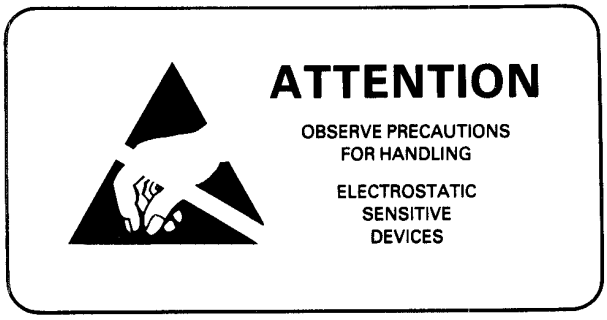
Contents of ( ) represent the value at $V_{CC}$ = +9V

## MN 3101 (631-301)

The MN3101 is a two phase clock generator that is ideally suited for driving the MN3004 or MN3011 bucket brigade delay lines. Oscillation frequency is adjusted by the addition of an external RC circuit.

### Absolute maximum ratings

| | |
|---|---|
| Supply voltage | −18V to +0.3V |
| Input voltage | $V_{DD}$ −0.3V to +0.3V |
| Output voltage | $V_{DD}$ −0.3V to +0.3V |
| Power dissipation | 200mW |
| Operating temperature | −10°C +70°C |
| Storage temperature | −30°C to +125°C |




### Features

- Suitable for driving MN3004 and MN3011 directly
- Internal or external frequency adjustment
- Two phase clock output (Duty: 1/2)
- $V_{GG}$ voltage generator is built-in for MN3004 and 3011
- Single power supply: −8 to −16V
- 8-lead Dual-in-Line plastic package.

Pin connections

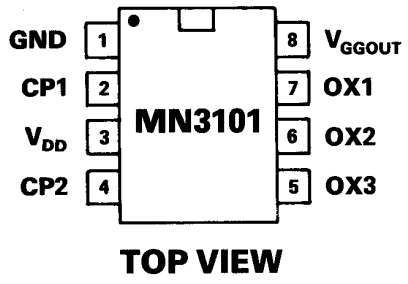
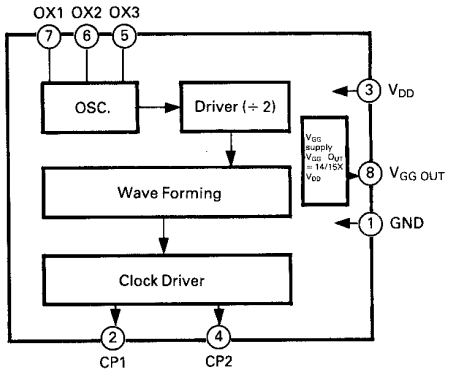



Figure 24 **Block diagram**

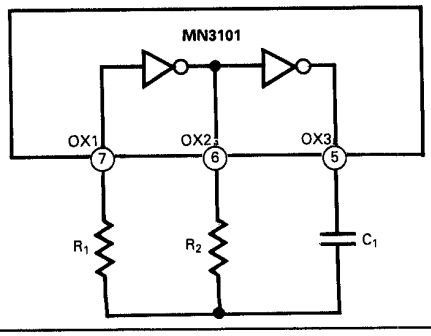



### Operating condition (Ta = 25°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain supply voltage | $V_{DD}$ | GND = 0V | −8 | −15 | −16 | V |

### Clock oscillator frequency adjustment

Figure 25 **Oscillation generation circuit**



## Electrical characteristics (Ta = 25°C, $V_{DD}$ = −15V, GND = 0V)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input drain current | $I_{DD}$ | No load | | 3 | | mA |
| Total power dissipation | $P_{tot}$ | Clock output 40kHz | | 45 | | mW |
| OX1 Input terminal | | | | | | |
| Voltage 'H' level | $V_{IH}$ | | 0 | | −1 | V |
| Voltage 'L' level | $V_{IL}$ | | $V_{DD}$ +1 | | $V_{DD}$ | V |
| Input leakage current | $I_{LK}$ | $V_I$ = 0 ~ −15V | | | 30 | μA |
| OX2 Output terminal | | | | | | |
| Output current 'H' level | $I_{OH1}$ | $V_O$ = −1V | 0.6 | | | mA |
| Output current 'L' level | $I_{OL1}$ | $V_O$ = −14V | 0.5 | | | mA |
| Output leakage current | $I_{LOL1}$ | $V_O$ = $V_{DD}$ | | | 30 | μA |
| Output leakage current | $I_{LOH1}$ | $V_O$ = GND | | | 30 | μA |
| OX3 Output terminal | | | | | | |
| Output current 'H' level | $I_{OH2}$ | $V_O$ = −1V | 1.5 | | | mA |
| Output current 'L' level | $I_{OL2}$ | $V_O$ = −14V | 2 | | | mA |
| Output leakage current | $I_{LOL2}$ | $V_O$ = $V_{DD}$ | | | 30 | μA |
| Output leakage current | $I_{LOH2}$ | $V_O$ = GND | | | 30 | μA |
| CP1, CP2 Output terminal | | | | | | |
| Output current 'H' level | $I_{OH3}$ | $V_O$ = −1V | 10 | | | mA |
| Output current 'L' level | $I_{OL3}$ | $V_O$ = −14V | 10 | | | mA |
| Output leakage current | $I_{LOL3}$ | $V_O$ = $V_{DD}$ | | | 30 | μA |
| Output leakage current | $I_{LOH3}$ | $V_O$ = GND | | | 30 | μA |
| $V_{GG\ OUT}$ Output terminal * | | | | | | |
| Output voltage | $V_{GG\ OUT}$ | | | −14 | | V |

This terminal generates $V_{GG}$ voltage for the MN3004 and MN3011 devices only.

## Terminal description

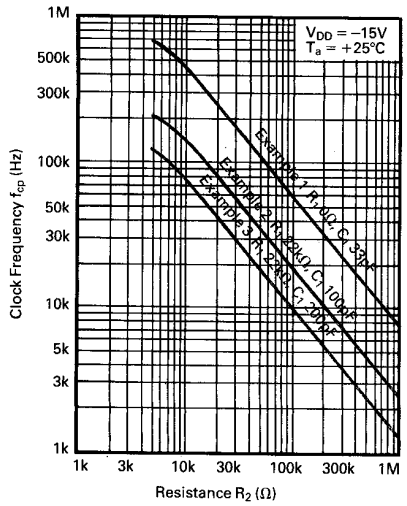
| Terminal No. | Symbol | I/O | Description | |
|---|---|---|---|---|
| 1 | GND | Power supply | Ground | |
| 2 | CP1 | 0 | Clock output 1 | |
| 3 | $V_{DD}$ | Power supply | Supply voltage | |
| 4 | CP 2 | 0 | Clock output 2 (antiphase to CP1) | |
| 5 | OX 3 | 0 | For internal timing see table below | For external timing apply a square wave of the required frequency to pin 7 and leave pins 5 and 6 open circuit |
| 6 | OX 2 | 0 | | |
| 7 | OX 1 | 1 | | |
| 8 | $V_{GG\ OUT}$ | 0 | $V_{GG}$ supply for MN3004 and MN3011 ($V_{GG}$ = $V_{DD}$ x 14/15) | |

## Clock oscillator frequency range

| Example \ Constant | $R_1$ (Ω) | $R_2$ (Ω) | $C_1$ (pF) | $f_{OSC}$** (kHz) | $f_{CP}$* (kHz) |
|---|---|---|---|---|---|
| Example ① | 0 | 5k to 1M | 33 | 15 to 1500 | 7.5 to 750 |
| Example ② | 22k | 5k to 1M | 100 | 5.2 to 440 | 2.6 to 220 |
| Example ③ | 22k | 5k to 1M | 200 | 1.4 to 280 | 0.7 to 140 |

* Clock output frequency of CP1 or CP2 terminals.
** Oscillation frequency of OX1, OX2 and OX3.

Figure 26 **Clock oscillator frequency characteristics**




## The maximum clock frequency

The upper limit of the value of clock frequency is determined depending on the load capacitance and power consumption.

The permissible dissipation for this LSI is $P_D$ = 200mW.

If the clock frequency on the load capacitance is increased, the power consumption will be increased. (Refer to Figure 27.)

Accordingly, in order to utilize the MN3101 with dissipation less than the permissible value, it is necessary to select adequate values for the clock frequency and load capacitance.

Figure 28 shows an example of the dependence of the maximum clock frequency on the load capacitance is $P_D$ = 150mW.

By connecting a resistance to the clock output terminal, it is made possible to increase the value of the maximum clock frequency without increasing dissipation. (Refer to Figures 27 and 28.)

It is because the dissipation on the LSI side is lessened, as a part of the power consumption required for driving the load capacitance is consumed by the series resistance.

Figure 27 **Example of the dependence of power consumption on the clock frequency**

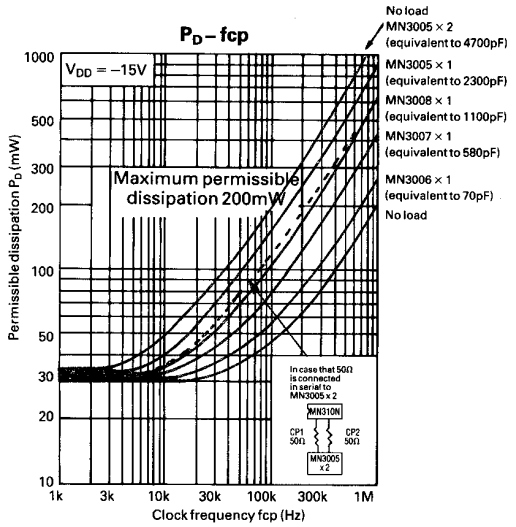



Figure 28 **Example of load capacitance characteristic of the maximum clock frequency in the power consumption of 150mW**