Bar Graph Array Applications

Application Note 1007

Introduction

The need for converting analog information into a visual display exists in many applications. Historically, the designer has had two possible solutions: the traditional panel meter or discrete indicators aligned in an array. There are serious drawbacks with both solutions. Analog panel meters with inherently mechanical movements have been plagued with low tolerance for mechanical shock. Also, there is a strong customer demand for a more aesthetically pleasing display medium. Discrete indicators cause problems due to high parts count, difficult mechanical and optical alignment, as well as intensity and color variations across a display panel. Hewlett-Packard has solved many of these typical problems by introducing the HDSP-4820/-4830/-4840 series of 10 element LED bar graph arrays. The 10 element bar graph array series, available in standard red, high efficiency red, and yellow, offers the designer ultimate flexibility and ease of use in designing a display system.

This application note begins with a description of the manufacturing process used to construct the 10 element array. Next is a discussion of the package design and basic electrical configuration and how they affect designing with the bar graph array. Mechanical information including pin spacing and wave soldering recommendations are made.

Display interface techniques of two basic types are thoroughly discussed. The first of these two drive schemes is applicable in systems requiring display of analog signals in a bar graph format. The second major drive technique interfaces bar graph arrays in systems where the data is of a digital nature. Examples of microprocessor controlled bar graph arrays are presented.

Summarized for the design engineer are tables of available integrated circuits for use with bar graph arrays. Finally, a list of recommended filters is included.

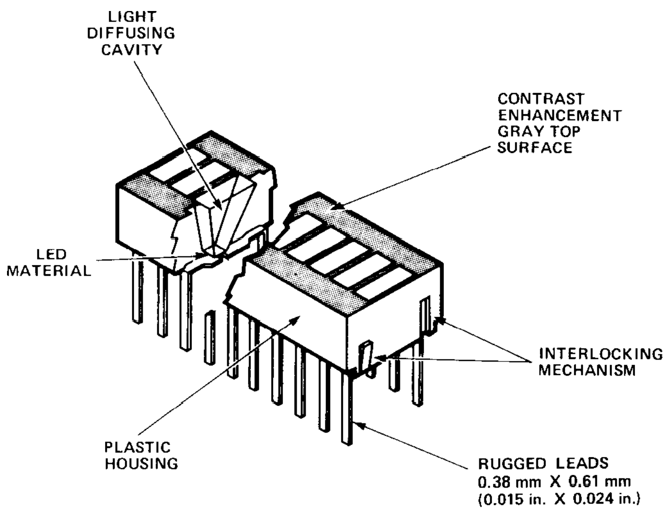

Figure 1. 10 Element Bar Graph (Cutaway)

Device Characteristics

The 10 element bar graph array devices are manufactured using the concept of “stretching” the light from an LED by diffusion and reflection as shown in Figure 1. The LED chips are mechanically supported and electrically connected by a lead frame. The plastic housing, called a “scrambler”, contains reflective cavities which act as light pipes. These cavities are filled with a diffusant epoxy to provide uniform illumination at the emitting surface.

All bar graph arrays are manufactured in standard DIP packages with leads on 2.54 mm (0.100 inch) centers with a row-to-row spacing of 7.6 mm (0.300 inch). As shown in the device schematic in Figure 2, each LED anode and cathode is present on external pins for ease of use.

Each of the 10 elements within the device is matched for luminous intensity. The effect of this matching is that users of a single ten element array need not worry about element-to-element matching within the package. The average luminous intensity for the device is coded by a letter on the side of the package. In applications requiring two or more bar graph arrays end stacked, the user merely chooses devices from a single light intensity category to provide uniform brightness across the display panel.

Color uniformity of the bar graph arrays is an important consideration. The standard red and high efficiency red displays have inherent color uniformity and need not be categorized. However, the eye is more sensitive to color differences in the yellow region. Therefore, the yellow bar graph arrays are categorized by dominant wavelength. These categories are coded by a number on the side of the package. The user should choose units from a single color category to achieve a display panel with optimal color uniformity.

The bar graph arrays have a neutral gray top surface and

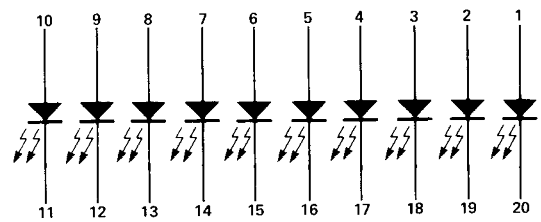

Figure 2. 10 Element Bar Graph Array Schematic

untinted segments to ensure maximum color difference between on and off segments. To maximize contrast enhancement, specially developed filters should be used in conjunction with the bar graph arrays. A list of recommended filters is contained in Table I.

The bar graph arrays offer substantial improvement over discrete devices in the area of mechanical alignment. Because the ten light emitting cavities are molded in a single package, element-to-element consistency as well as mechanical and optical alignment are vastly improved. The package also has a unique interlocking mechanism that eases alignment in applications requiring arrays to be end stacked.

If the bar graph arrays are to be wave soldered, Sn60 or Sn63 solder is recommended. The solder wave temperature should be no greater than 260°C with a maximum dwell time of 3 seconds. The devices have a 1 mm (0.040 inch) standoff which provides clearance above the printed circuit board to facilitate flux removal.

To optimize optical performance, specifically developed plastics are used in the bar graph arrays. These plastics restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes. The immersion time in the vapors should be less than two (2) minutes. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Analog Input Interface Techniques

Many applications for bar graph arrays are in systems where the analog signal needs to be displayed with little or no conditioning. Several analog input IC decoders are available from different manufacturers and are listed in Table II. Although these decoders differ somewhat from manufacturer, the principle upon which they all operate is the same. A block diagram of a typical five element analog input bar graph decoder is shown in Figure 3. Within each IC is a reference voltage network and a set of comparators to detect the level of the analog input signal. When the input signal is greater than the reference voltage for the first comparator, the first output is enabled. As the input signal is increased, subsequent outputs are

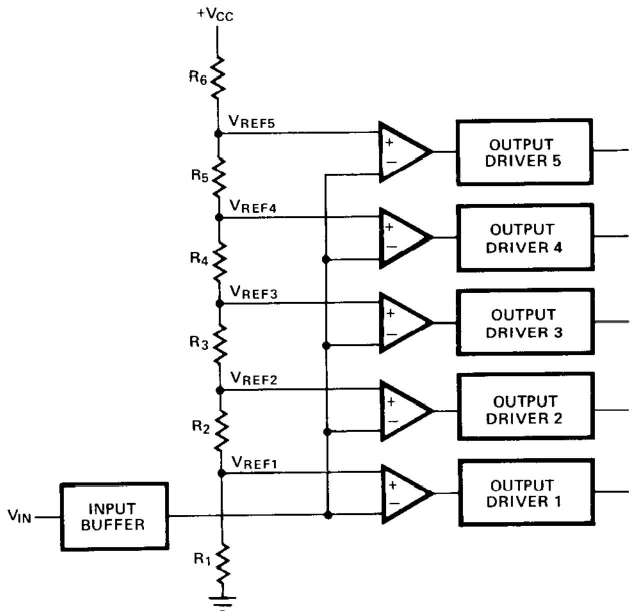

Figure 3. Typical Analog Input Bar Graph Decoder

also enabled. Some manufacturers have incorporated two types of input signal decoding. The first type of decoding turns on all LEDs with voltage thresholds below the analog input (standard bar graph). The second type of decoding turns on only one output at any given time. When the analog input lies within the active region of a particular comparator ($V_{REF\ N} \le V_{IN} < V_{REF\ N+1}$), that output is enabled and all others are disabled. This is known as position indicator mode. Since only one LED is on at any time in the position indicator mode, power dissipation is significantly reduced. Examples of both types of decoding are discussed in this section.

The circuit shown in Figure 4 uses the Texas Instruments TL480C and the HDSP-4820 to form a low cost audio system VU meter. The ten comparators combined with the voltage reference network within the TL480C detect the level of an analog input signal at the A input. Output Q1 is switched to a logic low at a typical input voltage of 203 millivolts. Due to the logarithmic scaling within the part, as the input signal is increased by 2 dB increments, the subsequent outputs are switched to logic low levels and the LEDs are illuminated. If the TL480C is set to display full scale when the analog input is at 2.0 volts, 0 dB to 18 dB can be displayed on the bar graph array.

The circuit shown in Figure 5 utilizes the National LM3914 and the HDSP-4830 to form a flexible, ten element bar graph. The LM3914 is a versatile decoder in that it can operate in two distinct modes. The state of MODE (pin 9) determines the display format. When it is tied directly to Vcc (pin 3), full bar graph decoding occurs. But when MODE is tied to pin 11 the LM3914 operates in position indicator mode. This MODE pin can also be used to cascade additional LM3914s to form bar graphs of greater resolution.

The circuit in Figure 5 displays a 0 V to 5 V signal on the HDSP-4830 high efficiency red bar graph array. The full scale reading is determined by the adjustable voltage at the REF OUT node. The LM3914 forces a nominal 1.25 V constant voltage between REF OUT (pin 7) and REF ADJ (pin 8). In Figure 5 this voltage is applied across resistor R1. Since this voltage is constant, a constant current flows

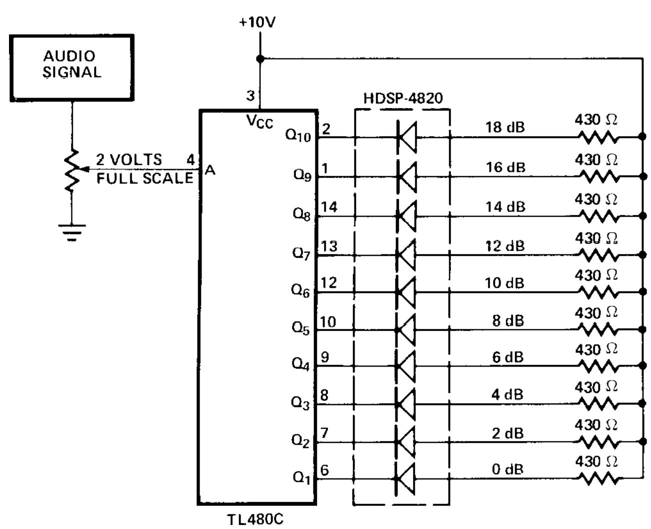

Figure 4. Audio VU Meter

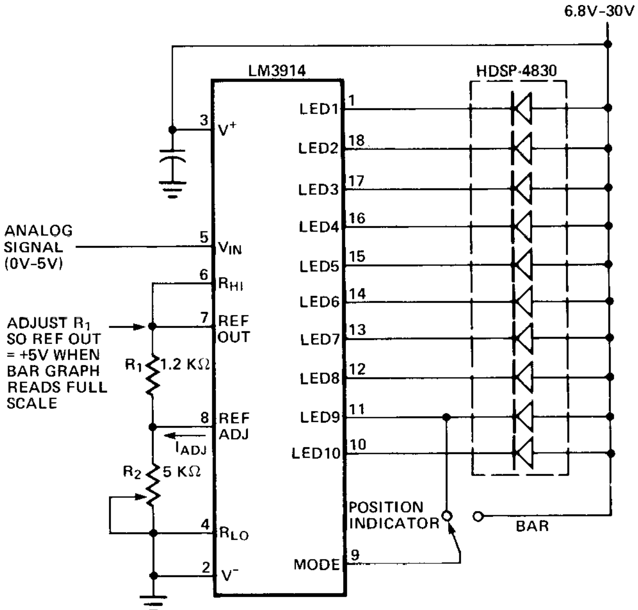

Figure 5. 0 V - 5 V Bar Graph/Position Indicator Meter

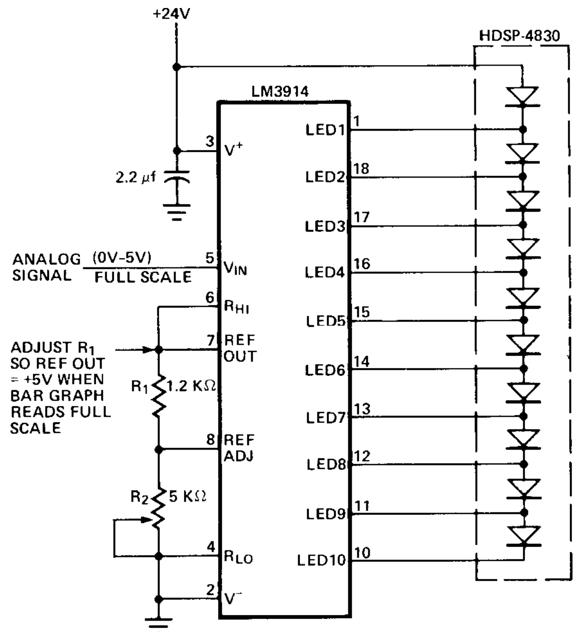

Figure 6. Low Power 0 V - 5 V Bar Graph Meter

through R1 giving an output voltage REF OUT as calculated below.

The value of R1 also determines the LED current. Approximately ten times the current that flows from REF OUT (pin 7) is drawn by each lighted LED. The calculation of LED current is shown below.

Therefore, by choosing R1 for the desired LED brightness, and using the value of I_{ADJ} stated in the LM3914 data sheet (75 µA typical), R2 can be determined. By using a potentiometer for R2, the value of REF OUT can be adjusted to the precise level desired.

The LED current in Figure 5 has been set nominally to 10 mA DC using the techniques described above. When operated in position indicator mode with V_{CC} = 6.8 V, the power dissipation is approximately 110 mW. The worst case power dissipation when operated in bar mode (10 elements on) is approximately 720 mW.

If low power dissipation and full bar graph decoding is desired, the LM3914 can be operated as shown in Figure 6. The LM3914 is again operated in position indicator mode. However, the ten LEDs are driven in series from a +24 V power supply. The REF OUT voltage is adjusted so the bar graph reads +5 V full scale. When V_{IN} lies between 0 V and +0.5 V, no LEDs will be on. When V_{IN} lies between +0.5 V and +1.0 V, Output 1 is enabled and LED 1 is illuminated. Each time the input voltage increases 0.5 V, the 10 mA sink moves to the next output pin, illuminating an additional LED. When the input voltage is +5 V or more (+35 V maximum), all ten LEDs are illuminated with the same 10 mA. To the observer the bar graph appears to operate identically to the one in Figure 5 when in BAR mode. However, the worst case power dissipation has been reduced by approximately one half to 380 mW.

Equations

$$REF\ OUT = 1.25\ V\ (1+R2/R1) + I_{ADJ}(R2)$$

$$I_{LED} = (1.25\ V/R1)\ (10)$$

Digital Input Interface Techniques

Many applications for bar graph arrays are in digital systems. While the data being displayed may relate directly to an analog signal, it often will be converted to a digital format for processing. This conversion can be accomplished by a microprocessor and/or dedicated hardware. Several interface techniques that have been developed for displaying this digitized data in bar graph form are covered in this section. A list of digital input integrated circuits suitable for use as bar graph drivers is compiled in Table III.

Binary Coded Decimal (BCD) is one commonly used method for coding display data in digital systems. Figures 7 and 8 contain circuits designed for interfacing BCD systems to a ten element bar graph. In each case a 1-of-10 decoder (7442) is used to convert the BCD information to the display format. The circuit in Figure 7 drives the bar graph in position indicator mode. That is, only the one LED corresponding to the BCD input is on at any one time. The circuit in Figure 8 has additional hardware to provide a true bar graph display. Therefore, when any output is decoded and turned on, that LED and all the LEDs below it are illuminated. The circuits in Figures 7 and 8 use the HDSP-4840 yellow bar graph with the forward current set nominally at 10 mA DC.

Figure 9 shows a thirty element, DC driven bar graph array utilizing the National MM5450 LED Display Driver. The circuit uses 3 HDSP-4830 high efficiency red bar graphs end stacked to form the display portion of the circuit. The MM5450 is a serial in-parallel out shift register with 34 output pins that can sink up to 15 mA each. This current can be adjusted by an external potentiometer applied between V_{DD} (pin 20) and Brightness Control (pin 19). Serial data transfer from the data source, in this case the microprocessor, to the display driver is accomplished with the two signals SERIAL DATA and CLOCK. By using a format of a leading “1” bit followed by 35 data bits, data transfer is allowed with a minimal hardware interface. The 35 data bits are latched after the 36th bit is complete. This provides non-multiplexed, direct drive to the bar graph array.

Figure 10 contains the software necessary to interface the MM5450 to the 6800 microprocessor. The serial display data is transferred from the microprocessor via bit 7 of the Data Bus. The data is clocked in each time the microprocessor writes to the MM5450. The clocking is accomplished through a combination of higher order addresses, R/W, VMA and $\phi 2$.

The software first outputs a start bit to the MM5450. Next, the binary number corresponding to the number of bar graph elements to be displayed is loaded from memory location BINARY. This value is subtracted from $34_{10} = 22_H$, leaving the number of OFF elements to be clocked. These OFF bits are clocked first, followed immediately by the ON bits.

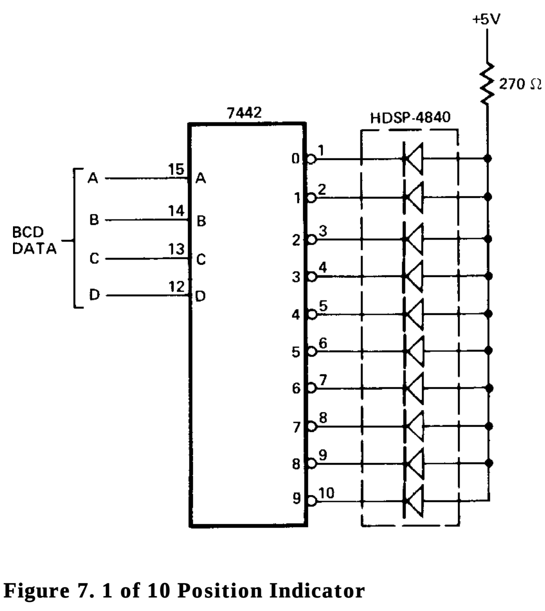

Figure 7. 1 of 10 Position Indicator

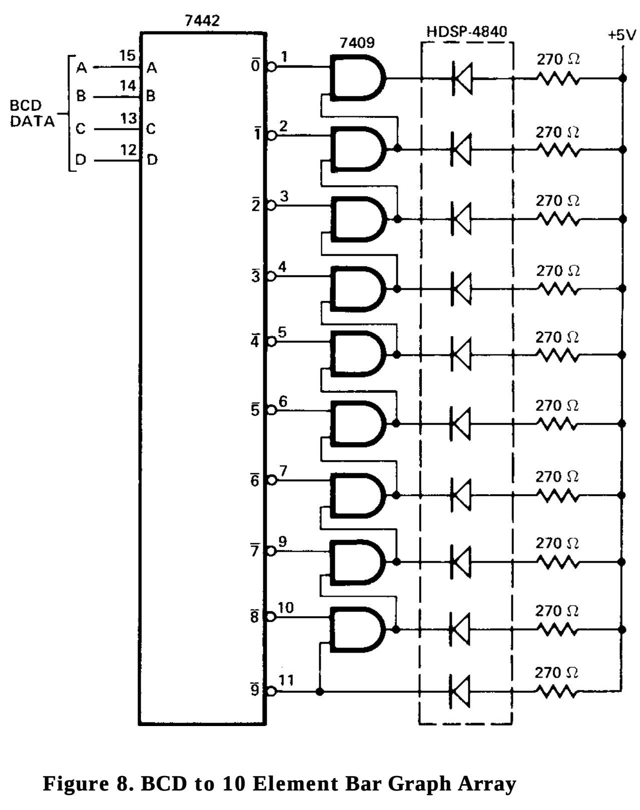

Figure 8. BCD to 10 Element Bar Graph Array

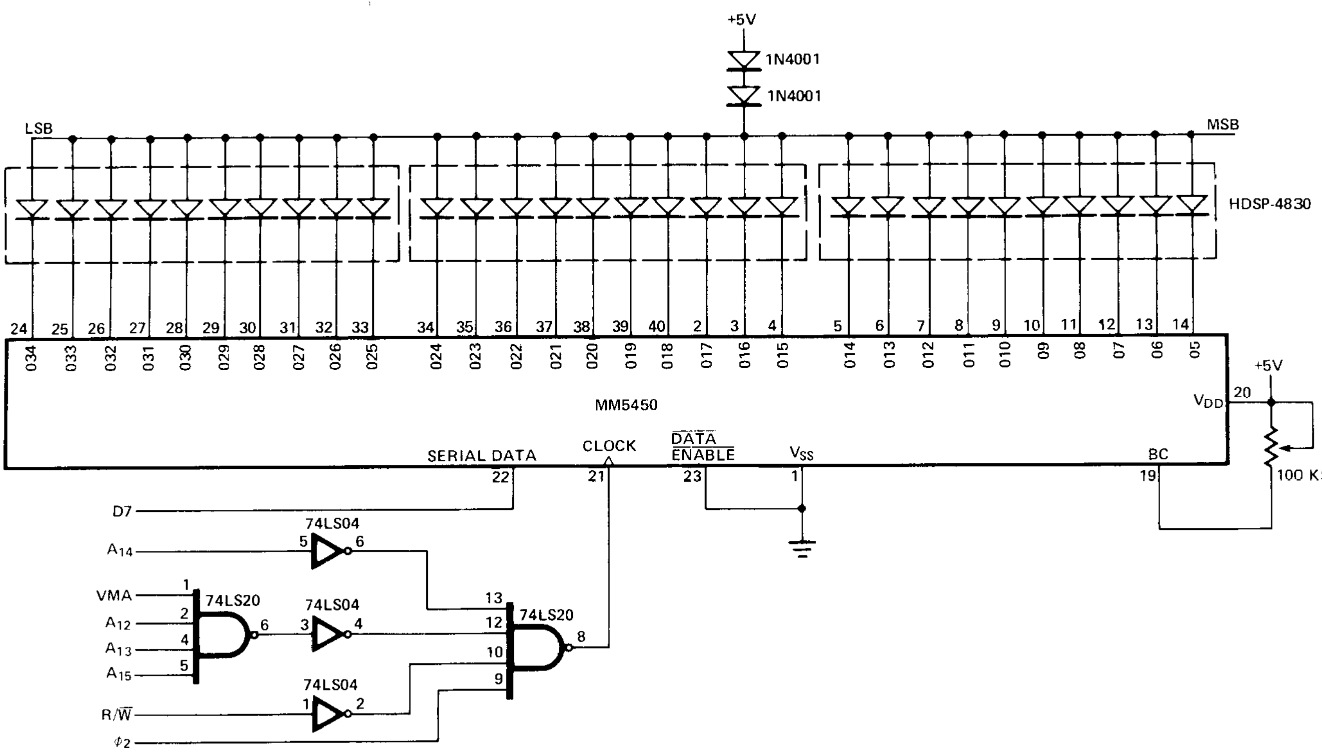

Figure 9. Serial Data Interface Between 6800 and 30 Element Bar Graph Array

```
                      ASMB, A, L
      B000            DSPLAY   EQU    $B000
0006                           ORG    $0006
0006                  BINARY   RMB    $1         NUMBER OF ELEMENTS ON (30₁₀ = 1E_H OR LESS)
0400                           ORG    $0400
0400  86   80                  LDA A  I, $80
0402  B7   B000                STA A  E, DSPLY    OUTPUT START BIT
0405  D6   06                  LDA B  D, BINARY   GET BINARY
0407  86   22                  LDA A  I, $22
0409  10                       SBA                DETERMINE NUMBER OF ZEROS
040A  81   00         ZEROS    CMP A  I, $0       NO ZEROS THEN BRANCH, ELSE CONTINUE
040C  27   06                  BEQ    ONES
040E  7F   B000                CLR    E, DSPLY    OUTPUT ZERO
0411  4A                       DEC A
0412  20   F6                  BRA    ZEROS       LOOP
0414  86   80         ONES     LDA A  I, $80      LOAD ONES
0416  C1   00                  CMP B  I, $00
0418  27   07                  BEQ    QUIT        BRANCH IF DONE, ELSE CONTINUE
041A  B7   B000                STA A  E, DSPLY    OUTPUT ONE
041D  5A                       DEC B
041E  7E   0416                JMP    ONES + 2    LOOP
0421  7F   B000       QUIT     CLR    E, DSPLY    FINAL CLOCK, DATA LATCHED
                               END
```

Figure 10. Software to Interface 6800 to the Circuit in Figure 9

Finally, the 36th clock pulse is generated, and the bar graph is illuminated. This display will remain illuminated without the need for microprocessor interaction until the data needs changing.

The user should ensure that the correct number of clock pulses are always applied to the MM5450. If this condition is violated once, the bar graph will display erroneous data until it is reset. Due to the lack of an external reset pin on the MM5450, the chip must then be turned off and subsequently repowered to reset and initialize correctly.

Figure 11 shows an 8080A microprocessor to bar graph interface utilizing the Intersil ICM7218A. This display driver has an 8x8 static RAM to store display data, sourcing and sinking drivers, and refresh timing for interfacing up to 64 LED elements to a microprocessor. However, the ICM7218A drives these elements at 20mA $I_{PEAK/ELEMENT\ (MINIMUM)}$ on a 12%

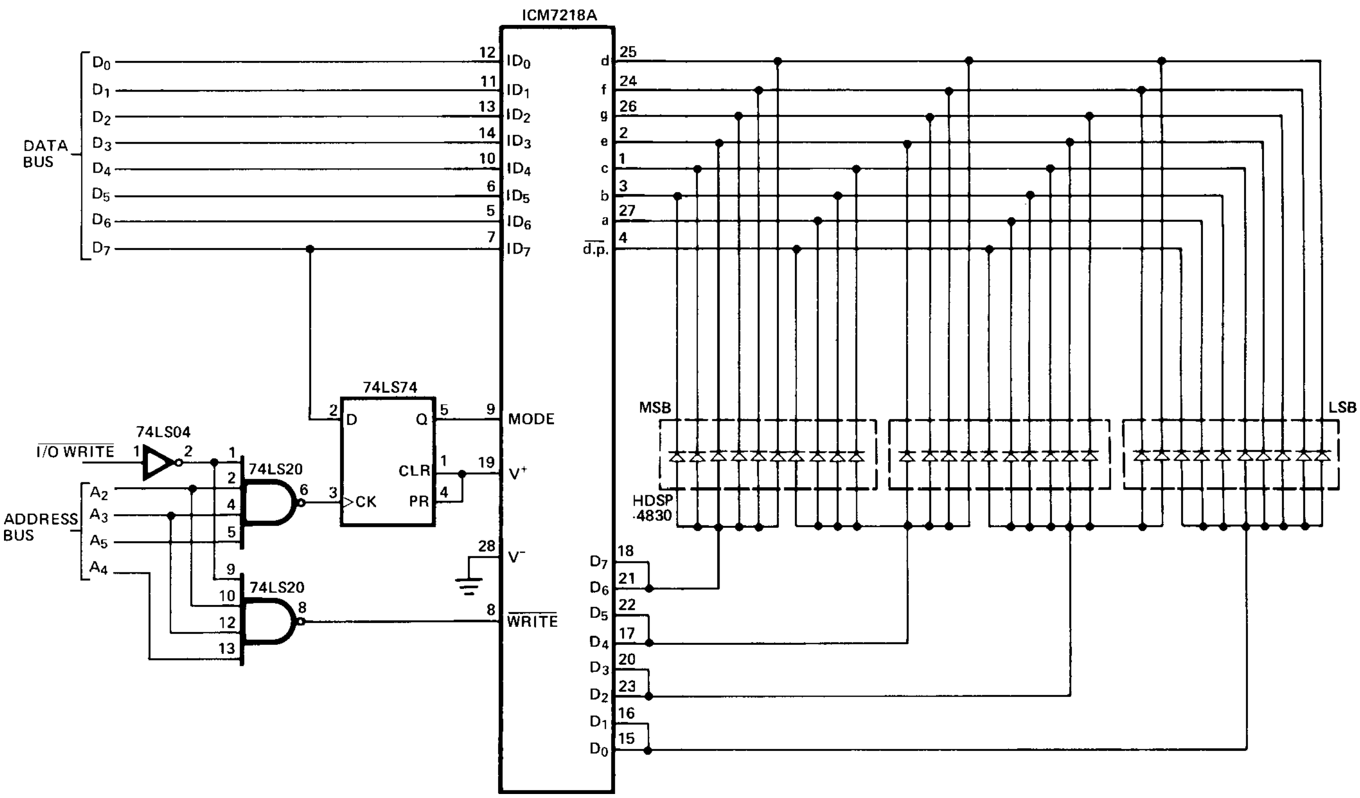

Figure 11. Parallel Data Interface Between 8080A and 30 Element Bar Graph Array

duty factor which may result in unacceptably low average current and brightness. For this reason, the eight digit drivers are paralleled in pairs in Figure 11. This results in a thirty element bar graph array operating at 20 mA $I_{PEAK/SEGMENT\ (MINIMUM)}$ with a duty factor of 24%.

The software to interface the 8080A to the ICM7218A is shown in Figure 14. With the MODE input at a logic, high WRITE is pulsed low. This clocks a control word from the data bus to the ICM7218A. This control word is decoded as described in Figure 12. Inputs ID_4, ID_5, and ID_7 are all logic highs which initialize the device into the proper mode of operation. This means that the next eight data words that are clocked into the ICM7218A will appear on the strobed outputs.

MODE = 1 CONTROL WORD FORMAT

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
1	X	1	C	X	X	X	X

C = 0 BLANK DISPLAY (RAM CONTENTS UNCHANGED)
C = 1 NORMAL OPERATION
X = DON'T CARE

MODE = 0 DATA WORD FORMAT

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
d.p.	a	b	c	e	g	f	d

UNCODED SEGMENT INFORMATION

LOGIC 1 REPRESENTS AN ON SEGMENT FOR ALL INPUTS EXCEPT d.p., WHERE LOGIC 0 REPRESENTS AN ON d.p.

Figure 12. MODE and DATA Words for the ICM7218A

Memory location BINARY contains the number of elements in the bar graph that are to be illuminated. The software converts this information to bar graph form by rotating a 1 bit through the accumulator until BINARY decrements to zero. Since the logic is inverted for the d.p. output, an exclusive OR mask has been used to complement this bit. Also since the digit drivers have been paired, two

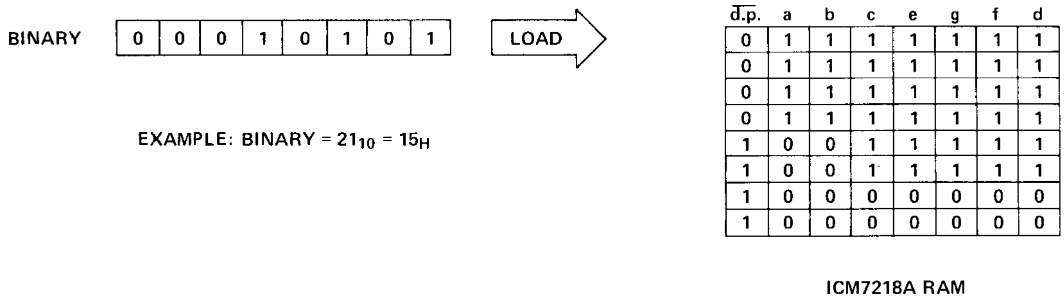

Figure 13. Subroutine LOAD

```
001C                     DSPLY   EQU    001CH
002C                     MODE    EQU    002CH
0000                             ORG    0E000H
E000  01                 BINARY  DB     1          ;NUMBER OF ELEMENTS ON (30₁₀ = 1EH OR LESS)
E001  F5                 LOAD    PUSH   PSW
E002  C5                         PUSH   B
E003  E5                         PUSH   H
E004  3E  F0                     MVI    A, 0F0H
E006  D3  2C                     OUT    MODE       ;MODE IS ONE
E008  D3  1C                     OUT    DSPLY      ;CLOCK CONTROL WORD
E00A  3E  00                     MVI    A, 00H
E00C  D3  2C                     OUT    MODE       ;MODE IS ZERO
E00E  06  08                     MVI    B, 08H     ;BIT COUNTER
E010  0E  04                     MVI    C, 04H     ;BYTE COUNTER
E012  21  00  E0                 LXI    H, BINARY  ;GET BINARY
E015  7E                         MOV    A, M
E016  FE  00                     CPI    00
E018  CA  33  E0                 JZ     LOOP 1     ;JUMP IF ZERO, ELSE CONTINUE
E01B  3E  00             CLEAR   MVI    A, 00
E01D  37                 SET     STC               ;SET CARRY
E01E  17                         RAL               ;ROTATE ONE BIT
E01F  35                         DCR    M
E020  CA  33  E0                 JZ     LOOP 1     ;JUMP IF ZERO, ELSE CONTINUE
E023  05                         DCR    B          ;DECREMENT BIT COUNTER
E024  C2  1D  E0                 JNZ    SET        ;JUMP IF NOT ZERO, ELSE CONTINUE
E027  EE  80                     XRI    80H        ;COMPLEMENT BIT 7
E029  D3  1C                     OUT    DSPLY      ;CLOCK DISPLAY
E02B  D3  1C                     OUT    DSPLY      ;CLOCK DISPLAY
E02D  0D                         DCR    C          ;DECREMENT BYTE COUNTER
E02E  06  08                     MVI    B, 08H     ;RESET BIT COUNTER
E030  C3  1B  E0                 JMP    CLEAR      ;START NEW BYTE
E033  EE  80             LOOP 1  XRI    80H        ;COMPLEMENT BIT 7
E035  D3  1C                     OUT    DSPLY      ;CLOCK DISPLAY
E037  D3  1C                     OUT    DSPLY      ;CLOCK DISPLAY
E039  0D                         DCR    C          ;DECREMENT BYTE COUNTER
E03A  CA  42  E0                 JZ     QUIT       ;JUMP IF ZERO, ELSE CONTINUE
E03D  3E  80                     MVI    A, 80H     ;ENSURE BIT 7 CORRECT
E03F  C3  35  E0                 JMP    LOOP 1 + 2
E042  E1                 QUIT    POP    H
E043  C1                         POP    B
E044  F1                         POP    PSW
E045  C9                         RET
E046                             END
```

Figure 14. Software to Interface 8080A to the Circuits in Figure 11

OUT put instructions are required for each byte decoded. The software is graphically depicted in Figure 13. When the ICM7218A has received nine words (control word and eight data words), the information is displayed on the bar graph. This bar graph array will remain illuminated without the need for microprocessor interaction until the data needs changing.

Table I. Filter Materials

LED Color	Panelgraphic	SGL Homalite	3M Co.	Glarecheq	Rohm and Haas	Schott	OCLI	Polaroid
Standard Red	Ruby Red 60 Dark Red 63 Purple 90	H100-1600 H100-1605 H100-1804 (Purple)	R6510 P7710	Spectrafilter 112 Spectraflter 118	Plexiglass 2423 Oroglass 2414	RG-645 RG-630		
High Efficiency Red	Scarlet Red 65 Neutral Gray 10	H100-1670	R6310 N0220 (Neut.Gray)	Spectrafilter 110 Spectrafilter 105 (Neutral Gray)		RG-610	Sunguard™ (Neut.Gray)	HNCP10 (Neut. Gray)
Yellow	Yellow 27 Neutral Gray 10	H100-1720	A5910 N0220 (Neut.Gray)	Spectrafilter 106 Spectrafilter 105 (Neutral Gray)			Sunguard™ (Neut.Gray)	HNCP10 (Neut.Gray)

Addresses for companies listed above.

Panelgraphic Corp., 10 Henderson Dr.
West Caldwell, NJ 07006 (201) 227-1500

SGL Homalite, 11 Brookside Drive
Wilmington, DE 19804 (302) 652-3686

3M Company, Visual Products Division
3M Center, Bldg. 220-10W
St Paul, MN 55101 (612) 733-0128

Glarecheq, Chequers Engraving Ltd.
1-4 Christina Street
London EC2A P4A England (01)739-6964

Rohm and Haas, Independence Mall West
Philadelphia, PA 19105 (215) 592-3000

Schott Optical Glass, Duryea, PA 13642
(717) 457-7485

Optical Coating Labs, Inc. (OCLI)
2789 Griffen Avenue
Santa Rosa,CA 95401 (707)545-6440

Polaroid Corporation, Polarizer Division
20 Ames Street, Cambridge,MA
(617) 577-2000/3655

HEWLETT® PACKARD

Table II. Analog Input Bar Graph Array Drivers

Part Number	Vendor*	Drive Conditions	Scale	Elements	Comments
UAA170	Siemens	≤ 50 mA DC	External	16	Position indicator only, user sets scale
UAA180	Siemens	10 mA DC (typ)	External	12	User sets scale
TL489	TI	≤ 40 mA DC	Linear	5	200 mV increments
TL487	TI	≤ 40 mA DC	Log	5	3 dB increments
TL490	TI	≤ 40 mA DC	Linear	10	50 - 200 mV adjustable increments
TL480	TI	≤ 40 mA DC	Log	10	2 dB increments
TL491	TI	≤ -25 mA DC	Linear	10	50 - 200 mV adjustable increments
TL481	TI	≤ -25 mA DC	Log	10	2 dB increments
LM3914	National	2 ≤ I ≤ 30 mA DC	Linear	10	Position indicator/bar option
LM3915	National	2 ≤ I ≤ 30 mA DC	Log	10	Position indicator/bar option
LM3916	National	2 ≤ I ≤ 30 mA DC	Log	10	Position indicator/bar option
U237B	AEG-Tel.	20 mA (typ)	Linear	5	200 mV increments (200 mV-1000 mV)
U244B	AEG-Tel.	20 mA (typ)	Linear	5	180 mV increments (200 mV-1000 mV with overlap)
U247B	AEG-Tel.	20 mA (typ)	Linear	5	200 mV increments (100 mV-900 mV)
U254B	AEG-Tel.	20 mA (typ)	Linear	5	100 mV increments (110 mV-900 mV with overlap)
U257B	AEG-Tel.	20 mA (typ)	Log	5	-15 dB to +6 dB
U267B	AEG-Tel.	20 mA (typ)	Log	5	-20 dB to +3 dB
XR-2277	Exar	≤ 18 mA DC	Log	12	-30 dB to +6 dB, position indicator/bar option
XR-2278	Exar	≤ 18 mA DC	Log	12	-20 dB to +8 dB, position indicator/bar option
XR-2279	Exar	≤ 18 mA DC	Log	12	3 dB increments, position indicator/bar option

*This is a partial list of vendors. Other suppliers may exist.

Table III. Digital Input Bar Graph Drlvers

Part Number	Vendor*	Drive Conditions	Elements	Comments
MM74C911	National	100 mA pk, 25% DF	32	Software decode, parallel interface
MM5450/51	National	≤ 15 mA DC	34/35	Software decode, serial interface
ICM7218A	Intersil	20 mA pk, 12% DF	64	Common Anode, software decode, parallel interface
8243	Signetics	13 mA DC	8	n of 8 decoder
7442	Tl, Fairchild, et al.	16 mA DC	10	1 of 10 decoder

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-235-0312 or (408) 654-8675

Far East/Australasia: Call your local HP sales office.

Japan: (81 3) 3335-8152

Europe: Call your local HP sales office.

Data Subject to Change

Obsoletes 5953-0452

Printed in U.S.A. 5965-6545E (5/97)